Altera’s Avalon Communication Fabric

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Altera’s Avalon Bus

Something like “PCI on a chip”

Described in Altera’s *Avalon Memory-Mapped Interface Specification* document.

Protocol defined between peripherals and the “bus” (actually a fairly complicated circuit).
Intended System Architecture

Avalon-MM System

- Processor
  - 32-bit Avalon-MM Master Port

- Ethernet MAC
  - 32-bit Avalon-MM Master Port

- Custom Logic
  - 64-bit Avalon-MM Master Port

System Interconnect Fabric

- 32-bit Avalon-MM Slave Port
  - SDRAM Controller

- 16-bit Avalon-MM Slave Port
  - UART

- 64-bit Avalon-MM Slave Port
  - Custom Logic

- 8-bit Avalon-MM Tristate Slave Port
  - Flash Memory Chip

- 16-bit Avalon-MM Tristate Slave Port
  - SRAM Memory Chip

- SDRAM Memory Chip
  - RS-232

Source: Altera
Masters and Slaves

Most bus protocols draw a distinction between

**Masters**: Can initiate a transaction, specify an address, etc. E.g., the Nios II processor

**Slaves**: Respond to requests from masters, can generate return data. E.g., a video controller

Most peripherals are slaves.

Masters speak a more complex protocol

Bus arbiter decides which master gains control
The Simplest Slave Peripheral

Avalon-MM Interface

(Avalon-MM Slave Port)

Application-Specific Interface

Avalon-MM Peripheral

\[
\text{writedata}[15..0] \quad \text{pio\_out}[15..0]
\]

\[
\text{write} \quad \text{CLK\_EN}
\]

\[
\text{chipselect} \quad \text{D} \quad \text{Q}
\]

\[
\text{clk}
\]

Basically, “latch when I’m selected and written to.”
Used by the SOPC Builder’s New Component Wizard to match up VHDL entity ports with Avalon bus signals.

*type_interface_signal*

type is is typically *avs* for Avalon-MM Slave

*interface* is the user-selected name of the interface, e.g., *s1*.

*signal* is chipselect, address, etc.

Thus, *avs_s1_chipselect* is the chip select signal for a slave port called “s1.”
For a 16-bit connection that spans 32 halfwords,

Slave Signals

For a 16-bit connection that spans 32 halfwords, the signals are as follows:

- **clk**
- **reset**
- **chipselect**
- **address[4:0]**
- **read**
- **write**
- **byteenable[1:0]**
- **writedata[15:0]**
- **readdata[15:0]**
- **irq**

These signals connect between the Slave and Avalon components.
### Avalon Slave Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>Master clock</td>
</tr>
<tr>
<td>reset</td>
<td>Reset signal to peripheral</td>
</tr>
<tr>
<td>chipselect</td>
<td>Asserted when bus accesses peripheral</td>
</tr>
<tr>
<td>address[..]</td>
<td>Word address (data-width specific)</td>
</tr>
<tr>
<td>read</td>
<td>Asserted during peripheral→bus transfer</td>
</tr>
<tr>
<td>write</td>
<td>Asserted during bus→peripheral transfer</td>
</tr>
<tr>
<td>writedata[..]</td>
<td>Data from bus to peripheral</td>
</tr>
<tr>
<td>byteenable[..]</td>
<td>Indicates active bytes in a transfer</td>
</tr>
<tr>
<td>readdata[..]</td>
<td>Data from peripheral to bus</td>
</tr>
<tr>
<td>irq</td>
<td>peripheral→processor interrupt request</td>
</tr>
</tbody>
</table>

All are optional, as are many others for, e.g., flow-control and burst transfers.
The Nios II and Avalon bus are little-endian:

31 is the most significant bit, 0 is the least

Bytes and halfwords are right-justified:

<table>
<thead>
<tr>
<th></th>
<th>msb</th>
<th>lsb</th>
<th></th>
<th>lsb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Bit</td>
<td>31</td>
<td>24</td>
<td>23</td>
<td>16</td>
</tr>
<tr>
<td>Word</td>
<td>31</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Halfword</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Byte</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
entity avalon_slave is
    port (
        avs_s1_clk       : in  std_logic;
        avs_s1_reset_n   : in  std_logic;
        avs_s1_read      : in  std_logic;
        avs_s1_write     : in  std_logic;
        avs_s1_chipselect: in  std_logic;
        avs_s1_address   : in  std_logic_vector(4 downto 0);
        avs_s1_readdata  : out std_logic_vector(15 downto 0);
        avs_s1_writedata : in  std_logic_vector(15 downto 0);
    );
end avalon_slave;
Bus cycle starts on rising clock edge.
Data latched at next rising edge.
Such a peripheral must be purely combinational.
Slave Read Transfer w/ 1 wait state

Bus cycle starts on rising clock edge.
Data latched two cycles later.
Approach used for synchronous peripherals.
Basic Async. Slave Write Transfer

Bus cycle starts on rising clock edge.
Data available by next rising edge.
Peripheral may be synchronous, but must be fast.
Bus cycle starts on rising clock edge. Peripheral latches data two cycles later. For slower peripherals.
32 16-bit word interface

First 16 halfwords are data to be displayed on the LEDs.

Halfwords 16–31 all write to a “linger” register that controls cycling rate.

Red LEDs cycle through displaying memory contents.
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity de2_led_flasher is

  port ( 
    clk                : in  std_logic;
    reset_n            : in  std_logic;
    read               : in  std_logic;
    write              : in  std_logic;
    chipselect         : in  std_logic;
    address            : in  unsigned(4 downto 0);
    readdata           : out unsigned(15 downto 0);
    writedata          : in  unsigned(15 downto 0);
    leds               : out unsigned(15 downto 0) 
  );

end de2_led_flasher;
architecture rtl of de2_led_flasher is

  type ram_type is array(15 downto 0) of unsigned(15 downto 0);
signal RAM : ram_type;

signal ram_address, display_address : unsigned(3 downto 0);

signal counter_delay : unsigned(15 downto 0);
signal counter : unsigned(31 downto 0);

begin
  ram_address <= address(3 downto 0);
process (clk)
begin
if rising_edge(clk) then
  if reset_n = '0' then
    readdata <= (others => '0');
    display_address <= (others => '0');
    counter <= (others => '0');
    counter_delay <= (others => '1');
  else
    if chipselect = '1' then
      if address(4) = '0' then -- read or write RAM
        if read = '1' then
          readdata <= RAM(to_integer(ram_address));
        elsif write = '1' then
          RAM(to_integer(ram_address)) <= writedata;
        end if;
      end if;
    else
      if write = '1' then -- Change delay
        counter_delay <= writedata;
      end if;
    end if;
  end if;
end if;

else -- No access to us: update display
    leds <= RAM(to_integer(display_address));
    if counter = x"00000000" then
        counter <= counter_delay & x"0000";
        display_address <= display_address + 1;
    else
        counter <= counter - 1;
    end if;
end if;
end if;
end if;
end if;
end if;
end process;
end rtl;