Internet Radio

Embedded System Design

Design Proposal

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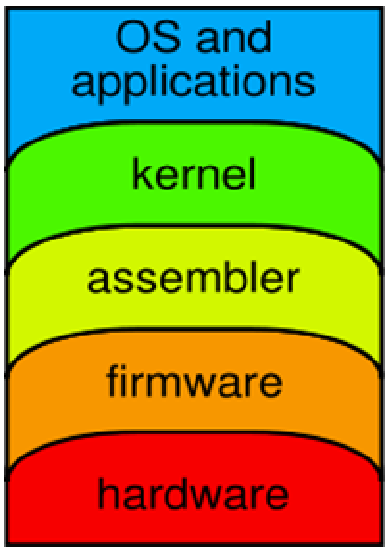
1. Introduction

The project aims to deliver radio from the internet to the user through the Altera DE2 board. The Altera board would fetch radio from a preprogrammed radio station from http://www.shoutcast.com and plays it using the on board audio controller.

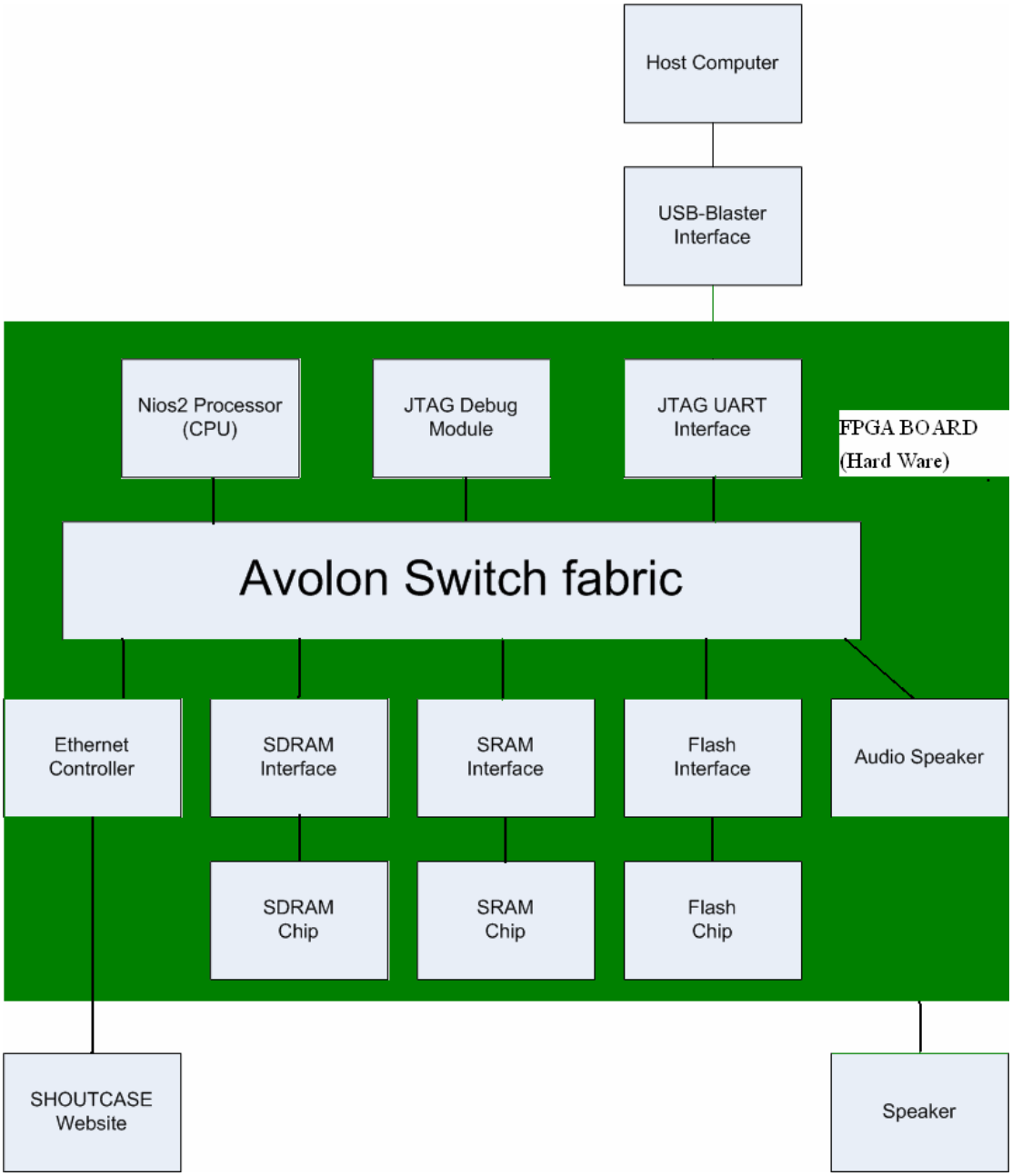
We propose to use the operating system- uClinux by setting up the software up to a point where the kernel can be downloaded to the Altera DE2 board. Under this operating system, the Nios would pass in a URL (for example: http://www.shoutcast.com/sbin/shoutcast-playlist.pls?rn=783&file=filename.pls) which delivers radio in the format of a mp3 playlist. The on board ethernet controller would be used with nios to establish a TCP connection to receive packets of the mp3 stream. The packet stream is then buffered, and decoded using a third-party mp3 decoder library. The resulting audio is fed into the on-board audio controller which converts the stream into audible sound.

2. Operating System

The first step of our project is to download the operating system- uClinux to the Altera DE2 board. We try to modify the C code from an Open Source Firmware project - U-Boot. U-Boot is a boot loader program that is stored in flash memory on the target system. The booting method is by using Blackfin processors contains a small on-chip boot kernel (Boot-ROM), which configures the appropriate peripheral for booting.



3. Block diagram

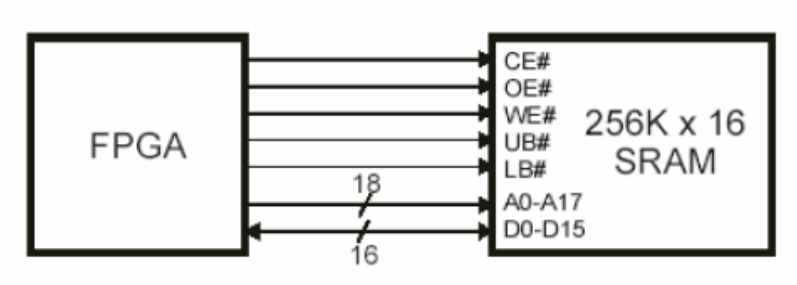


Ethernet Controller

The DE2 Board provides Ethernet Controller MD 9000A chip.

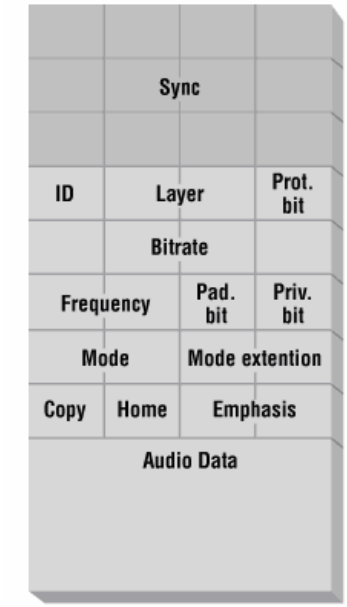
SRAM

We use the on board SRAM as our buffer and in the project, and two buffers are needed. One is to buffer the streams from the website to the MP3 Decoder; the other is to buffer the decoded data (raw data) from MP3 Decoder to Audio Speaker. The method is to control the clock such that each buffer works in certain time slot.



MP3 Decoder

The following is the MP3 Format. We use C program to write the MP3 Decoder.



3.1 Audio Speaker

The DE2 Board provides Audio CODEC WM8731 chip. The audio controller is included in the audio_wm8731.vhd and will expect the data input 16 bits in a periodic manner.

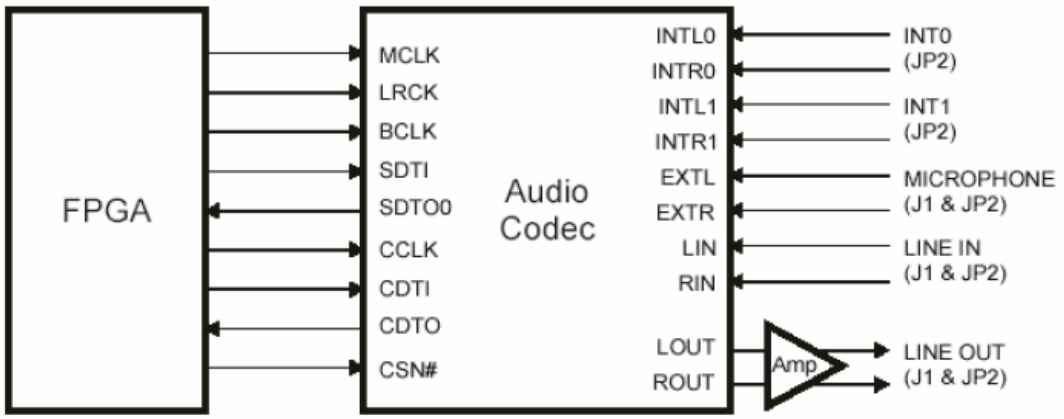


Figure 10 FPGA/Audio Codec Connection