Processors, FPGAs, and ASICs

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Spectrum of IC choices

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NMOS Transistor Cross Section

Inverter Transistors and Layout

NAND Gate Transistors and Layout

Full-custom ICs

Standard Cell ASICs

Channeled Gate Arrays
Spartan-IIE 1.8V FPGA Family: Functional Description

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can be modified by the user.

Spartan-IIE Array

The Spartan-IIE user-programmable gate array, shown in Figure 1, has a Basic Array Structure. Each of these elements will be discussed in detail in the following sections.

Input/Output Block

- **CLBs** provide the functional elements for constructing basic logic functions.
- **Dedicated block RAM memories** of 4096 bits each are available for design-specific memory applications.
- **Clock DLLs** for clock-distribution delay compensation are available for improved performance.
- **Versatile multi-level interconnect structure** allows easy and quick routing of signals on and off the chip.

Figure 1: Basic Spartan-IIE Family FPGA Block Diagram

The three IOB registers function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three registers and independent Clock Enable (CE) signals for each register.
Always 0

One for the XAB and one for the YAB

b0 Source

PC Stack

SR Stack

Frame Pointer

End-of-block-transfer interrupts

x0 One for the XAB, or

Six DMA channels supporting internal and external accesses

Input Registers

M4 24

Triggering from interrupt lines and all peripherals

The offset N (stored in the respective offset register)

High Address ALU

R7

YAB

Next PC

r31/i7

PAB

Program Counter

Global Registers

y0

Local Registers

Accumulator

Motorola DSP56301

DSP 56000 Programmer’s Model

Motorola DSP56301 ALU

Motorola DSP56301 AGU

FIR Filter in 56000

TI TMS320C6000 VLIW DSP

gcd:

save %sp, -112, %sp

mov %r0, %r1

b .LL3

mov %r1, %r0

mov %r1, %r0

.b.LL3:

mov %r0, %r1

call .rem, 0

mov %r0, %r1

cmp %r0, 0

ret

restore

move #samples, r0

move #coeffs, r4

move #n-1, m0

move m0, m4

movep y:input, x:(r0)+, x0 y:(r4)+, y0

cr a x:(r0)+, x0 y:(r4)+, y0

rep #n-1

mac x0, y0, a x:(r0)+, x0 y:(r4)+, y0

macr x0, y0, a (r0)-
mov ep a, y:output
FIR in One 'C6 Assembly Instruction

- Load a halfword (16 bits)
- Do this on unit D1

FIR LOOP:

LDH .D1  *A1++, A2  : Fetch next sample
[B0] SUB .L2  B0, 1, B0  : Decrement count
[B0]  B .S2  FIRLOOP  : Branch if non-zero
ADD .L1  A4, A3, A4  : Accumulate result

Predicated instruction (only if B0 non-zero)
Run these instruction in parallel

AX88796 Ethernet Controller

- AX88796 Fast Ethernet Controller is a high performance and highly integrated local CPU bus Ethernet Controller with embedded 10/100Mbps PHY/Transceiver and 8K*16 bit SRAM.
- Supports both 8 bit and 16 bit local interface, Home LAN PHY type media can be supported.
- As well as, the chip also provides optional Standard Print Port ( parallel port interface ), can be used for printer server device or treat as simple general I/O port. The chip also support upto 3/1 additional General Purpose In/Out pins.
- Ultra low power consumption is an outstanding feature and enlarges the application field. It is suitable for some power consumption sensitive product like small size embedded products, PDA (Personal Digital Assistant) and Palm size computer … etc.

SAA7114H Video Decoder

Philips SAA7114H Video Decoder

SAA7114H Registers, page 1 of 7 (!)

- This section provides a comprehensive overview of the SAA7114H Video Decoder registers, detailing their functions and operations.

Ethernet Controller Registers

- This section outlines the registers and functionalities associated with the AX88796 Ethernet Controller, offering insights into its architecture and usage.

Fixed-function: The 7400 series

- Quad NAND Gate
- Octal D Flip-Flop

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**Fig.3** Logic diagram (one gate).

**Fig.4** Function diagram.

**Fig.5** IEC logic symbol.