



CY22393
CY22394
CY22395

Three-PLL Serial-Programmable Flash-Programmable Clock Generator

Features

- Three integrated phase-locked loops (PLLs)
- Ultra-wide divide counters (8-bit Q, 11-bit P, and 7-bit post divide)
- Improved linear crystal load capacitors
- Flash programmability with external programmer
- Field-programmable
- Low-jitter, high-accuracy outputs
- Power-management options (Shutdown, OE, Suspend)
- Configurable crystal drive strength
- Frequency select via three external LVTTTL inputs
- 3.3V operation
- 16-pin TSSOP package
- CyClocksRT™ support

Advanced Features

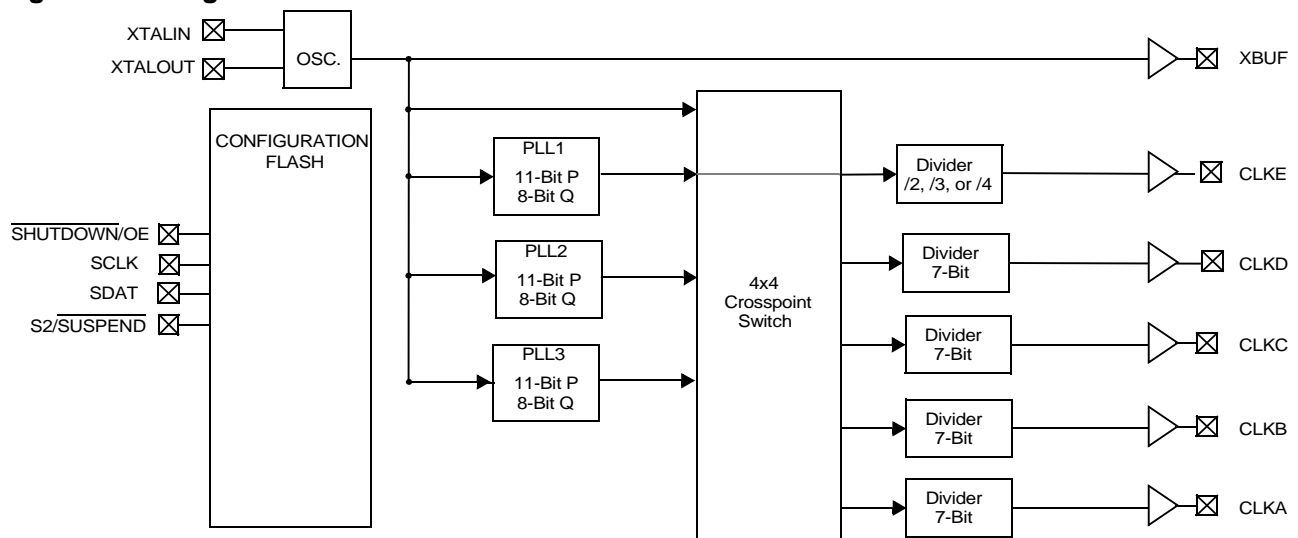
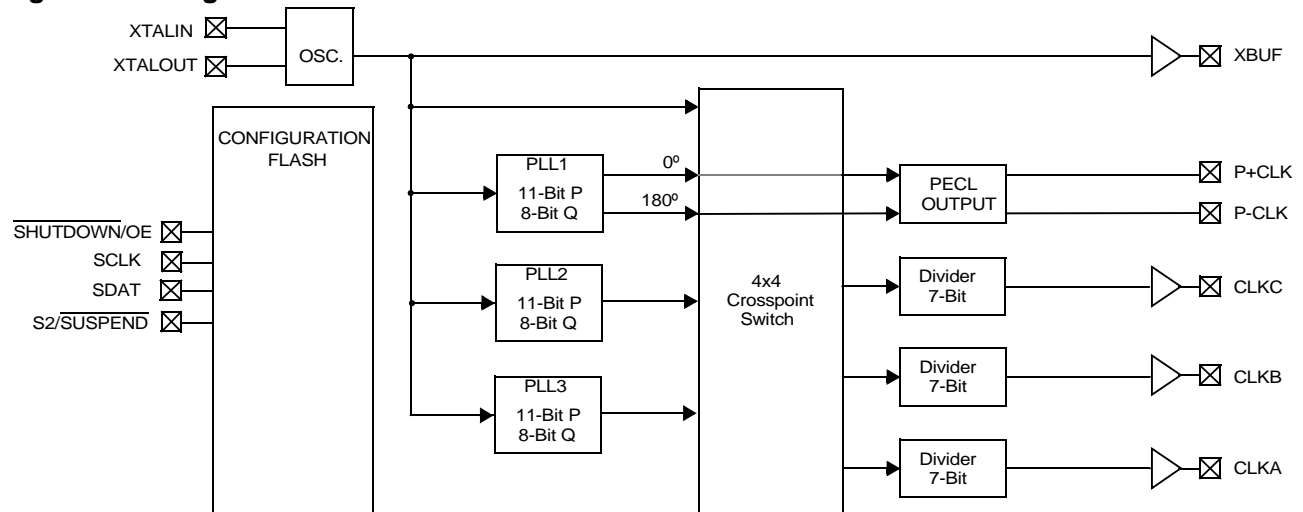
- Serial-programmable
- Configurable output buffer
- Digital VCXO
- High-frequency LVPECL output (CY22394 only)
- 3.3/2.5V outputs (CY22395 only)

Benefits

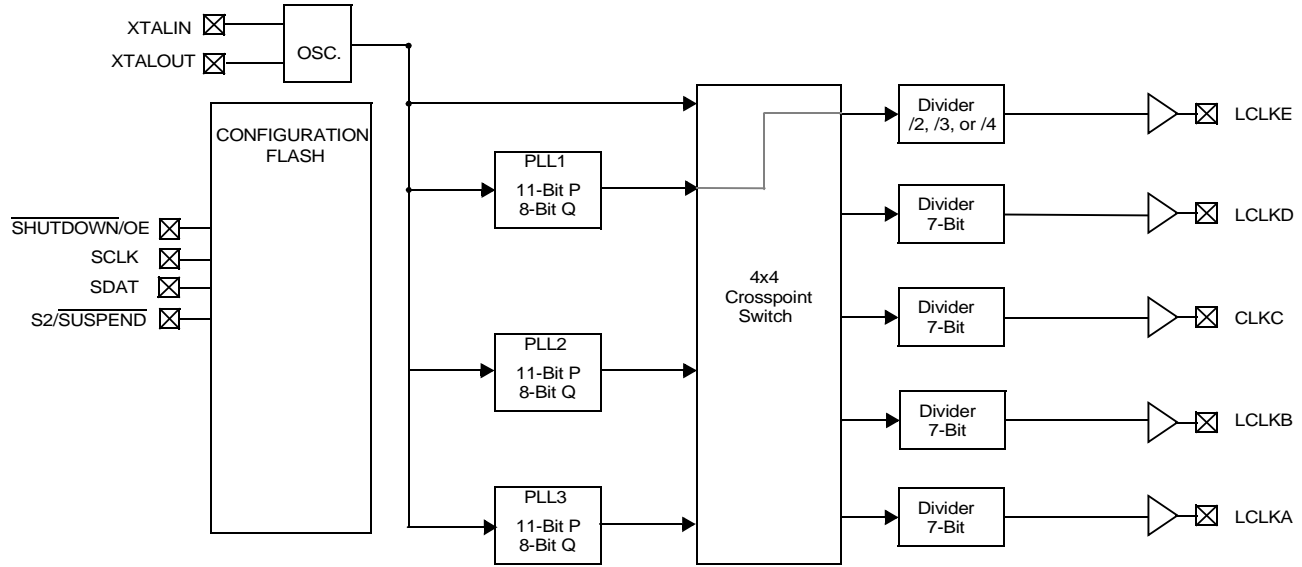
- Generates up to three unique frequencies on up to six outputs from an external source.
- Allows for 0-ppm frequency generation and frequency conversion in the most demanding applications.
- Improves frequency accuracy over temperature, age, process, and initial ppm offset.
- Non-volatile programming enables easy customization, ultra-fast turnaround, performance tweaking, design timing margin testing, inventory control, lower part count, and more secure product supply. In addition, any part in the family can be programmed multiple times, which reduces programming errors and provides an easy upgrade path for existing designs.
- In-house programming of samples and prototype quantities are available using the CY3672 FTG Development Kit. Production quantities are available through Cypress Semiconductor's value-added distribution partners or by using third-party programmers from BP Microsystems, HiLo Systems, and others.
- Performance suitable for high-end multimedia, communications, industrial, A/D converters, and consumer applications.
- Supports numerous low-power application schemes and reduces electromagnetic interference (EMI) by allowing unused outputs to be turned off.
- Adjust crystal drive strength for compatibility with virtually all crystals.
- 3-bit external frequency select options for PLL1, CLKA, and CLKB.
- Industry-standard supply voltage.
- Industry-standard packaging saves on board space.
- Easy to use software support for design entry.
- Allows in-system programming into volatile configuration memory. All frequency settings can be changed providing literally millions of frequency options.
- Adjust output buffer strength to lower EMI or improve timing margin.
- Fine tune crystal oscillator frequency by changing load capacitance.
- Differential output up to 400 MHz.
- Provides interfacing option for low-voltage parts.

Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY22393FC	6 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–166 MHz (reference clock)	Up to 200 MHz	Commercial Temperature
CY22393FI	6 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–150 MHz (reference clock)	Up to 166 MHz	Industrial Temperature
CY22394FC	1 PECL/ 4 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–166 MHz (reference clock)	100 MHz–400 MHz (PECL) Up to 200 MHz (CMOS)	Commercial Temperature
CY22394FI	1 PECL/ 4 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–150 MHz (reference clock)	125 MHz–375 MHz (PECL) Up to 166 MHz (CMOS)	Industrial Temperature
CY22395FC	4 LVCMOS/ 1 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–166 MHz (reference clock)	Up to 200 MHz (3.3V) Up to 133 MHz (2.5V)	Commercial Temperature
CY22395FI	4 LVCMOS/ 1 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–150 MHz (reference clock)	Up to 166 MHz (3.3V) Up to 133 MHz (2.5V)	Industrial Temperature

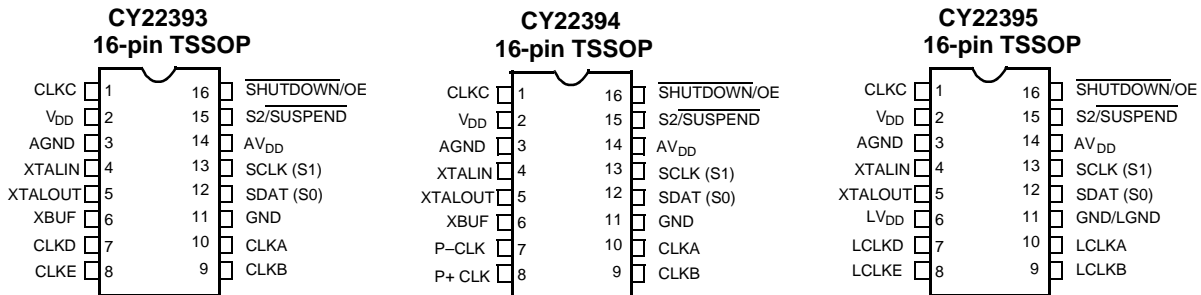
Logic Block Diagram — CY22393

Logic Block Diagram — CY22394


Logic Block Diagram — CY22395



LCLKA, LCLKB, LCLKD, LCLKE referenced to LVDD

Pin Configurations



Pin Summary

Name	Pin Number CY22393	Pin Number CY22394	Pin Number CY22395	Description
CLKC	1	1	1	Configurable clock output C
V _{DD}	2	2	2	Power supply
AGND	3	3	3	Analog Ground
XTALIN	4	4	4	Reference crystal input or external reference clock input
XTALOUT	5	5	5	Reference crystal feedback
XBUF	6	6	N/A	Buffered reference clock output
LV _{DD}	N/A	N/A	6	Low Voltage Clock Output Power Supply
CLKD or LCLKD	7	N/A	7	Configurable clock output D; LCLKD referenced to LVDD
P-CLK	N/A	7	N/A	LV PECL Output ^[1]
CLKE or LCLKE	8	N/A	8	Configurable clock output E; LCLKE referenced to LVDD
P+ CLK	N/A	8	N/A	LV PECL Output ^[1]
CLKB or LCLKB	9	9	9	Configurable clock output B; LCLKB referenced to LVDD

Note:

1. LVPECL outputs require an external termination network.

Pin Summary (continued)

Name	Pin Number CY22393	Pin Number CY22394	Pin Number CY22395	Description
CLKA or LCLKA	10	10	10	Configurable clock output A; LCLKA referenced to LVDD
GND/LGND	11	11	11	Ground
SDAT (S0)	12	12	12	Two Wire Serial Port Data. S0 value latched during start-up
SCLK (S1)	13	13	13	Two Wire Serial Port Clock. S1 value latched during start-up
AV _{DD}	14	14	14	Analog Power Supply
S2/ SUSPEND	15	15	15	General Purpose Input for Frequency Control; bit 2. Optionally Suspend mode control input
SHUTDOWN/ OE	16	16	16	Places outputs in three-state condition and shuts down chip when LOW. Optionally, only places outputs in three-state condition and does not shut down chip when LOW

Operation

The CY22393, CY22394, and CY22395 are a family of parts designed as upgrades to the existing CY22392 device. These parts have similar performance to the CY22392, but provide advanced features to meet the needs of more demanding applications.

The clock family has three PLLs which, when combined with the reference, allow up to four independent frequencies to be output on up to six pins. These three PLLs are completely programmable.

Configurable PLLs

PLL1 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL1 is sent to two locations: the crosspoint switch and the PECL output (CY22394). The output of PLL1 is also sent to a /2, /3, or /4 synchronous post-divider that is output through CLKE. The frequency of PLL1 can be changed via serial programming or by external CMOS inputs, S0, S1, and S2. See the following section on general-purpose inputs for more detail.

PLL2 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL2 is sent to the crosspoint switch. The frequency of PLL2 can be changed via serial programming.

PLL3 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL3 is sent to the crosspoint switch. The frequency of PLL3 can be changed via serial programming.

General-Purpose Inputs

S2 is a general-purpose input that can be programmed to allow for two different frequency settings. Options that may be switched with this general-purpose input are as follows: the frequency of PLL1, the output divider of CLKB, and the output divider of CLKA.

The two frequency settings are contained within an eight-row frequency table. The values of SCLK (S1) and SDAT (S0) pins are latched during start-up and used as the other two indexes into this array.

CLKA and CLKB both have 7-bit dividers that point to one of two programmable settings (register 0 and register 1). Both clocks share a single register control, so both must be set to register 0, or both must be set to register 1.

For example, the part may be programmed to use S0, S1, and S2 (0,0,0 to 1,1,1) to control eight different values of P and Q on PLL1. For each PLL1 P and Q setting, one of the two CLKA and CLKB divider registers can be chosen. Any divider change as a result of switching S0, S1, or S2 is guaranteed to be glitch free.

Crystal Input

The input crystal oscillator is an important feature of this family of parts because of its flexibility and performance features.

The oscillator inverter has programmable drive strength. This allows for maximum compatibility with crystals from various manufacturers, process, performance, and quality.

The input load capacitors are placed on-die to reduce external component cost. These capacitors are true parallel-plate capacitors for ultra-linear performance. These were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. Non-linear (FET gate) crystal load capacitors should not be used for MPEG, POTS dial tone, communications, or other applications that are sensitive to absolute frequency requirements.

The value of the load capacitors is determined by six bits in a programmable register. The load capacitance can be set with a resolution of 0.375 pF for a total crystal load range of 6 pF to 30 pF.

For driven clock inputs the input load capacitors may be completely bypassed. This enables the clock chip to accept driven frequency inputs up to 166 MHz. If the application requires a driven input, then XTALOUT must be left floating.

Digital VCXO

The serial programming interface may be used to dynamically change the capacitor load value on the crystal. A change in crystal load capacitance corresponds with a change in the reference frequency.

For special pullable crystals specified by Cypress, the capacitance pull range is +150 ppm to -150 ppm from midrange.

Be aware that adjusting the frequency of the reference will affect all frequencies on all PLLs in a similar manner since all frequencies are derived from the single reference.

Output Configuration

Under normal operation there are four internal frequency sources that may be routed via a programmable crosspoint switch to any of the four programmable 7-bit output dividers. The four sources are: reference, PLL1, PLL2, and PLL3. The following is a description of each output.

CLKA's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. See the section on General-Purpose Inputs for more information.

CLKB's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. See the section on General-Purpose Inputs for more information.

CLKC's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.

CLKD's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register. For the CY22394, CLKD is brought out as the complimentary version of a LV PECL Clock referenced to CLKE, bypassing both the crosspoint switch and 7-bit post divider.

CLKE's output originates from PLL1 and goes through a post divider that may be programmed to /2, /3, or /4. For the CY22394, CLKE is brought out as an LV PECL Clock, bypassing the post divider.

XBUF is simply the buffered reference.

The Clock outputs have been designed to drive a single point load with a total lumped load capacitance of 15 pF. While driving multiple loads is possible with the proper termination it is generally not recommended.

Power-Saving Features

The $\overline{\text{SHUTDOWN/OE}}$ input three-states the outputs when pulled LOW. If system shutdown is enabled, a LOW on this pin also shuts off the PLLs, counters, reference oscillator, and all other active components. The resulting current on the V_{DD} pins will be less than 5 mA (typical). After leaving shutdown mode, the PLLs will have to relock.

The S2/SUSPEND input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.

With the serial interface, each PLL and/or output can be individually disabled. This provides total control over the power savings.

Improving Jitter

Jitter Optimization Control is useful in mitigating problems related to similar clocks switching at the same moment,

causing excess jitter. If one PLL is driving more than one output, the negative phase of the PLL can be selected for one of the outputs (CLKA–CLKD). This prevents the output edges from aligning, allowing superior jitter performance.

Power Supply Sequencing

For parts with multiple V_{DD} pins, there are no power supply sequencing requirements. The part will not be fully operational until all V_{DD} pins have been brought up to the voltages specified in the "Operating Conditions" table.

All grounds should be connected to the same ground plane.

CyClocksRT Software

CyClocksRT is our second-generation software application that allows users to configure this family of devices. The easy-to-use interface offers complete control of the many features of this family including, but not limited to, input frequency, PLL and output frequencies, and different functional options. Data sheet frequency range limitations are checked and performance tuning is automatically applied. CyClocksRT also has a power estimation feature that allows the user to see the power consumption of a specific configuration. You can download a free copy of CyberClocks that includes CyClocksRT for free on Cypress's web site at www.cypress.com

CyClocksRT is used to generate P, Q, and divider values used in serial programming. There are many internal frequency rules which are not documented in this data sheet, but are required for proper operation of the device. These rules can be checked by using the latest version of CyClocksRT.

Junction Temperature Limitations

It is possible to program this family such that the maximum Junction Temperature rating is exceeded. The package q_{JA} is 115 °C/W. Use the CyClocksRT power estimation feature to verify that the programmed configuration meets the Junction Temperature and Package Power Dissipation maximum ratings.

Dynamic Updates

The output divider registers are not synchronized with the output clocks. Changing the divider value of an active output will likely cause a glitch on that output.

PLL P and Q data is spread between three bytes. Each byte becomes active on the acknowledge for that byte, so changing P and Q data for an active PLL will likely cause the PLL try to lock on an out-of-bounds condition. For this reason, it is recommended that the PLL being programmed be turned off during the update. This can be done by setting the PLL*_En bit LOW.

PLL1, CLKA, and CLKB each have multiple registers supplying data. Programming these resources can be accomplished safely by always programming an inactive register, and then transitioning to that register. This allows these resources to stay on during programming.

The serial interface is active even with the $\overline{\text{SHUTDOWN/OE}}$ pin LOW as the serial interface logic uses static components and is completely self-timed. The part will not meet the I_{DD5} current limit with transitioning inputs.

Memory Bitmap Definitions

Clk{A-D}_Div[6:0]

Each of the four main output clocks (CLKA–CLKD) features a 7-bit linear output divider. Any divider setting may be used between 1 and 127 by programming the value of the desired divider into this register. Odd divide values are automatically duty-cycle corrected. Setting a divide value of zero powers down the divider and forces the output to a three-state condition.

CLKA and CLKB have two divider registers, selected by the DivSel bit (which in turn is selected by S2, S1, and S0). This allows dynamic changing of the output divider value. For the CY22394 device, ClkD_Div = 000001.

ClkE_Div[1:0]

CLKE has a simpler divider. For the CY22394, set ClkE_Div = 01.

ClkE_Div[1:0]	ClkE Output
00	Off
01	PLL1 0° Phase/4
10	PLL1 0° Phase/2
11	PLL1 0° Phase/3

Clk*_FS[2:0]

Each of the four main output clocks (CLKA–CLKD) has a three-bit code that determines the clock sources for the output divider. The available clock sources are: Reference, PLL1, PLL2, and PLL3. Each PLL provides both positive and negative phased outputs, for a total of seven clock sources. Note that the phase is a relative measure of the PLL output phases. No absolute phase relation exists at the outputs.

Clk*_FS[2:0]	Clock Source
000	Reference Clock
001	Reserved
010	PLL1 0° Phase
011	PLL1 180° Phase
100	PLL2 0° Phase
101	PLL2 180° Phase
110	PLL3 0° Phase
111	PLL3 180° Phase

Xbuf_OE

This bit enables the XBUF output when HIGH. For the CY22395, Xbuf_OE = 0.

PdnEn

This bit selects the function of the SHUTDOWN/OE pin. When this bit is HIGH, the pin is an active LOW shutdown control. When this bit is LOW, this pin is an active HIGH output enable control.

Clk*_ACAdj[1:0]

These bits modify the output predrivers, changing the duty cycle through the pads. These are nominally set to 01, with a higher value shifting the duty cycle higher. The performance of the nominal setting is guaranteed.

Clk*_DCAdj[1:0]

These bits modify the DC drive of the outputs. The performance of the nominal setting is guaranteed.

Clk*_DCAdj[1:0]	Output Drive Strength
00	–30% of nominal
01	Nominal
10	+15% of nominal
11	+50% of nominal

PLL*_Q[7:0]

PLL*_P[9:0]

PLL*_P0

These are the 8-bit Q value and 11-bit P values that determine the PLL frequency. The formula is:

$$F_{PLL} = F_{REF} \times \left(\frac{P_T}{Q_T} \right)$$

$$P_T = (2 \times (P + 3)) + P_0$$

$$Q_T = Q + 2$$

PLL*_LF[2:0]

These bits adjust the loop filter to optimize the stability of the PLL. The following table can be used to guarantee stability. However, CyClocksRT uses a more complicated algorithm to set the loop filter for enhanced jitter performance. It is recommended to use the Print Preview function in CyClocksRT to determine the charge pump settings for optimal jitter performance.

PLL*_LF[2:0]	P _T Min	P _T Max
000	16	231
001	232	626
010	627	834
011	835	1043
100	1044	1600

PLL*_En

This bit enables the PLL when HIGH. If PLL2 or PLL3 are not enabled, then any output selecting the disabled PLL must have a divider setting of zero (off). Since the PLL1_En bit is dynamic, internal logic automatically turns off dependent outputs when PLL1_En goes LOW.

DivSel

This bit controls which register is used for the CLKA and CLKB dividers.



OscCap[5:0]

This controls the internal capacitive load of the oscillator. The approximate effective crystal load capacitance is:

$$C_{LOAD} = 6pF + (OscCap \times 0.375pF)$$

Set to zero for external reference clock.

OscDrv[1:0]

These bits control the crystal oscillator gain setting. These should always be set according to the following table. The parameters are the Crystal Frequency, Internal Crystal Parasitic Resistance (available from the manufacturer), and the OscCap setting during crystal start-up (which occurs when power is applied, or after shutdown is released). If in doubt, use the next higher setting.

OscCap Crystal Freq\ R	00H–20H		20H–30H		30H–40H	
	30Ω	60Ω	30Ω	60Ω	30Ω	60Ω
8–15 MHz	00	01	01	10	01	10
15–20 MHz	01	10	01	10	10	10
20–25 MHz	01	10	10	10	10	11
25–30 MHz	10	10	10	11	11	NA

For external reference, the following table must be used.

External Freq (MHz)	1–25	25–50	50–90	90–166
OscDrv[1:0]	00	01	10	11

Reserved

These bits must be programmed LOW for proper operation of the device.

Serial Programming Bitmaps — Summary Tables

Addr	DivSel	b7	b6	b5	b4	b3	b2	b1	b0	
08H	0	ClkA_FS[0]	ClkA_Div[6:0]							
09H	1	ClkA_FS[0]	ClkA_Div[6:0]							
0AH	0	ClkB_FS[0]	ClkB_Div[6:0]							
0BH	1	ClkB_FS[0]	ClkB_Div[6:0]							
0CH	–	ClkC_FS[0]	ClkC_Div[6:0]							
0DH	–	ClkD_FS[0]	ClkD_Div[6:0]							
0EH	–	ClkD_FS[2:1]	ClkC_FS[2:1]	ClkB_FS[2:1]		ClkA_FS[2:1]				
0FH	–	Clk{C,X}_ACAdj[1:0]	Clk{A,B,D,E}_ACAdj[1:0]	PdnEn	Xbuf_OE	ClkE_Div[1:0]				
10H	–	ClkX_DCAdj[1]	Clk{D,E}_DCAdj[1]	ClkC_DCAdj[1]		Clk{A,B}_DCAdj[1]				
11H	–	PLL2_Q[7:0]								
12H	–	PLL2_P[7:0]								
13H	–	Reserved	PLL2_En	PLL2_LF[2:0]		PLL2_PO	PLL2_P[9:8]			
14H	–	PLL3_Q[7:0]								
15H	–	PLL3_P[7:0]								
16H	–	Reserved	PLL3_En	PLL3_LF[2:0]		PLL3_PO	PLL3_P[9:8]			
17H	–	Osc_Cap[5:0]						Osc_Drv[1:0]		

Addr	S2 (1,0)	b7	b6	b5	b4	b3	b2	b1	b0
40H	000	PLL1_Q[7:0]							
41H		PLL1_P[7:0]							
42H		DivSel	PLL1_En	PLL1_LF[2:0]		PLL1_PO	PLL1_P[9:8]		
43H	001	PLL1_Q[7:0]							
44H		PLL1_P[7:0]							
45H		DivSel	PLL1_En	PLL1_LF[2:0]		PLL1_PO	PLL1_P[9:8]		
46H	010	PLL1_Q[7:0]							
47H		PLL1_P[7:0]							
48H		DivSel	PLL1_En	PLL1_LF[2:0]		PLL1_PO	PLL1_P[9:8]		
49H	011	PLL1_Q[7:0]							
4AH		PLL1_P[7:0]							
4BH		DivSel	PLL1_En	PLL1_LF[2:0]		PLL1_PO	PLL1_P[9:8]		



Addr	S2 (1,0)	b7	b6	b5	b4	b3	b2	b1	b0
4CH	100	PLL1_Q[7:0]							
4DH		PLL1_P[7:0]							
4EH		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
4FH	101	PLL1_Q[7:0]							
50H		PLL1_P[7:0]							
51H		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
52H	110	PLL1_Q[7:0]							
53H		PLL1_P[7:0]							
54H		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
55H	111	PLL1_Q[7:0]							
56H		PLL1_P[7:0]							
57H		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	

Serial Programming Interface (SPI) Protocol and Timing

The CY22393, CY22394 and CY22395 utilizes a 2-serial-wire interface SDAT and SCLK that operates up to 400 kbits/sec in Read or Write mode. The basic Write serial format is as follows:

Start Bit; 7-bit Device Address (DA); $\overline{R/W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; etc. until STOP Bit. The basic serial format is illustrated in *Figure 2*.

Default Startup Condition for the CY22393/94/95

The default (programmed) condition of each device is generally set by the distributor, who will program the device using a customer-specified JEDEC file produced by CyClocksRT, Cypress's proprietary development software. Parts shipped by the factory are blank and unprogrammed. In this condition, all bits are set to 0, all outputs are three-stated, and the crystal oscillator circuit is active.

While users can develop their own subroutine to program any or all of the individual registers as described in the following pages, it may be easier to simply use CyClocksRT to produce the required register setting file.

Device Address

The device address is a 7-bit value that is configured during Field Programming. By programming different device addresses, two or more parts can be connected to the serial interface and be independently controlled. The device address is combined with a read/write bit as the LSB and is sent after each start bit.

The default serial interface address is 69H, but should there be a conflict with any other devices in your system, this can also be changed using CyClocksRT.

Data Valid

Data is valid when the clock is HIGH, and may only be transitioned when the clock is LOW as illustrated in *Figure 3*.

Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in *Figure 4*.

Start Sequence - Start Frame is indicated by SDAT going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (seven bits) and a $\overline{R/W}$ bit, followed by register address (eight bits) and register data (eight bits).

Stop Sequence - Stop Frame is indicated by SDAT going HIGH when SCLK is HIGH. A Stop Frame frees the bus for writing to another part on the same bus or writing to another random register address.

Acknowledge Pulse

During Write Mode the CY22393, CY22394 and CY22395 will respond with an Acknowledge pulse after every eight bits. This is accomplished by pulling the SDAT line LOW during the Nth clock cycle as illustrated in *Figure 5*. (N = the number of bytes transmitted). During Read Mode the acknowledge pulse after the data packet is sent is generated by the master.

Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (ack = 0/LOW). The next eight bits must contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (ack = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

In order to write more than one byte at a time, the master does not end the write sequence with a stop condition. Instead, the master can send multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, just like after the first byte, and will accept data until the acknowledge bit is responded to by the STOP condition. When receiving multiple bytes, the CY22393, CY22394, and CY22395 internally increments the register address.

Read Operations

Read operations are initiated the same way as Write operations except that the R/W bit of the slave address is set to '1' (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY22393, CY22394 and CY22395 has an onboard address counter that retains 1 more than the address of the last word access. If the last word written or read was word 'n', then a current address read operation would return the value stored in location 'n+1'. When the CY22393, CY22394 and CY22395 receives the slave address with the R/W bit set to a '1', the CY22393, CY22394 and CY22395 issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition, which causes the CY22393, CY22394 and CY22395 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first the word address must be set. This is accomplished by sending the address to the CY22393, CY22394 and CY22395 as part of a write operation. After the word address is sent, the

master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next the master reissues the control byte with the R/W byte set to '1'. The CY22393, CY22394 and CY22395 then issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition which causes the CY22393, CY22394 and CY22395 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action results in an incrementing of the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master may serially read the entire contents of the slave device memory. Note that register addresses outside of 08H to 1BH and 40H to 57H can be read from but are not real registers and do not contain configuration information. When the internal address pointer points to the FFH register, after the next increment, the pointer will point to the 00H register.

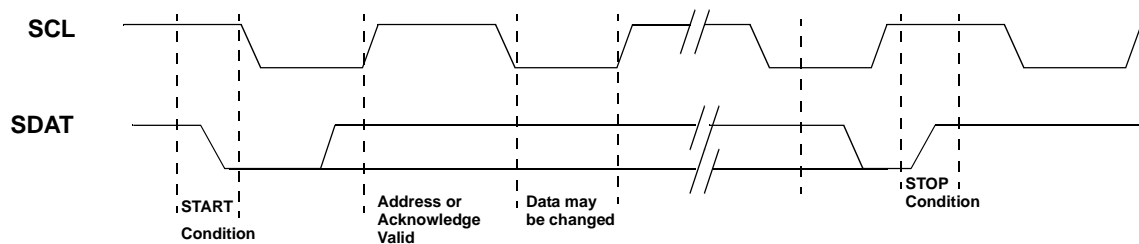


Figure 1. Data Transfer Sequence on the Serial Bus

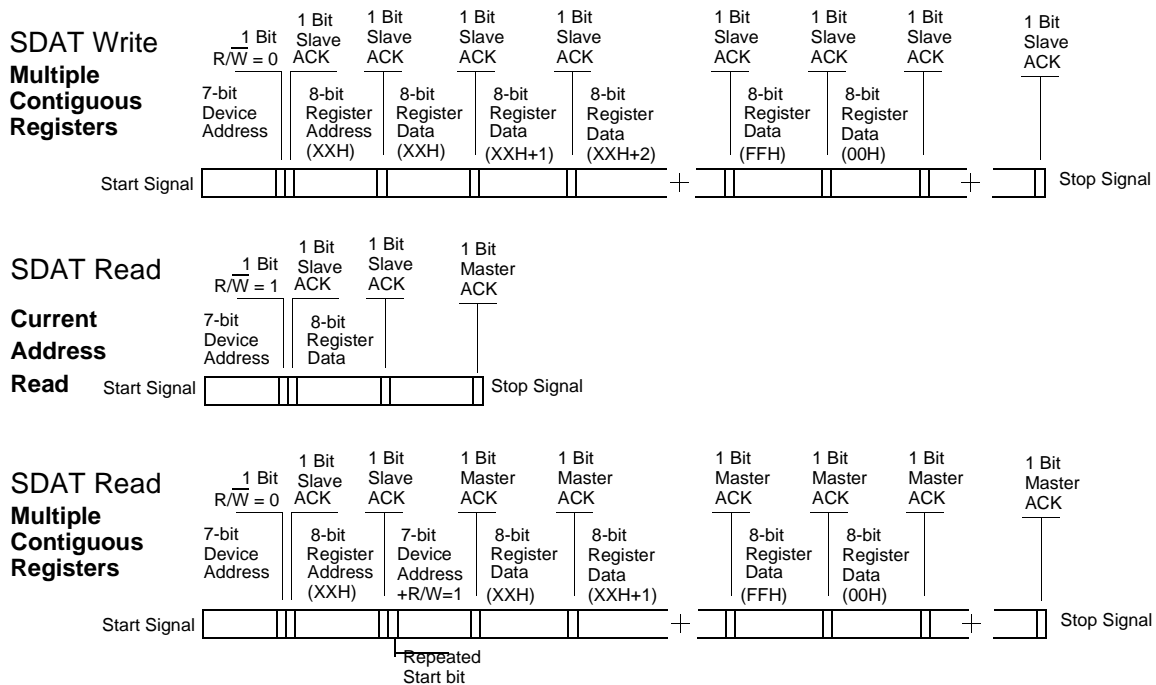


Figure 2. Data Frame Architecture

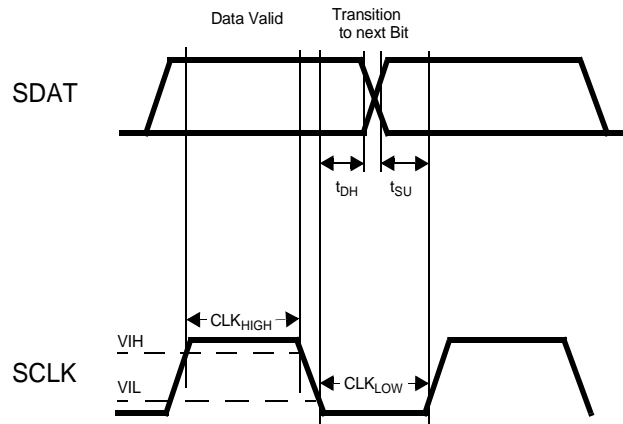


Figure 3. Data Valid and Data Transition Periods

Serial Programming Interface Timing

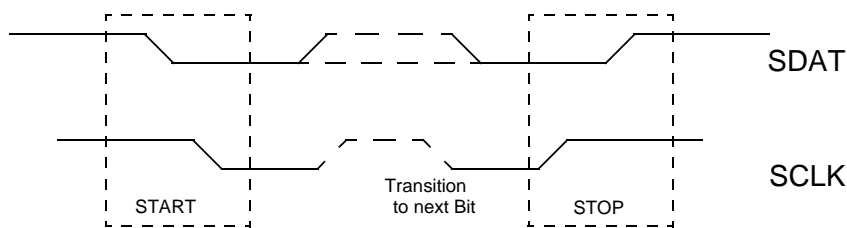


Figure 4. Start and Stop Frame

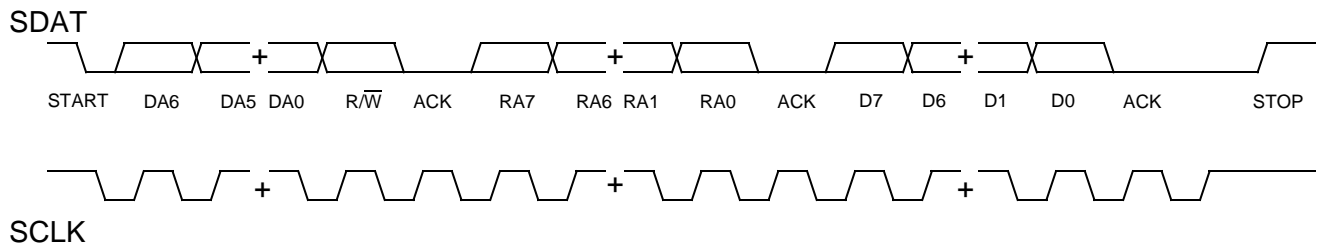


Figure 5. Frame Format (Device Address, $\overline{R/W}$, Register Address, Register Data)

Serial Programming Interface Timing Specifications

Parameter	Description	Min.	Max.	Unit
f_{SCLK}	Frequency of SCLK		400	kHz
	Start mode time from SDA LOW to SCL LOW	0.6		μ s
CLK_{LOW}	SCLK LOW period	1.3		μ s
CLK_{HIGH}	SCLK HIGH period	0.6		μ s
t_{SU}	Data transition to SCLK HIGH	100		ns
t_{DH}	Data hold (SCLK LOW to data transition)	0		ns
	Rise time of SCLK and SDAT		300	ns
	Fall time of SCLK and SDAT		300	ns
	Stop mode time from SCLK HIGH to SDAT HIGH	0.6		μ s
	Stop mode to Start mode	1.3		μ s



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5V to +7.0V
DC Input Voltage -0.5V to + (AV_{DD} + 0.5V)
Storage Temperature -65°C to +125°C

Junction Temperature 125°C
Data Retention @ T_j=125°C > 10 years
Maximum Programming Cycles 100
Package Power Dissipation 350 mW
Static Discharge Voltage
(per MIL-STD-883, Method 3015) ≥ 2000V
Latch up (per JEDEC 17) ≥ ±200 mA

Operating Conditions^[2]

Parameter	Description	Part Numbers	Min.	Typ	Max.	Unit
V _{DD} /AV _{DD} /LV _{DD}	Supply Voltage	All	3.135	3.3	3.465	V
LV _{DD}	2.5V Output Supply Voltage	22395	2.375	2.5	2.625	V
T _A	Commercial Operating Temperature, Ambient	All	0		+70	°C
	Industrial Operating Temperature, Ambient	All	-40		+85	°C
C _{LOAD_OUT}	Max. Load Capacitance	All			15	pF
f _{REF}	External Reference Crystal	All	8		30	MHz
	External Reference Clock, ^[3] Commercial	All	1		166	MHz
	External Reference Clock, ^[3] Industrial	All	1		150	MHz

3.3V Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{OH}	Output High Current ^[4]	V _{OH} = (L)V _{DD} - 0.5, (L)V _{DD} = 3.3V	12	24		mA
I _{OL}	Output Low Current ^[4]	V _{OL} = 0.5, (L)V _{DD} = 3.3V	12	24		mA
C _{XTAL_MIN}	Crystal Load Capacitance ^[4]	Capload at minimum setting		6		pF
C _{XTAL_MAX}	Crystal Load Capacitance ^[3]	Capload at maximum setting		30		pF
C _{IN}	Input Pin Capacitance ^[4]	Except crystal pins		7		pF
V _{IH}	HIGH-Level Input Voltage	CMOS levels, % of AV _{DD}	70%			AV _{DD}
V _{IL}	LOW-Level Input Voltage	CMOS levels, % of AV _{DD}			30%	AV _{DD}
I _{IH}	Input HIGH Current	V _{IN} = AV _{DD} - 0.3 V		<1	10	μA
I _{IL}	Input LOW Current	V _{IN} = +0.3 V		<1	10	μA
I _{OZ}	Output Leakage Current	Three-state outputs			10	μA
I _{DD}	Total Power Supply Current	3.3V Power Supply; 2 outputs @ 20 MHz; 4 outputs @ 40 MHz		50		mA
		3.3V Power Supply; 2 outputs @ 166 MHz; 4 outputs @ 83 MHz		100		mA
I _{DDS}	Total Power Supply Current in Shutdown Mode	Shutdown active		5	20	μA

2.5V Electrical Characteristics (CY22395 only)^[5]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{OH_2.5}	Output High Current ^[4]	V _{OH} = LV _{DD} - 0.5, LV _{DD} = 2.5 V	8	16		mA
I _{OL_2.5}	Output Low Current ^[4]	V _{OL} = 0.5, LV _{DD} = 2.5 V	8	16		mA

Notes:

- Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
- External input reference clock must have a duty cycle between 40% and 60%, measured at V_{DD}/2.
- Guaranteed by design, not 100% tested.
- V_{DDL} is only specified and characterized at 3.3V ± 5% and 2.5V ± 5%. V_{DDL} may be powered at any value between 3.465 and 2.375.

3.3V Switching Characteristics

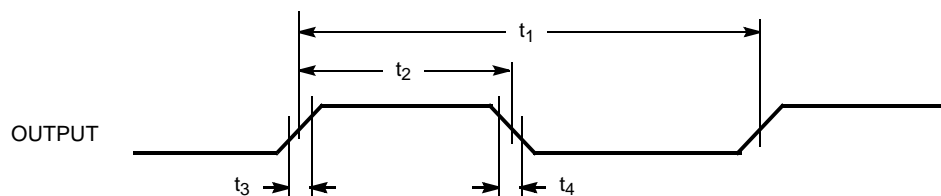
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
1/t ₁	Output Frequency ^[4, 6]	Clock output limit, CMOS, Commercial			200	MHz
		Clock output limit, CMOS, Industrial			166	MHz
		Clock output limit, PECL, Commercial (CY22394 only)	100		400	MHz
		Clock output limit, PECL, Industrial (CY22394 only)	125		375	MHz
t ₂	Output Duty Cycle ^[4, 7]	Duty cycle for outputs, defined as $t_2 \div t_1$, F _{out} <100 MHz, divider>=2, measured at V _{DD} /2	45%	50%	55%	
		Duty cycle for outputs, defined as $t_2 \div t_1$, F _{out} >100 MHz or divider = 1, measured at V _{DD} /2	40%	50%	60%	
t ₃	Rising Edge Slew Rate ^[4]	Output clock rise time, 20% to 80% of V _{DD}	0.75	1.4		V/ns
t ₄	Falling Edge Slew Rate ^[4]	Output clock fall time, 20% to 80% of V _{DD}	0.75	1.4		V/ns
t ₅	Output three-state Timing ^[4]	Time for output to enter or leave three-state mode after SHUTDOWN/OE switches		150	300	ns
t ₆	Clock Jitter ^[4, 8]	Peak-to-peak period jitter, CLK outputs measured at V _{DD} /2		400		ps
V ₇	P+/P- Crossing Point ^[4]	Crossing point referenced to V _{DD} /2, balanced resistor network (CY22394 only)	-0.2	0	0.2	V
t ₈	P+/P- Jitter ^[4, 8]	Peak-to-peak period jitter, P+/P- outputs measured at crossing point (CY22394 only)		200		ps
t ₉	Lock Time ^[4]	PLL Lock Time from Power-up		1.0	3	ms

2.5V Switching Characteristics (CY22395 only)^[5]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
1/t _{1_2.5}	Output Frequency ^[4, 6]	Clock output limit, LVCMOS			133	MHz
t _{2_2.5}	Output Duty Cycle ^[4, 7]	Duty cycle for outputs, defined as $t_2 \div t_1$ measured at LV _{DD} /2	40%	50%	60%	
t _{3_2.5}	Rising Edge Slew Rate ^[4]	Output clock rise time, 20% to 80% of LV _{DD}	0.5	1.0		V/ns
t _{4_2.5}	Falling Edge Slew Rate ^[4]	Output clock fall time, 20% to 80% of LV _{DD}	0.5	1.0		V/ns

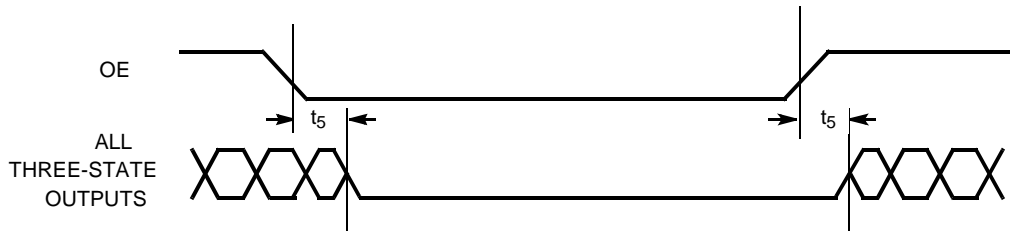
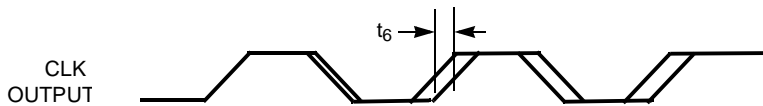
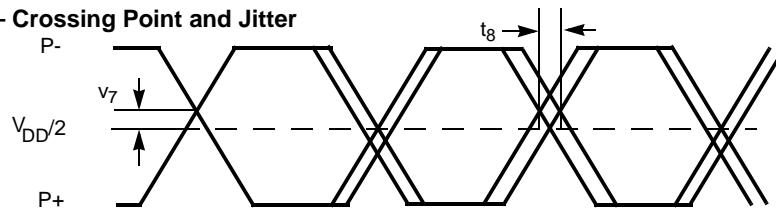
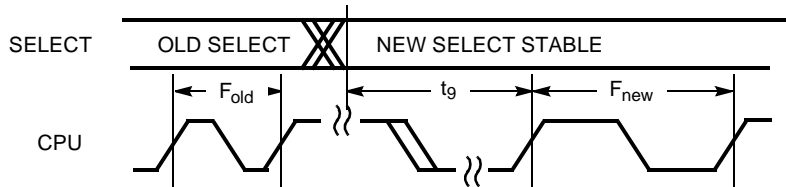
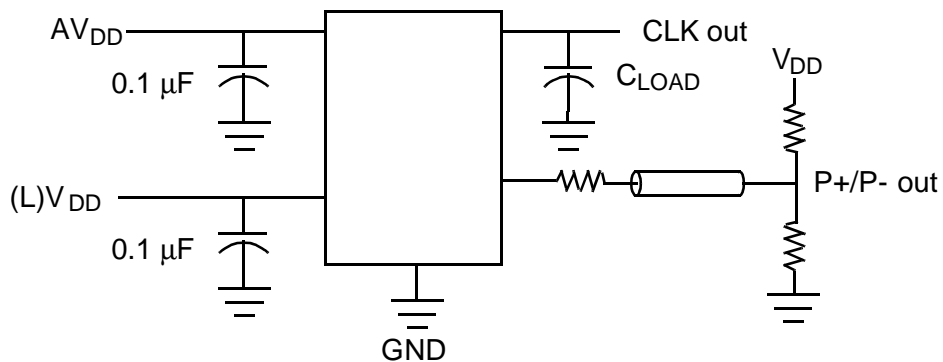
Switching Waveforms

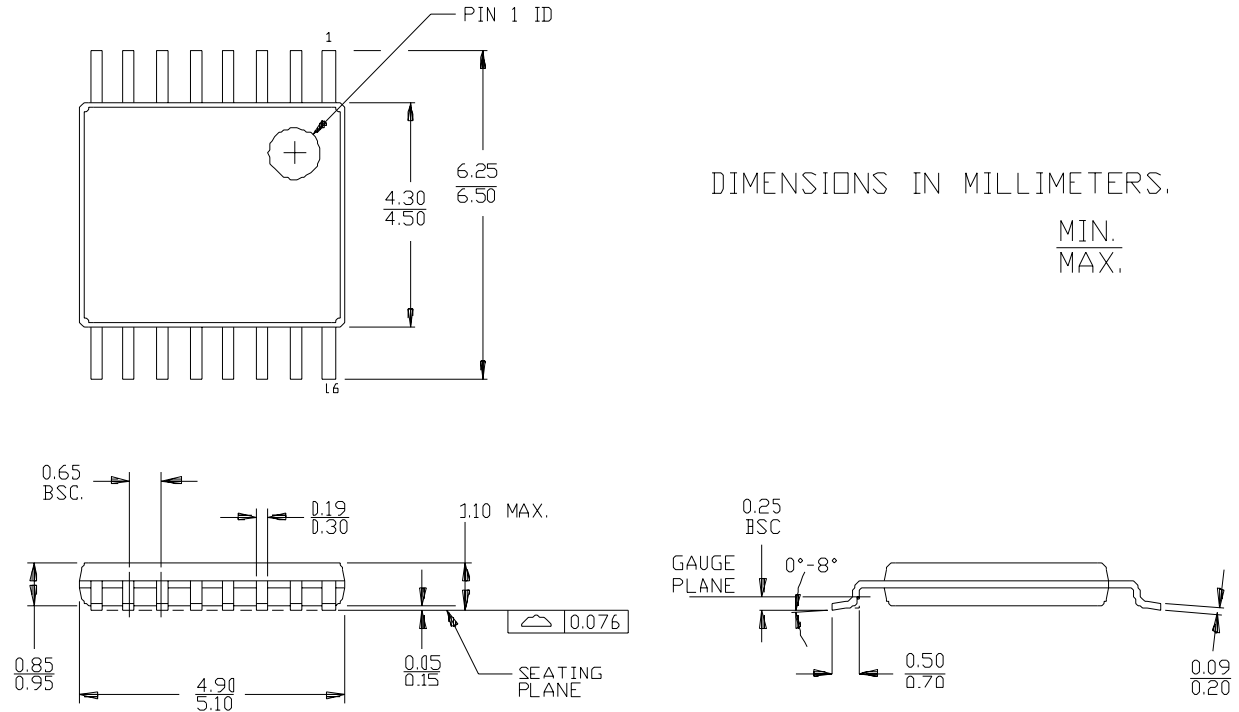
All Outputs, Duty Cycle and Rise/Fall Time



Notes:

6. Guaranteed to meet 20%–80% output thresholds, duty cycle, and crossing point specifications.
7. Reference Output duty cycle depends on XTALIN duty cycle.
8. Jitter varies significantly with configuration. Reference Output jitter depends on XTALIN jitter and edge rate.

Output Three State Timing

CLK Output Jitter

P+/P- Crossing Point and Jitter

CPU Frequency Change

Test Circuit


Package Diagram
16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16


51-85091-**

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Document History Page

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Document Number: 38-07186

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111984	12/09/01	DSG	Change from Spec number: 38-01144 to 38-07186
*A	129388	10/13/03	RGL	Added timing information