Using Esterel-C to Model and Verify the PIC16F84 Microcontroller

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In the present day and age, reactive embedded systems with real-time requirements are extensively used. Given the mission-critical nature of such systems, highlevel abstraction and formal (software-based) modeling has become an integral part of the design process of embedded systems. Formal models of hardware allow us to rigorously verify the behavior of the hardware under all possible inputs, thus ensuring that the final product is error-free. In addition, since most such models are deterministic, the verification process can be automated.

Any form of formal model of hardware must have "precise mathematical a specification" [ELLS99]. This enables the model to be verified using guaranteed tools. To allow such a mathematically precise specification, a language such as Esterel (or Esterel-C) is useful. The synchronous nature of Esterel combined with the time-triggered nature of most hardware (such as microcontrollers) ensures that models specified in Esterel completely are

deterministic [Gu99] and thus mathematically precise. In addition, the Esterel compiler allows us to generate finite state automata representations of the model, which can be used to automate the verification process.

The aim of this project is to create a formal model for the PIC16F84 microcontroller using the synchronous, eventdriven Esterel-C language and perform rigorous and automated verification of that model. The first step in the modeling process will be to decompose the hardware design of the PIC16F84 into functionally independent modules (coded in Esterel). Deciding the reactive behavior of each one of these modules will be the next step. Finally, we will have to model the interactions between the modules and represent this modular structure in Esterel-C. Once we have the software model in place, we have to translate the model into a finite state automaton and perform the verification of the model using a tool such as Xeve (a verification package for Esterel).

Works Cited

[ELLS97] S. Edwards, L. Lavagno, E. A. Lee, and A. Sangiovanni-Vincentelli. Design of Embedded Systems: Formal Models, Validation, and Synthesis. In Proceedings of the IEEE, 1997

- [Gu99] Micheal Gunzert. Building Safety-Critical Real-Time Systems with Sychronous Software Components. Technical Report, Institute of Industrial Automation and Software Engineering (IAS), 1999.
- [MSS99] Christian Siemers, Dietmar P. F. Moller, Sybille Siemers. Modelling and Simulation of a New Combined Blockoriented Microarchitecture Model for Controllers in Responsive Systems. In *Proceedings of the Conference of the United Kingdom Simulation Society UKSIM'99*, 1999.