NAME

cec − The Columbia Esterel Compiler

SYNOPSIS

cec [**−−pdg** | **−−lists** | **−−lists-goto** | **−−vm** | **−−blif** | **−−verilog** | **−−sm**] [*options...*] *file***.strl**

cec [**−−blif** | **−−verilog**] [*options...*] *file***.sm**

cec −−vm-only

DESCRIPTION

The **cec** command invokes the compiler, translating Esterel source code (suffix **.strl**) into either a C program or a circuit representation in either the BLIF format accepted by the **sis**(1) logic optimizer from Berkeley or the Verilog language. In the most basic form,

cec myfile.strl

compiles the Esterel source file **myfile.strl** into the C file **myfile.c**. A gate-level logic circuit, in the form of a BLIF file named **myfile.blif** can be generated by providing an option:

cec −−blif myfile.strl

Similarly, a Verilog file named **myfile.v** may also be generated:

cec −−verilog myfile.strl

In circuit-generation mode, all local state machines are given a default encoding that can be manually overriden by supplying a **.sm** file. This is done by asking **cec** to generate an **.sm** file, editing it, then asking **cec** to finish its job, e.g.,

cec −−sm myfile.strl

Edit the file **myfile.sm**

cec −−blif myfile.sm

This generates a **.blif** file. Verilog may also be generated:

cec −−verilog myfile.sm

OPTIONS

Output language options

−−pdg Generate a **.c** file generated with program dependence graphs. This is the default.

−−lists Generate a **.c** file generated with dynamic lists. This is generally less efficient than the **−−pdg** option, although it may be superior on very parallel programs.

−−lists-goto
Generate a **.c** file generated with dynamic lists that uses GCC's computed-goto extension. The generated code may be slightly faster than **−−lists-goto** option, but is less portable.

−−vm Generate a **.c** file built around a virtual machine. The generated code is generally much slower, but much smaller than that from the other C code generators.

−−blif Generate a **.blif** file as output.

−−verilog
Generate a **.v** (Verilog) file as output.

−−sm Generate a **.sm** (state machine) file as output. This file may be edited and later resupplied to **cec** to complete the compilation process and produce either Verilog or BLIF.

−−vm-only
Print source for the virtual machine (in C) to standard out. This is not necessary to compile the **.c** file generated by the **−−vm** option as that file automatically includes the output of this option.

Circuit-generation options

−−sis Invoke the **sis**(1) logic synthesis system as part of the compilation process. By default, this runs the standard **script.rugged** optimization script, but this may be changed using the following option.

−−sis−script *script*
Specify the script invoked by **sis**(1) during optimization. This implies **−−sis**

−−pdgblifargs *args*
Specify additional arguments to be passed directly to the **pdgblif** pass. Useful mostly to developers.

−s Do not do the usual schziophrenic expansion. This experimental option may cause your program to fail. Not recommended.

Output control options

−B *basename*
Specify the basename of generated files. This normally defaults to the basename of the given **.strl** file, but may be specified explicitly using this option.

−D *directory*
Specify the destination directory for generated files. This defaults to the current working directory.

−K Keep all intermediate files; by default all are deleted after compilation is complete. Most are in XML format. This is useful mostly to developers.

−−keep *extension*
Keep the intermediate file with the given extension. Invoking **cec −−keep** alone lists the possible extensions. Multiple **−−keep** directives may be issued.

Miscellaneous options

−h

−−help Print a usage summary.

−−version
Print the version of the compiler.

−v

−−verbose
Enable verbose mode. Report each internal command as it is executed.

−−logfile *file*
Generate a log file with the given name. This contains version information, the command line that invoked the compiler, and the list of commands invoked during the compilation process.

−−eachcmd *cmd*
Specify a command to precede each command invoked by the compiler. For example, **−−eachcmd time** times each internally-executed command. Useful mostly to developers.

BUGS

Cec does not support certain parts of the Esterel V5 language, including the *pre* operator and tasks. In addition, circuit generation mode does not support variables, external types, functions, and procedures.

The generated circuit can always be improved.

The virtual machine has substantial limitations (e.g., 256 registers) that prevent it from being used for large programs.

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SEE ALSO

<http://www.cs.columbia.edu/~sedwards/>

The CMA/INRIA Esterel V5 compiler, available from <http://www.esterel−techologies.com/>

The Esterel V5 Language Primer

Gerard Berry, *The Constructive Semantics of Esterel*

The Icarus Verilog simulator/synthesizer <http://www.icarus.com/eda/verilog/>

The **sis**(1) logic synthesis system.