Christian Pilato

Postdoctoral Researcher

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Personal Information

- Born on December 28th, 1982 in Busto Arsizio (VA), Italy

Education

- **Ph.D. in Information Technology** at Politecnico di Milano   February 2011
  Thesis Title: *Design Methodologies for Improving Embedded Systems with Hardware Accelerators*
  Advisor: *Fabrizio Ferrandi* – Supervisor: *Donatella Sciuto*
- **M.Sc. in Computer Science Engineering** at Politecnico di Milano   April 2007
  Thesis title: *High Level Synthesis with Area Constraints for FPGA Designs: An Evolutionary Approach*
  Advisor: *Fabrizio Ferrandi* – Grade: 110/110
- **B.Sc. in Computer Science Engineering** at Politecnico di Milano   October 2004
  Thesis title: *Progetto in Linguaggio VHDL di un Processore di Segnale Audio Digitale per FPGA*
  Advisor: *Fabrizio Ferrandi* – Grade: 102/110

Research Experience

- **Postdoctoral Researcher**   *Jun. 2016 – current*
  Faculty of Informatics, Università della Svizzera italiana (USI), Lugano, Switzerland
  Supervisor: Francesco Regazzoni
  - Design methodologies for security-aware high-level synthesis, security metrics for cyber-physical systems.
- **Visiting Research Scientist**   *Sept. 2016 – Jan. 2017*
  Department of Microelectronics, Delft University of Technology, Delft, The Netherlands
  Supervisor: Edoardo Charbon
  - Design of FPGA controllers for SPAD chips.
- **Postdoc Research Scientist**   *Sept. 2013 – May 2016*
  Department of Computer Science, Columbia University, New York, NY, USA
  Supervisor: Luca Carloni
  - Design and integration of hardware accelerators for heterogeneous architectures (including FPGA prototypes, CPU-FPGA platforms, and SoCs), with emphasis on memory-related aspects.
- **Postdoc Research Assistant**   *Jun. 2011 – Sept. 2013*
  Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy
  Supervisor: Donatella Sciuto
  - Hardware-software methodologies for the design of partially reconfigurable architectures; high-level synthesis methods for memory-intensive applications; profiling techniques to support automatic parallelization.
- **Visiting Researcher**   *Sept. 2012 – Dec. 2012*
  Department of Computer Science, Chalmers University of Technology, Gothenburg, Sweden
  Supervisor: Georgi Gaydadjiev
  - Integration of polymorphic register files for high-performance dataflow computing.
- **Visiting Researcher**   *Dec. 2009 – May 2010*
  Nangate A/S, Herlev, Denmark
  Supervisor: Martin Elhøj
  - Design of application-specific standard-cell libraries to improve circuit manufacturing.
- **Research Assistant**   *Jun. 2007 – Dec. 2007*
  Dipartimento di Elettronica ed Informazione, Politecnico di Milano, Italy
  Supervisor: Donatella Sciuto
  - Development of hardware-software co-design methods for heterogeneous architectures.

Awards and Honors

- Collaboration grant (5K€) by HiPEAC European Network of Excellence for the research "Adaptive and heterogeneous computing systems" with Chalmers University of Technology, Gothenburg, Sweden (2012)
- Technology Transfer Award by HiPEAC European Network of Excellence (2012)
- Ph.D. fully funded by a scholarship of STMicroelectronics (2008–2010)

Selected publications

Referred Journal Publications

1. **C. Pilato**, S. Garg, K. Wu, R. Karri, F. Regazzoni. "Securing Hardware Accelerators: a New Challenge for High-Level Synthesis," in *IEEE Embedded Systems Letter*, (*to appear*), 2017.

   [doi: http://dx.doi.org/10.1109/LES.2017.2774800]

2. C. Ciobanu, **C. Pilato**, G. Gaydadjiev, D. Sciuto. "The Case for Polymorphic Registers in Dataflow Computing," in *International Journal of Parallel Programming*, (to appear), 2017.

   [doi: http://dx.doi.org/10.1007/s10766-017-0494-1]

3. **C. Pilato**, P. Mantovani, G. Di Guglielmo, L.P. Carloni, "System-Level Optimization of Accelerator Local Memory for Heterogeneous Systems-on-Chip," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 3, pp. 435–448, March 2017.

   [doi: http://dx.doi.org/10.1109/TCAD.2016.2611506]

4. R. Nane, V.-M. Sima, **C. Pilato**, J. Choi, B. Fort, A. Canis, Y.T. Chen, H. Hsiao, S. Brown, F, Ferrandi, J. Anderson, K. Bertels. "A Survey and Evaluation of FPGA High-Level Synthesis Tools," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 10, pp. 1591-1604, October 2016 (impact factor: 1.003).

   [doi: http://dx.doi.org/10.1109/TCAD.2015.2513673]

5. M. Lattuada, **C. Pilato**, F. Ferrandi. "Performance Estimation of Task Graphs based on Path Profiling," in *International Journal of Parallel Programming*, vol. 44, no. 4, pp. 735-771, August 2016 (impact factor: 0.491).

   [doi: http://dx.doi.org/10.1007/s10766-015-0372-7]

6. K. Bertels, V.M. Sima, Y. Yankova, G. Kuzmanov, W. Luk, J.G.F. Coutinho, F. Ferrandi, **C. Pilato**, M. Lattuada, D. Sciuto, A. Michelotti, "hArtes: Hardware-Software Codesign for Heterogeneous Multicore Platforms," in *IEEE Micro*, vol. 30, no. 5, (2010), pp. 88-97 (ISSN: 0272-1732) (impact factor: 1.812).

   [doi: http://dx.doi.org/10.1109/MM.2010.91]

7. F. Ferrandi, P.L. Lanzi, **C. Pilato**, D. Sciuto, A. Tumeo, "Ant Colony Heuristic for Mapping and Scheduling Task and Communications on Heterogeneous Embedded Systems," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 6, (2010), pp. 911-924 (ISSN: 0278-0070) (impact factor: 1.252).

   [doi: http://dx.doi.org/10.1109/TCAD.2010.2048354]

8. **C. Pilato**, A. Tumeo, G. Palermo, F. Ferrandi, P.L. Lanzi, D. Sciuto, "Improving Evolutionary Exploration to Area-Time Optimization of FPGA Designs," in *Journal of Systems Architecture*, vol. 54, no. 11, (2008), pp. 1046-1057 (ISSN: 1383-7621) (impact factor: 0.440).

   [doi: http://dx.doi.org/10.1016/j.sysarc.2008.04.010]

Referred Conference Publications

1. P. Mantovani, E. Cota, **C. Pilato**, G. Di Guglielmo, L.P. Carloni, "Handling Large Data Sets for High-Performance Embedded Applications in Heterogeneous Systems-on-Chip," in *Proceedings of ACM/IEEE International Conference on Compilers, Architectures and Synthesis For Embedded Systems* (CASES 2016), Pittsburgh, PA, USA, October 2-7, 2016, pp. 1-10.

   [doi: http://doi.acm.org/10.1145/2968455.2968509]

2. P. Mantovani, E. Cota, K. Tien, **C. Pilato**, G. Di Guglielmo, K. Shepard, L.P. Carloni, "An FPGA-Based Infrastructure for Fine-Grained DVFS Analysis in High-Performance Embedded Systems," in *Proceedings of ACM/IEEE Design Automation Conference* (DAC 2016), Austin, TX, USA, June 5-9, 2016, pp. 1-6.

   [doi: http://doi.acm.org/10.1145/2897937.2897984]

3. G. Di Guglielmo, **C. Pilato**, L.P. Carloni, "A Design Methodology for Compositional High-Level Synthesis of Communication-Centric SoCs," in *Proc. of ACM/IEEE Design Automation Conf.* (DAC 2014), San Francisco, CA, USA, June 1-5, 2014, pp. 1-6.

   [doi: http://doi.acm.org/10.1145/2593069.2593071]

4. **C. Pilato**, F. Ferrandi, D. Sciuto, "A Design Methodology to Implement Memory Accesses in High-Level Synthesis," in *Proceedings of ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis* (CODES+ISSS 2011), Taipei, Taiwan, October 9-14, 2011, pp. 49-58.

   [doi: http://dx.doi.org/10.1145/2039370.2039381]

Positions of Trust

Dr. Pilato is leading the following grant proposals:

- *MEMENTO (Programming heterogeneous applications with emerging memory technologies towards exascale computing)*, EU H2020 FETHPC PROJECT (PI funding amount: 703K€out of 3.8M€) *(under evaluation)*
  Dr. Pilato is the **Technical Coordinator** of the entire project, which includes the work of eight different partners.
- *SCORPION (Secured-by-construction platforms for the Internet of Things)*, EU ERC STARTING GRANT 2018 PROJECT (PI funding amount: 1.43M€) *(under evaluation)*
  Dr. Pilato is the **Principal Investigator** of this individual proposal, which aims at developing an open framework for the security-aware design of IoT devices.

Dr. Pilato took a prominent role in the following research project:

- *FASTER (Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration)*, EU FP7 SPECIFIC TAR-GETED RESEARCH PROJECT (STREP), CONTRACT NO. 287804
  Local project leader: Donatella Sciuto, Politecnico di Milano.
  Dr. Pilato was the **Task Leader** of "Application Task Profiling and Identification of Reconfigurable Cores", which included the work of FORTH (Greece), Chalmers University of Technology (Sweden), Imperial College (UK), Politecnico di Milano (Italy), and Ghent University (Belgium). This task defined design methodologies for reconfigurable systems, involving the concurrent definition of the architecture (i.e., feasible reconfigurable regions) and the application (i.e., corresponding hardware-software partitioning). He collaborated with the local leader and the project coordinator since the definition of the proposal, providing support for all managerial aspects.

Research Projects

He is contributing actively in the following research projects:

- DARPA CIRCUIT REALIZATION AT FASTER TIMESCALES (CRAFT) PROJECT
  Local project leaders: Siddharth Garg and Ramesh Karri, New York University (NYU), Steve Fisher (Boeing)
  Dr. Pilato is collaborating with NYU for the design of methodologies based on high-level synthesis to obfuscate digital circuits and prevent reverse engineering of chips to be fabricated.
- *CERBERO (Cross-layer modEl-based fRamework for multi-oBjective dEsign of Reconfigurable systems in unceRtain hybRid envirOnments)*, EU H2020 PROJECT, CONTRACT NO. 732105
  Local project leader: Francesco Regazzoni, Università della Svizzera italiana (USI Lugano).
  Dr. Pilato is working on performance indicators and design methodologies to incorporate security concepts into the design of reliable and adaptive cyber-physical systems. This work is mainly done in collaboration with University of Sassari, University of Cagliari, Thales Alenia Space, Centro Ricerche Fiat, and IBM Haifa.

In the past, he also contributed to the following research projects:

- *C-FAR (Center for Future Architectures Research)*, STARNET RESEARCH CENTER
  Local project leader: Luca Carloni, Columbia University.
  Dr. Pilato worked on design methodologies and CAD tools for the optimization of the accelerator local memory in heterogeneous SoCs. This also included hardware support for the allocation of massive data sets. This work promoted collaborations with the *Architecture and Design* lab at Columbia University (Martha Kim).
- *ESP (Embedded Scalable Platform)*, DARPA POWER EFFICIENCY REVOLUTION FOR EMBEDDED COMPUTING TECHNOLOGIES (PERFECT) PROJECT, CONTRACT NO. HR0011-13-C-0003
  Local project leader: Luca Carloni, Columbia University.
  Dr. Pilato provided support for the FPGA prototype of the proposed SoC architecture. His work includes the support for the integration of hardware accelerators, the exploration of multiple design implementations, and the characterization of the power consumption for the different components at each voltage-frequency pair. This work has been mainly done in collaboration with the *Bioelectronics Systems* lab at Columbia University (Ken Shepard).
- *Synaptic (SYNthesis using Advanced Process Technology Integrated in regular Cells, IPs, architectures, and design platforms)*, EU FP7 SPECIFIC TARGETED RESEARCH PROJECT (STREP), CONTRACT NO. 248538
  Local project leader: Fabrizio Ferrandi, Politecnico di Milano.

Dr. Pilato defined a heuristic methodology to automatically identify a minimal set of application-specific standard cells to extend an existing library and improve the manufacturing of digital circuits in state-of-the-art industrial flows. He also provided support through all project's phases since the definition of the proposal.

- *hArtes (Holistic Approach to Reconfigurable real Time Embedded Systems)*, EU FP6 INTEGRATED PROJECT (IP), CONTRACT NO. 035143
  Local project leader: Donatella Sciuto, Politecnico di Milano.
  Dr. Pilato was involved in the definition of compiler-based methodologies (based on GCC) for the semi-automatic parallelization of sequential C-based applications. He also proposed methodologies for defining an early hardware-software partitioning in heterogeneous architectures having limited hardware resources and multiple hardware implementations generated with the support of high-level synthesis.

Research Interests

Dr. Pilato's research focuses on innovative architectures and companion design methodologies, which can be mostly combined with existing commercial tools, for the semi-automatic parallelization of sequential algorithms, their hardware/software partitioning, the design of self-adaptive and reconfigurable architectures, and the generation and optimization of accelerator-based computing systems. The resulting combined solutions allow the acceleration of various applications (e.g., computer vision, seismic migration, machine learning, etc.) with significant energy savings. Specifically, his contributions cover the following topics.

Hardware/software co-design of application-specific systems. The design of heterogeneous SoCs requires determining how to implement computational tasks and communications, depending on a set of constraints of the application and the architecture. For this reason, he developed an integrated methodology to determine how to efficiently implement each part of the input application, either computational tasks or communications. This method effectively combines the requirements of the application and the constraints of the target architecture, spanning from the automatic generation of specialized accelerators to the system-level design. Specifically, he developed BAMBU, an open-source framework for research in *high-level synthesis* (HLS) [IC.19][IC.30] (first release in March 2012, available at http://github.com/ferrandi/PandA-bambu). It was also shown that BAMBU outperforms state-of-the-art academic HLS tools for memory-intensive applications [JR.8]. BAMBU also automatically generates multiple hardware implementations starting from the same C-based specification using a multi-objective design space exploration [JR.1]. Given a partitioned application, these multiple hardware implementations are then combined at the system level with an innovative approach based on *ant colony optimization* [JR.2]. This algorithm uses a constructive approach to generate solutions, and it thus explores more efficiently the design space, reducing the number of unfeasible solutions. In this way, it improves the application performance while respecting the constraints of the target architecture (e.g., limited hardware resources). This research has been included in hArtes, an EU-funded project (2006-2010), where Dr. Pilato worked on the compiler-based analysis of sequential applications for their semi-automatic parallelization and implementation on heterogeneous architectures [JR.3][JR.7].

High-level synthesis of high-performance accelerators. Thanks to the evolution of commercial HLS tools, Dr. Pilato raised the abstraction level of his research to design more complex SoCs for high- performance applications. So he developed EDA design flows that efficiently combine and coordinate existing tools [IC.34][JR.9]. On one hand, he worked on optimizing the communication primitives to avoid deadlock during the computation [IC.34]. On the other hand, he did extensive research on memory aspects since embedded memories are generally responsible for 70-90% of the chip area and 40-50% of the power consumption. First, he proposed an innovative memory architecture for the accelerators that can support, for the first time, almost all the software constructs usually used by software programmers [IC.17][JR.5]. Then, during his 3-month visit at Chalmers University, he worked on the generation of dedicated memory subsystems for the Maxeler platforms [IC.29]. This memory structure allowed the execution of parallel accesses with an application speedup of 40x with respect to solutions using serial memory accesses. Finally, he proposed a methodology, which is complementary to existing HLS tools, to automatically determine an efficient organization of the accelerator memory microarchitecture and minimize the memory footprint while guaranteeing the required memory bandwidth to the computational resources [JR.9]. This methodology has been embodied in MNEMOSYNE, an open-source CAD prototype (first released in January 2017, available at https://github.com/chrpilat/mnemosyne) for the generation of multi-bank memories. This combined tool flow allowed the creation of complex accelerators with performance improvements from

one to three orders of magnitude with respect to the corresponding software-based solutions. Such accelerators were also included in a prototype chip recently fabricated in a 32nm CMOS technology. After that, he also considered the interaction with the operating system with efficient methods for the allocation of massive sets of data in embedded systems [IC.37]. All these approaches promote *design reuse*, which is expected to be a key ingredient for future embedded systems and Dr. Pilato is currently applying them to several other research areas, including machine learning, natural language processing, and computer vision.

Hardware security. Dr. Pilato is actively pursuing an additional line of research for developing design methods that improve the hardware security of hardware accelerators. In collaboration with NYU, Dr. Pilato defined the challenges for integrating security countermeasures into such components in order to mitigate their area/performance overhead [JR.11]. Dr. Pilato is also working on the development of the identified solutions in BAMBU, showing a novel approach based on high-level synthesis. This has already led to one journal submission (under major review) on intrinsic hardware support for dynamic information flow tracking [UR.2], and one conference submission on obscuration techniques to thwart the reverse engineering of the chips to fabricate [UR.3]. In this context, Dr. Pilato is currently an external consultant for a DARPA project involving NYU and Boeing for improving the design time of integrated circuits, while increasing their security level.

Self-adaptive and reconfigurable systems. Dr. Pilato extended his ACO-based co-design methodology [JR.2] to take into account the effects of *partial dynamic reconfiguration* [IC.31] and accordingly specialize the target architecture in terms of static components and reconfigurable regions. This allows the design of adaptive and reconfigurable architectures that are up to three times faster than solutions where the designer was required to manually pre-determine the organization of the architecture. This idea was at the basis of FASTER, an EU-funded project (2011-2014), which was intended to be an extension of hArtes to develop methodologies on the top of existing tools for FPGA synthesis in order to include the aspects related to partial dynamic reconfiguration in the early stages of the hardware/software co-design [WS.10][IC.28]. In this project, he coordinated the technical work among five different partners (i.e., FORTH from Greece, Chalmers University of Technology from Sweden, Imperial College from UK, Politecnico di Milano from Italy, and Ghent University from Belgium) to perform high-level analyses and determine the hardware/software partitioning of a parallel application, along with the level of reconfiguration for each hardware component. In this context, he extensively collaborated with Maxeler, which offers a tool flow to optimize algorithms for scientific computation. For example, he mentored a student, who integrated the proposed methodology in their tools such that they can offer dynamically adaptive systems to their customers [IC.27]. The work received a Technology Transfer Award in 2012, which is an award given by HiPEAC, that is an European Network of Excellence to recognize promising technology transfers between academia and industry. Finally, in consideration of my contributions in this research area, he was also involved in the organization of different workshops and in the technical program committees for the most relevant conferences for adaptive and reconfigurable systems, including but not limited to the IEEE International Conference on Design, Automation and Test in Europe (DATE), which is the most relevant conference for EDA in Europe. He also reused this extensive research in FPGA prototyping for modeling the effects on autonomous dynamic voltage and frequency scaling in complex heterogeneous SoCs [IC.36]. This solution allowed significant energy savings (up to 75%) and performance improvements (up to 10%) when multiple accelerators are executing concurrently and competing for shared resources.

Design of energy-aware smart spaces. The goals of the Kyoto protocol in terms gas reduction and energy savings need a complex ecosystem of intelligent and interacting embedded systems, able to adapt their behavior at runtime accordingly to the environment. In this context, Dr. Pilato applied EDA techniques (i.e., methods to design electronic circuits) to problems from a very different context (e.g., energy management in public spaces). He thus proposed a SystemC-based framework for the simulation of the energy aspects of smart spaces [IC.32]. The key idea is to use a software-based approach to model the behavior of appliances and their power consumption. To reduce peaks in power consumption, he also proposed an architecture with a centralized controller, called *energy box*, to determine when the appliances can absorb energy from the network or when it is better to absorb energy from the equipped batteries. This demonstrated how the achievements of my research can be effectively and efficiently applied to very different contexts and problems, not limited to the design of digital circuits.

Logic and physical optimizations with cell-library extensions. Current EDA tools often rely on standard-cell libraries typically optimized with full-custom layouts. However, the quality of these libraries can considerably impact the result-

ing digital circuits when not properly designed. For this reason, in collaboration with ST Microelectronics (i.e., a leading manufacturer of semiconductors) and NanGate (i.e., an EDA company for standard-cell library optimization, where he was an intern for six months), Dr. Pilato developed a complete design flow for the generation of application-specific standard-cell libraries that can be used in industrial EDA flows for logic and physical synthesis. Specifically, he proposed a methodology to determine which Boolean functions could be implemented with macro gates in order to optimize the circuit. In this way, it is possible to obtain an average reduction of 10% in terms of silicon area and power consumption [IC.12]. This method has been then extended to determine the proper composition of a custom standard-cell library, which allowed a reduction in terms of used cells by almost 90% with negligible impact on the circuits [IC.14]. This research has been at the basis of SYNAPTIC, an FP7-STREP EU project (2009-2013) for improving the manufacturing of digital circuits with regular layouts. With this experience, he recently collaborated in the tape-out and verification of two prototype chips. This allowed the acquisition of an end-to-end expertise in the design of digital circuits.

Scientific Publications

Citations: 594   **H-Index:** 14   (Google Scholar, January 10, 2018)

Refereed Submissions (under review)

UR.3. **C. Pilato**, F. Regazzoni, R. Karri, S. Garg. "TAO: Techniques for Algorithmic Obscuration during High-Level Synthesis," submitted to *ACM/IEEE Design Automation Conference* (DAC 2018) (*under revision*).

UR.2. **C. Pilato**, S. Garg, K. Wu, R. Karri, F. Regazzoni. "TaintHLS: Enabling Dynamic Information Flow Tracking in Hardware Accelerators," submitted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, August 2017 (*under major revision*).

UR.1. P. Fezzardi, **C. Pilato**, F. Ferrandi. "Enabling Automated Bug Detection for IP-based Designs using High-Level Synthesis," submitted to *IEEE Design & Test Magazine*, July 2017 (*under major revision*).

Referred Journal Publications

JR.11. **C. Pilato**, S. Garg, K. Wu, R. Karri, F. Regazzoni. "Securing Hardware Accelerators: a New Challenge for High-Level Synthesis," in *IEEE Embedded Systems Letter*, (*to appear*), 2017.
[doi: http://dx.doi.org/10.1109/LES.2017.2774800]

JR.10. C. Ciobanu, **C. Pilato**, G. Gaydadjiev, D. Sciuto. "The Case for Polymorphic Registers in Dataflow Computing," in *International Journal of Parallel Programming*, (*to appear*), 2017.
[doi: http://dx.doi.org/10.1007/s10766-017-0494-1]

JR.9. **C. Pilato**, P. Mantovani, G. Di Guglielmo, L.P. Carloni. "System-Level Optimization of Accelerator Local Memory for Heterogeneous Systems-on-Chip," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 3, pp. 435–448, March 2017.
[doi: http://dx.doi.org/10.1109/TCAD.2016.2611506]

JR.8. R. Nane, V.-M. Sima, **C. Pilato**, J. Choi, B. Fort, A. Canis, Y.T. Chen, H. Hsiao, S. Brown, F, Ferrandi, J. Anderson, K. Bertels. "A Survey and Evaluation of FPGA High-Level Synthesis Tools," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 10, pp. 1591–1604, October 2016.
[doi: http://dx.doi.org/10.1109/TCAD.2015.2513673]

JR.7. M. Lattuada, **C. Pilato**, F. Ferrandi. "Performance Estimation of Task Graphs based on Path Profiling," in *International Journal of Parallel Programming*, vol. 44, no. 4, pp. 735–771, August 2016.
[doi: http://dx.doi.org/10.1007/s10766-015-0372-7]

JR.6. D. Pnevmatikatos, K. Papadimitriou, T. Becker, P. Böhm, A. Brokalakis, K. Bruneel, C. Ciobanu, T. Davidson, G. Gaydadjiev, K. Heyse, W. Luk, X. Niu, I. Papaefstathiou, D. Pau, O. Pell, **C. Pilato**, M.D. Santambrogio, D. Sciuto, D. Stroobandt, T. Todman, E. Vansteenkiste. "FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration," in *Microprocessors and Microsystems*, vol. 39, no. 4–5, pp. 321–338, June-July 2015.
[doi: http://dx.doi.org/10.1016/j.micpro.2014.09.006]

JR.5. A. Miele, **C. Pilato**, D. Sciuto, "A Simulation-based Framework for the Exploration of Mapping Solutions on Heterogeneous MPSoCs," in *International Journal of Embedded and Real-Time Communication Systems*, vol. 4, no. 1, pp. 22–41, April 2013.
[doi: http://dx.doi.org/10.4018/jertcs.2013010102]

JR.4. S. Cecchi, A. Primavera, F. Piazza, F. Bettarelli, E. Ciavattini, R. Toppi, J.G.F. Coutinho, W. Luk, **C. Pilato**, F. Ferrandi, V.M. Sima, K. Bertels, "The hArtes CarLab: A new approach to advanced algorithms development for automotive audio," in *Journal of the Audio Engineering Society*, vol. 59, no. 11, pp. 858–869, November 2011.
[url: http://www.aes.org/e-lib/browse.cfm?elib=16153]

JR.3. K. Bertels, V.M. Sima, Y. Yankova, G. Kuzmanov, W. Luk, J.G.F. Coutinho, F. Ferrandi, **C. Pilato**, M. Lattuada, D. Sciuto, A. Michelotti, "hArtes: Hardware-Software Codesign for Heterogeneous Multicore Platforms," in *IEEE Micro*, vol. 30, no. 5, pp. 88–97, September 2010.
[doi: http://dx.doi.org/10.1109/MM.2010.91]

JR.2. F. Ferrandi, P.L. Lanzi, **C. Pilato**, D. Sciuto, A. Tumeo, "Ant Colony Heuristic for Mapping and Scheduling Task and Communications on Heterogeneous Embedded Systems," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 6, pp. 911–924, June 2010.

[doi: http://dx.doi.org/10.1109/TCAD.2010.2048354]

JR.1. **C. Pilato**, A. Tumeo, G. Palermo, F. Ferrandi, P.L. Lanzi, D. Sciuto, "Improving Evolutionary Exploration to Area-Time Optimization of FPGA Designs," in *Journal of Systems Architecture*, vol. 54, no. 11, pp. 1046–1057, November 2008.

[doi: http://dx.doi.org/10.1016/j.sysarc.2008.04.010]

Editorial contributions

ED.2. S. Vinco, **C. Pilato**. "Editorial: Special Issue on Innovative Design Methods for Smart Embedded Systems," in *ACM Transactions on Embedded Computing Systems*, vol. 15, no. 2, April 2016.

[doi: http://dx.doi.org/10.1145/2885505]

ED.1. **C. Pilato**, M. Porrmann. "Message from the Program Committee Chairs - EUC 2014," in *Proceedings of the 12th IEEE International Conference on Embedded and Ubiquitous Computing (EUC)*, September 2014.

[doi: https://doi.org/10.1109/EUC.2014.6]

Referred Conference Publications

IC.39. **C. Pilato**, L.P. Carloni, "DarkMem: Fine-Grained Power Management of Local Memories for Accelerators in Embedded Systems," in *Proceedings of the Asia and South Pacific Design Automation Conference* (ASPDAC 2018), Jeju Island, Korea, January 22-25, 2018, pp. 1-6 *(to appear)*.

IC.38. **C. Pilato**, "Bridging the Gap between Software and Hardware Designers using High-Level Synthesis," in *of Parallel Computing with FPGAs Symposium* (paraFPGA 2017), Bologna, Italy, September 12, 2017, pp. 1-10 (*keynote paper*), *(to appear)*.

IC.37. P. Mantovani, E. Cota, **C. Pilato**, G. Di Guglielmo, L.P. Carloni, "Handling Large Data Sets for High-Performance Embedded Applications in Heterogeneous Systems-on-Chip," in *Proceedings of ACM/IEEE International Conference on Compilers, Architectures and Synthesis For Embedded Systems* (CASES 2016), Pittsburgh, PA, USA, October 2-7, 2016, pp. 1-10.

[doi: http://doi.acm.org/10.1145/2968455.2968509]

IC.36. P. Mantovani, E. Cota, K. Tien, **C. Pilato**, G. Di Guglielmo, K. Shepard, L.P. Carloni, "An FPGA-Based Infrastructure for Fine-Grained DVFS Analysis in High-Performance Embedded Systems," in *Proceedings of ACM/IEEE Design Automation Conference* (DAC 2016), Austin, TX, USA, June 5-9, 2016, pp. 1-6.

[doi: http://doi.acm.org/10.1145/2897937.2897984]

IC.35. **C. Pilato**, P. Mantovani, G. Di Guglielmo, L.P. Carloni, "System-Level Memory Optimization for High-Level Synthesis of Component-based SoCs," in *Proceedings of International Conference on Hardware/Software Codesign and System Synthesis* (CODES+ISSS 2014), New Delhi, India, October 12-17, 2014, pp. 1-10.

[doi: http://dx.doi.org/10.1145/2656075.2656098]

IC.34. G. Di Guglielmo, **C. Pilato**, L.P. Carloni, "A Design Methodology for Compositional High-Level Synthesis of Communication-Centric SoCs," in *Proceedings of ACM/IEEE Design Automation Conference* (DAC 2014), San Francisco, CA, USA, June 1-5, 2014, pp. 1-6.

[doi: http://doi.acm.org/10.1145/2593069.2593071]

IC.33. D.N. Pnevmatikatos, T. Becker, A. Brokalakis, G.N. Gaydadjiev, W. Luk, K. Papadimitriou, I. Papaefstathiou, D. Pau, O. Pell, **C. Pilato**, M.D. Santambrogio, D. Sciuto, D. Stroobandt, "Effective Reconfigurable Design: The FASTER Approach," in *Proceedings of 10th International Symposium on Applied Reconfigurable Computing* (ARC 2014), Algarve, Portugal, April 14-16, 2014, pp. 318-323

[doi: http://dx.doi.org/10.1007/978-3-319-05960-0_35]

IC.32. A.A. Nacci, G. Bettinazzi, **C. Pilato**, V. Rana, M.D. Santambrogio, D. Sciuto, "A SystemC-Based Framework for the Simulation of Appliances Networks in Energy-Aware Smart Spaces," in *Proceedings of IEEE World Forum on Internet of Things* (WF-IoT 2014), Seoul, South Korea, March 6-8, 2014.

[doi: http://dx.doi.org/10.1109/WF-IoT.2014.6803215]

IC.31. R. Cattaneo, **C. Pilato**, G. Durelli, M.D. Santambrogio, D. Sciuto, "SMASH: A Heuristic Methodology for Designing Partially Reconfigurable MPSoCs," in *Proceedings of IEEE International Symposium on Rapid System Prototyping* (RSP 2013), Montreal, Canada, October 3-4, 2013, pp. 102–108.

[doi: http://dx.doi.org/10.1109/RSP.2013.6683965]

IC.30. **C. Pilato**, F. Ferrandi, "Bambu: A Modular Framework for the High Level Synthesis of Memory-Intensive Applications," in *Proceedings of 23rd International Conference on Field Programmable Logic and Applications* (FPL 2013), Porto, Portugal, September 2-4, 2013, pp. 1–4.

[doi: http://dx.doi.org/10.1109/FPL.2013.6645550]

IC.29. C. Ciobanu, G. Gaydadjiev, **C. Pilato**, D. Sciuto, "Dataflow Computing with Polymorphic Registers," in *Proceedings of IEEE International Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation* (SAMOS 2013), Samos, Greece, July 15-18, 2013, pp. 314–321.

[doi: http://dx.doi.org/10.1109/SAMOS.2013.6621140]

IC.28. **C. Pilato**, R. Cattaneo, G. Durelli, A.A. Nacci, M.D. Santambrogio, D. Sciuto, "A2B: an Integrated Framework for Designing Heterogeneous and Reconfigurable Systems," in *Proceedings of the 2013 NASA/ESA Conference on Adaptive Hardware and Systems* (AHS 2013), Torino, Italy, June 25-27, 2013, pp. 198–203.

[doi: http://dx.doi.org/10.1109/AHS.2013.6604246]

IC.27. R. Cattaneo, **C. Pilato**, M. Mastinu, O. Kadlcek, O. Pell, M.D. Santambrogio, "Runtime Adaptation on Dataflow HPC Platforms," in *Proceedings of the 2013 NASA/ESA Conference on Adaptive Hardware and Systems* (AHS 2013), Torino, Italy, June 25-27, 2013, pp. 84–91.

[doi: http://dx.doi.org/10.1109/AHS.2013.6604230]

IC.26. F. Ferrandi, P.L. Lanzi **C. Pilato**, D. Sciuto, A. Tumeo, "Ant Colony Optimization for Mapping, Scheduling and Placing in Reconfigurable Systems," in *Proceedings of the 2013 NASA/ESA Conference on Adaptive Hardware and Systems* (AHS 2013), Torino, Italy, June 25-27, 2013, pp. 47–54.

[doi: http://dx.doi.org/10.1109/AHS.2013.6604225]

IC.25. M.D. Santambrogio, **C. Pilato**, D. Pnevmatikatos, K. Papadimitriou, D. Stroobandt, D. Sciuto, "The FASTER Vision for Designing Dynamically Reconfigurable Systems," in *Proceedings of the International Conference on IC Design and Technology* (ICICDT 2013), Pavia, Italy, May 29-31, 2013, pp. 5–8, (*invited paper*).

[doi: http://dx.doi.org/10.1109/ICICDT.2013.6563290]

IC.24. K. Papadimitriou, **C. Pilato**, D. Pnevmatikatos, M.D. Santambrogio, C. Ciobanu, T. Todman, T. Becker, T. Davidson, X. Niu, G. Gaydadjiev, W. Luk, D. Stroobandt, "Novel Design Methods and a Tool Flow for Unleashing Dynamic Reconfiguration," in *Proceedings of 10th International Conference on Embedded and Ubiquitous Computing* (EUC 2012), Paphos, Cyprus, December 5-7, 2012, pp. 391–398.

[doi: http://doi.ieeecomputersociety.org/10.1109/ICCSE.2012.61]

IC.23. A. Miele, **C. Pilato**, D. Sciuto, "An Automated Framework for the Simulation of Mapping Solutions on Heterogeneous MPSoCs," in *Proceedings of International Symposium on System-on-Chip* (SoC 2012), Tampere, Finland, October 11-12, 2012, pp. 1–6.

[doi: http://dx.doi.org/10.1109/ISSoC.2012.6376354]

IC.22. D. Pnevmatikatos, T. Becker, A. Brokalakis, K. Bruneel, G. Gaydadjiev, W. Luk, K. Papadimitriou, I. Papaefstathiou, O. Pell, **C. Pilato**, M. Robart, M.D. Santambrogio, D. Sciuto, D. Stroobandt, T. Todman, "FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration," in *Proceedings of 15th Euromicro Conference on Digital System Design* (DSD 2012), Cesme, Izmir, Turkey, September 5-8, 2012, pp. 234–241.

[doi: http://dx.doi.org/10.1109/DSD.2012.59]

IC.21. A. Cazzaniga, G. Durelli, **C. Pilato**, D. Sciuto, M.D. Santambrogio, "On the Development of a Runtime Reconfigurable Multicore System-on-Chip," in *Proceedings of 15th Euromicro Conference on Digital System Design* (DSD 2012), Cesme, Izmir, Turkey, September 5-8, 2012, pp. 132–135.

[doi: http://dx.doi.org/10.1109/DSD.2012.93]

IC.20. A. Bonetto, A. Cazzaniga, G. Durelli, **C. Pilato**, D. Sciuto, M.D. Santambrogio, "An open-source design and validation platform for reconfigurable systems," in *Proceedings of 22nd International Conference on Field Programmable Logic and Applications* (FPL 2012), Oslo, Norway, August 29-31, 2012, pp. 707–710.

[doi: http://dx.doi.org/10.1109/FPL.2012.6339158]

IC.19. **C. Pilato**, A. Cazzaniga, G. Durelli, A. Otero, D. Sciuto, M.D. Santambrogio, "On The Automatic Integration of Hardware Accelerators into FPGA-based Embedded Systems," in *Proceedings of 22nd International Conference on Field Programmable Logic and Applications* (FPL 2012), Oslo, Norway, August 29-31, 2012, pp. 607–610.

[doi: http://dx.doi.org/10.1109/FPL.2012.6339218]

IC.18. A. Bonetto, A. Cazzaniga, G.C. Durelli, **C. Pilato**, D. Sciuto, M.D. Santambrogio, "TaBit: a Framework for Task Graph to Bitstream Generation," in *Proceedings of IEEE International Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation* (SAMOS 2012), Samos, Greece, July 16-19, 2012, pp. 201–208.

[doi: http://dx.doi.org/10.1109/SAMOS.2012.6404175]

IC.17. **C. Pilato**, F. Ferrandi, D. Sciuto, "A Design Methodology to Implement Memory Accesses in High-Level Synthesis," in *Proceedings of ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis* (CODES+ISSS 2011), Taipei, Taiwan, October 9-14, 2011, pp. 49-58.

[doi: http://dx.doi.org/10.1145/2039370.2039381]

IC.16. **C. Pilato**, V.G. Castellana, S. Lovergine, F. Ferrandi, "A Runtime Adaptive Controller for Supporting Hardware Components with Variable Latency," in *Proceedings of NASA/ESA Conference on Adaptive Hardware and Systems* (AHS 2011), San Diego, CA, USA, June 6-9, 2011, pp. 153-160.

[doi: http://dx.doi.org/10.1109/AHS.2011.5963930]

IC.15. C. Bolchini, A. Miele, **C. Pilato**, "Combined Architecture and Hardening Techniques Exploration for Reliable Embedded System Design," *Proceedings of 31st ACM Great Lakes Symposium on VLSI* (GLSVLSI 2011), Lausanne, Switzerland, May 2-4, 2011, pp. 301-306.

[doi: http://dx.doi.org/10.1145/1973009.1973069]

IC.14. **C. Pilato**, F. Ferrandi, D. Pandini, "A Design Methodology for the Automatic Sizing of Standard-Cell Libraries," *Proceedings of 31st ACM Great Lakes Symposium on VLSI* (GLSVLSI 2011), Lausanne, Switzerland, May 2-4, 2011, pp. 151-156.

[doi: http://dx.doi.org/10.1145/1973009.1973040]

IC.13. S. Cecchi, A. Primavera, F. Piazza, F. Bettarelli, E. Ciavattini, R. Toppi, J.G.F. Coutinho, W. Luk, **C. Pilato**, F. Ferrandi, V. M. Sima, K. Bertels, "The hArtes CarLab: A New Approach to Advanced Algorithms Development for Automotive Audio," *Proceedings of 129th Audio Engineering Society Convention* (AES 2010), San Francisco, CA, USA, November 4-7, 2010, pp. 1-12.

[url: http://www.aes.org/e-lib/browse.cfm?elib=15605]

IC.12. **C. Pilato**, F. Ferrandi, D. Pandini, "A Fast Heuristic for Extending Standard Cell Libraries with Regular Macro Cells," *Proceedings of IEEE Computer Society Annual Symposium on VLSI* (ISVLSI 2010), Lixouri, Kefalonia, Greece, July 5-7, 2010, pp. 23-28.

[doi: http://doi.ieeecomputersociety.org/10.1109/ISVLSI.2010.69]

IC.11. F. Ferrandi, **C. Pilato**, A. Tumeo, D. Sciuto, "Mapping and Scheduling of Parallel C Applications with Ant Colony Optimization onto Heterogeneous Reconfigurable MPSoCs," *Proceedings of IEEE Asia and South Pacific Design Automation Conference* (ASPDAC 2010), Taipei, Taiwan, January 18-21, 2010, pp. 799 - 804.

[doi: http://dx.doi.org/10.1109/ASPDAC.2010.5419782]

IC.10. M. Branca, L. Camerini, F. Ferrandi, P.L. Lanzi, **C. Pilato**, D. Sciuto, A. Tumeo, "Mapping pipelined applications onto heterogeneous embedded systems: a Bayesian Optimization Algorithm based approach," *Proceedings of ACM/IEEE International Conference on Hardware-Software Codesign and System Synthesis* (CODES+ISSS 2009), Grenoble, France, October 11-16, 2009, pp. 443-452.

[doi: http://doi.acm.org/10.1145/1629435.1629495]

IC.9. F. Ferrandi, M. Lattuada, **C. Pilato**, A. Tumeo, "Performance Modeling of Parallel Applications on MPSoCs," *Proceedings of IEEE International Symposium on System-on-Chip* (SOC 2009), Tampere, Finland, October 5-7, 2009, pp. 64-67.

[doi: http://dx.doi.org/10.1109/SOCC.2009.5335675]

IC.8. F. Ferrandi, M. Lattuada, **C. Pilato**, A. Tumeo, "Performance Estimation for Task Graphs Combining Sequential Path Profiling and Control Dependence Regions," *Proceedings of ACM/IEEE International Conference on Formal Methods and Models for Codesign* (MEMOCODE 2009), Cambridge, MA, USA, July 13-15, 2009, pp. 131-140.

[doi: http://dx.doi.org/10.1109/MEMCOD.2009.5185389]

IC.7. M. Branca, L. Camerini, F. Ferrandi, P.L. Lanzi, **C. Pilato**, D. Sciuto, A. Tumeo, "Evolutionary algorithms for the mapping of pipelined applications onto heterogeneous embedded systems," *Proceedings of ACM/IEEE Genetic and Evolutionary Computation Conference* (GECCO 2009), Montreal, Canada, July 8-12, 2009, pp. 1435-1442.

[doi: http://doi.acm.org/10.1145/1569901.1570094]

IC.6. A. Tumeo, **C. Pilato**, G. Palermo, F. Ferrandi, D. Sciuto, "HW/SW methodologies for synchronization in FPGA multiprocessors," *Proceedings of ACM/SIGDA International Symposium on Field-Programmable Gate Arrays* (FPGA 2009), Monterey, CA, USA, February 22-24, 2009, pp. 265-268.

[doi: http://doi.acm.org/10.1145/1508128.1508174]

IC.5. A. Tumeo, **C. Pilato**, F. Ferrandi, D. Sciuto, P.L. Lanzi, "Ant Colony Optimization for Mapping and Scheduling in Heterogeneous Multiprocessor Systems," *Proceedings of IEEE International Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation* (SAMOS 2008), Samos, Greece, July 21-24, 2008, pp. 142-149.

[doi: http://dx.doi.org/10.1109/ICSAMOS.2008.4664857]

IC.4. **C. Pilato**, D. Loiacono, F. Ferrandi, P.L. Lanzi, D. Sciuto, "High-level Synthesis with Multi-objective Genetic Algorithm: a Comparative Encoding Analysis," *Proceedings of IEEE Congress on Evolutionary Computation* (CEC 2008), Hong Kong, China, June 1-6, 2008, pp. 3334-3341.

[doi: http://dx.doi.org/10.1109/CEC.2008.4631249]

IC.3. **C. Pilato**, D. Loiacono, F. Ferrandi, P.L. Lanzi, D. Sciuto, "A multi-objective genetic algorithm for design space exploration in high-level synthesis," *Proceedings of IEEE Computer Society Annual Symposium on VLSI* (ISVLSI 2008), Montpellier, France, April 7-9, 2008. pp. 417-422.

[doi: http://dx.doi.org/10.1109/ISVLSI.2008.73]

IC.2. **C. Pilato**, G. Palermo, A. Tumeo, F. Ferrandi, D. Sciuto, P.L. Lanzi, "Fitness Inheritance in Evolutionary and Multi-Objective High-Level Synthesis," *Proceedings of IEEE Congress on Evolutionary Computation* (CEC 2007), Singapore, September 25-28, 2007, pp. 3459-3466.

[doi: http://dx.doi.org/10.1109/CEC.2007.4424920]

IC.1. F. Ferrandi, P.L. Lanzi, G. Palermo, **C. Pilato**, D. Sciuto, A. Tumeo, "An Evolutionary Approach to Area-Time Optimization of FPGA designs," *Proceedings of IEEE International Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation* (SAMOS 2007), Samos, Greece, July 16-19, 2007, pp. 145-152.

[doi: http://dx.doi.org/10.1109/ICSAMOS.2007.4285745]

Book Chapters

IB.4. F. Bettarelli, E. Ciavattini, A. Lattanzi, G. Beltrame, F. Ferrandi, L. Fossati, **C. Pilato**, D. Sciuto, R.J. Meeuws, S.A. Ostadzadeh, Z. Nawaz, Y. Lu, T. Marconi, M. Sabeghi, V.M. Sima, K. Sigdel, "Extensions of the hArtes Tool Chain," in *Hardware/Software Co-design for Heterogeneous Multi-core Platforms*, K. Bertels (Eds.), Springer, pp. 193-228, November 2011 (ISBN: 978-94-007-1405-2 (Print) 978-94-007-1406-9 (Online))

[doi: http://dx.doi.org/10.1007/978-94-007-1406-9_6]

IB.3. S. Cecchi, L. Palestini, P. Peretti, A. Primavera, F. Piazza, F. Capman, S. Thabuteau, C. Levy, J.F. Bonastre, A. Lattanzi, E. Ciavattini, F. Bettarelli, R. Toppi, E. Capucci, F. Ferrandi, M. Lattuada, **C. Pilato**, D. Sciuto, W. Luk, J.G.F. Coutinho, "In Car Audio," in *Hardware/Software Co-design for Heterogeneous Multi-core Platforms*, K. Bertels (Eds.), Springer, pp. 155-192, 2012 (ISBN: 978-94-007-1405-2 (Print) 978-94-007-1406-9 (Online))

[doi: http://dx.doi.org/10.1007/978-94-007-1406-9_5]

IB.2. K. Bertels, A. Lattanzi, E. Ciavattini, F. Bettarelli, M.T. Chiaradia, R. Nutricato, A. Morea, A. Antola, F. Ferrandi, M. Lattuada, **C. Pilato**, D. Sciuto, R.J. Meeuws, Y. Yankova, V.M. Sima, K. Sigdel, W. Luk, J.G.F. Coutinho, Y.M Lam, T. Todman, A. Michelotti, A. Cerruto, "The hArtes Tool Chain," in *Hardware/Software Co-design for Heterogeneous Multi-core Platforms*, K. Bertels (Eds.), Springer, pp. 9-110, 2012 (ISBN: 978-94-007-1405-2 (Print) 978-94-007-1406-9 (Online))

[doi: http://dx.doi.org/10.1007/978-94-007-1406-9_2]

IB.1. **C. Pilato**, D. Loiacono, A. Tumeo, F. Ferrandi, P.L. Lanzi and D. Sciuto, "Speeding-Up Expensive Evaluations in High-Level Synthesis Using Solution Modeling and Fitness Inheritance," in *Computational Intelligence in Expensive Optimization Problems*, Y. Tenne and C.-K. Goh (Eds.), Springer, pp. 701-723, 2010 (ISBN: 978-3-642-10700-9 (Print) 978-3-642-10701-6 (Online))

[doi: http://dx.doi.org/10.1007/978-3-642-10701-6_26]

Workshop Publications

WS.18. **C. Pilato**, L.P. Carloni, F. Regazzoni, "Automatic generation of encrypted local memories for IoT devices," in *Proceedings of VLSI for IoT Workshop* (VLSI-IoT) (held in conjunction with DATE 2017), Lausanne, Switzerland, March 30, 2017. *(poster presentation)*

WS.17. G.C. Durelli, F. Spada, **C. Pilato**, M.D. Santambrogio, "Scala-based Domain-Specific Language for Creating Accelerator-based SoCs," in *Proceedings of 23rd Reconfigurable Architectures Workshop* (RAW 2016), Chicago, IL, USA, May 23-24, 2016, pp. 1–8.

[doi: http://doi.ieeecomputersociety.org/10.1109/IPDPSW.2016.169]

WS.16. **C. Pilato**, Q. Xu, P. Mantovani, G. Di Guglielmo, L.P. Carloni, "On the Design of Scalable and Reusable Accelerators for Big Data Applications," in *Proceedings of Workshop on Big Data Analytics* (BigDAW 2016), Como, Italy, May 16-18, 2016, pp. 1–6, (*invited paper*).

[doi: http://dx.doi.org/10.1145/2903150.2906141]

WS.15. P. Mantovani, E.G. Cota, S. Kim, K. Tien, J. Chan, G. Di Guglielmo, **C. Pilato**, M.A. Kim, M. Seok, K. Shepard, L.P. Carloni, "Benchmarking Methodology for Embedded Scalable Platforms," in *Proceedings of Workshop on Suite of Embedded Applications and Kernels* (SEAK 2014) (held in conjunction with DAC 2014), San Francisco, CA, USA, June 1, 2014. *(poster presentation)*.

WS.14. G.C. Durelli, F. Spada, R. Cattaneo, **C. Pilato**, D. Pau, M.D. Santambrogio, "Adaptive Raytracing Implementation using Partial Dynamic Reconfiguration," in *Proceedings of 21st Reconfigurable Architectures Workshop* (RAW 2014), Phoenix, AZ, USA, May 19-20, 2014, pp. 1–8.

[doi: http://dx.doi.org/10.1109/IPDPSW.2014.31]

WS.13. R. Cattaneo, R. Bellini, G.C. Durelli, **C. Pilato**, M.D. Santambrogio, D. Sciuto, "PaRA-Sched: a Reconfiguration-Aware Scheduler for Reconfigurable Architectures," in *Proceedings of 21st Reconfigurable Architectures Workshop* (RAW 2014), Phoenix, AZ, USA, May 19-20, 2014, pp. 1–8.

[doi: http://dx.doi.org/10.1109/IPDPSW.2014.32]

WS.12. A.A. Nacci, **C. Pilato**, M.D. Santambrogio, D. Sciuto, "Designing Self-Adaptive Smart Spaces for Energy Saving," in *Proceedings of 2nd Workshop on Self-Awareness in Reconfigurable Computing Systems* (SRCS 2013), Porto, Portugal, September, 5, 2013, pp. 1–4.

WS.11. F. Cancare, **C. Pilato**, A. Cazzaniga, D. Sciuto, M.D. Santambrogio, "A Complete Methodology to Implement Self Dynamic Reconfigurable FPGA-Based Systems," in *Proceedings of 8th International Workshop on Reconfigurable Communication-centric Systems-on-Chip* (ReCoSoC 2013), Darmstadt, Germany, July, 10-12, 2013, pp. 1–7.

[doi: http://dx.doi.org/10.1109/ReCoSoC.2013.6581550]

WS.10. R. Cattaneo, X. Niu, **C. Pilato**, T. Becker, W. Luk, M.D. Santambrogio, "A Framework for Effective Exploitation of Partial Reconfiguration in Dataflow Computing," in *Proceedings of 8th International Workshop on Reconfigurable Communication-centric Systems-on-Chip* (ReCoSoC 2013), Darmstadt, Germany, July, 10-12, 2013, pp. 1–8.

[doi: http://dx.doi.org/10.1109/ReCoSoC.2013.6581535]

WS.9. G. Durelli, A. A. Nacci, R. Cattaneo, **C. Pilato**, D. Sciuto, M.D. Santambrogio, "A Flexible and Reconfigurable Interconnection Structure for FPGA Dataflow Applications," in *Proceedings of 20th Reconfigurable Architectures Workshop* (RAW 2013), Boston, MA, USA, May 20-21, 2013, pp. 1–8.

[doi: http://doi.ieeecomputersociety.org/10.1109/IPDPSW.2013.127]

WS.8. **C. Pilato**, R. Cattaneo, G. Durelli, A. Nacci, M.D. Santambrogio, D. Sciuto, "A2B: a Framework for the Fast Prototyping of Reconfigurable Systems," in *Proceedings of 7th HiPEAC Workshop on Reconfigurable Computing* (WRC 2013), Berlin, Germany, January, 21, 2013, pp. 1–10.

WS.7. M.D. Santambrogio, D. Pnevmatikatos, K. Papadimitriou, **C. Pilato**, G. Gaydadjiev, D. Stroobandt, T. Davidson, T. Becker, T. Todman, W. Luk, A. Bonetto, A. Cazzaniga, G. Durelli, D. Sciuto, "Smart Technologies for Effective Reconfiguration: The FASTER approach," in *Proceedings of 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip* (ReCoSoC 2012), York, UK, July, 9-11, 2012, pp. 1–7.

[doi: http://dx.doi.org/10.1109/ReCoSoC.2012.6322881]

WS.6. G. Durelli, A. Cazzaniga, **C. Pilato**, M.D. Santambrogio, D. Sciuto, "Automatic Run-Time Manager Generation for Reconfigurable MPSoC Architectures," in *Proceedings of 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip* (ReCoSoC 2012), York, UK, July, 9-11, 2012, pp. 1–8.

[doi: http://dx.doi.org/10.1109/ReCoSoC.2012.6322883]

WS.5. **C. Pilato**, F. Ferrandi, "Improving Design Regularity by Targeting Custom Standard-Cell Libraries," in *Workshop on "Variability modelling and mitigation techniques in current and future technologies"* (VAMM 2012) (held during DATE 2012), Dresden, Germany, March 2012, *(poster presentation)*.

WS.4. **C. Pilato**, F. Ferrandi, D. Pandini, "Evaluating Static CMOS Complex Cells in Technology Mapping," in *Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms* (ERDIAP 2011), Como, Italy, February 23, 2011, pp. 222-229.

[url: https://www.vde-verlag.de/proceedings-en/563333031.html]

WS.3. M. Elhoj, A. Reis, R. Ribas, F. Ferrandi, **C. Pilato**, F. Moll, M. Miranda, P. Dobrovolny, N. Woolaway, A. Grasset, P. Bonnot, G. Desoli, D. Pandini, "SYNAPTIC Project: Regularity Applied to Enhance Manufacturability and Yield at Several Abstraction Levels," in *Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms* (ERDIAP 2011), Como, Italy, February 23, 2011, pp. 189-192 *(invited paper)*.

[url: https://www.vde-verlag.de/proceedings-en/563333026.html]

WS.2. F. Ferrandi, M. Lattuada, **C. Pilato**, D. Sciuto, "Performance Estimation for Mapping and Scheduling Parallel Applications on Heterogeneous Multi-Processor Systems," in *Workshop on "The European landscape of reconfigurable computing: Lessons learned, new perspectives and innovations"* (held during DATE 2010), Dresden, Germany, March 2010, *(poster presentation)*.

WS.1. **C. Pilato**, F. Ferrandi, P.L. Lanzi G. Palermo, A. Tumeo, D. Sciuto, "Bambu: a High Level Synthesis Framework with Evolutionary Design Space Exploration," in *Workshop on "The New Wave of the High-Level Synthesis"* (held during DATE 2008), Munich, Germany, March 2008, *(poster presentation)*.

Teaching Experience

Graduate level

- Teaching collaborator, "COMS E6998: Topics in Computer Science: Embedded Scalable Platforms" - Computer Science (Columbia University) - Spring 2015, Spring 2016.
- Teaching assistant, "Progettazione Hardware" - Computer Engineering (Politecnico di Milano) - 2010–2011, 2012–2013.
- Teaching assistant, "Metodologie di Progetto Hardware" - Computer Engineering (Politecnico di Milano) - 2008–2009.

Undergraduate level

- Teaching assistant, "Reti Logiche" - Computer Engineering (Politecnico di Milano) - 2007–2012, 2017–2018.
- Teaching assistant, "Architetture dei Calcolatori e Sistemi Operativi" - Telecommunications Engineering (Politecnico di Milano) - 2009–2012.
- Lab supervisor, "Informatica A" - Mathematical Engineering (Politecnico di Milano) - 2011–2012.
- Teaching assistant, "Informatica 2" - Telecommunications Engineering (Politecnico di Milano) - 2008–2009.
- Lab tutor, "Informatica 2" - Telecommunications Engineering (Politecnico di Milano) - 2007–2008.

Thesis Mentoring

- *Antonio Verlotta*, "Designing a Quantum Error Correction System on FPGA", advisor: D. Sciuto (in collaboration with the Quantum Information Science Theory Group at the National Institute of Informatics, Tokyo, Japan), 2014.
- *Matteo Mastinu*, "Design Flow to Support Dynamic Partial Reconfiguration on Maxeler Architectures", advisor: M.D. Santambrogio (in collaboration with Maxeler Technologies, London, UK, part of this thesis has been published in [IC.27] and won the "2012 HiPEAC Technology Transfer Award"), 2012.
- *Gianluca Durelli*, "A^2B: Application to Bitstream. Flusso semi automatico per lo sviluppo di MPSoC riconfigurabili", advisor: D. Sciuto, (part of this thesis has been in published in [WS.6][IC.18][IC.19]), 2012.
- *Stefano Manni*, "A Methodology for Improving the Library-Free Logic Synthesis of Integrated Circuits", advisor: F. Ferrandi, 2012.
- *Vito Giovanni Castellana* and *Silvia Lovergine*, "A Design Methodology for Efficient HLS Controllers", advisor: F. Ferrandi, (part of this thesis has been published in [IC.16]), 2010.
- *Luca Sisler*, "Metodologie di progetto per circuiti regolari", advisor: F. Ferrandi, 2010.
- *Andrea Conti*, 'Technology Mapping for Dynamic Cell Generation based on Canonical Boolean Matching", advisor: F. Ferrandi, 2009.

- *Francesca Malcotti*, "High-Level Synthesis optimization combining speculative execution and SSA-based liveness analysis", advisor: F. Ferrandi, 2008.
- *Gerardo Gallucci*, "Regularity-aware synthesis and regularity extraction from circuit RTL and structural logical representation", advisor: F. Ferrandi (in collaboration with STMicroelectronics, Agrate, MI, Italy), 2008.

In addition, Christian Pilato supervised the activity of around 20 M.Sc. and 3 Ph.D. students at Politecnico di Milano, and 2 students at Columbia University.

Academic Community Involvement

Conference and Workshop Organization

- Organizing Co-Chair for the Scientific School on "Designing Cyber-Physical Systems – From concepts to implementation", Porto Conte Ricerche, September 25-30, 2017.
- Special Session and Tutorial Chair for the 35th IEEE International Conference on Computer Design (ICCD 2017)
- Special Session and Tutorial Chair for the 34th IEEE International Conference on Computer Design (ICCD 2016)
- Special Session and Tutorial Chair for the 33rd IEEE International Conference on Computer Design (ICCD 2015)
- Publicity Chair for the 10th IEEE NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2015)
- Program Chair for the 12th IEEE/IFIP International Conf. on Embedded and Ubiquitous Computing (EUC 2014)
- Organizing Chair for the Workshop on "ReconfigurAble Computing for Embedded Systems" (RACES 2014), held in conjunction with the Design Automation Conference (DAC 2014)
- Publicity Chair of the 9th IEEE International Conference on Networking, Architecture, and Storage (NAS 2014)
- Program Vice-Chair and Track Chair ("Embedded System Architectures") for the 11th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC 2013)
- Organizing Co-Chair for the Workshop on "Variability modelling and mitigation techniques in current and future technologies" (VAMM 2012), held in conjunction with the conference on Design, Automation & Test in Europe (DATE 2012)

Technical Program Committee Work

- IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE), 2015–2016, 2018
- IEEE/ACM International Conference on Compilers, Architecture, and Synthesis of Embedded Systems (CASES), 2016–2017
- Conference on Design and Architectures for Signal and Image Processing (DASIP), 2017
- Symposium on Parallel Computing with FPGAs (ParaFPGA), 2017
- IEEE International Conference on Field-programmable Logic and Applications (FPL), 2015–2017
- International Workshop on Big Data Analytics (BigDAW), 2017
- International Workshop on Reliability, Security and Quality (RESCUE), 2017
- ACM International Conference on Computing Frontiers (CF), 2016–2017
- International Symposium on Applied Reconfigurable Computing (ARC), 2014–2017
- HiPEAC Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO), 2015–2017
- IEEE NASA/ESA Conference on Adaptive Hardware and Systems (AHS), 2015–2017
- IEEE Workshop on Virtual Prototyping of Parallel and Embedded Systems (ViPES), 2015–2016
- HiPEAC Workshop on Reconfigurable Computing (WRC), 2014–2016
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC), 2012–2015
- IEEE International Conference on ReConFigurable Computing and FPGAs (ReConFig), 2012–2015
- IEEE International Reconfigurable Architectures Workshop (RAW), 2013–2015
- IEEE Southern Programmable Logic Conference (SPL), 2012–2014
- Workshop on Variability modeling and mitigation techniques in current and future technologies (VAMM), 2012
- Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms (ERDIAP), 2011

Editorial Experience

- Guest Editor of the special issue on "Innovative design methods for smart embedded systems" in ACM Transaction on Embedded Computing (TECS), vol. 15, no. 2, May 2016 (http://dx.doi.org/10.1145/2885505)

Reviewer Role for Research Proposals

- NSF Graduate Research Fellowship Program (GRFP), 2016

Reviewer Role for Conferences and Journals
- ACM Transactions on Embedded Computing (TECS)
- ACM Transactions on Reconfigurable Technology Systems (TRETS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE Transactions on Emerging Topics in Computing
- IEEE Design & Test (D&T)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Evolutionary Computation (TEC)
- IEEE Transactions on Computers (TC)
- IEEE Embedded Systems Letters (ESL)
- Elsevier International Journal on Systems Architecture (JSA)
- International Journal of Signal Processing Systems (JSPS)
- International Journal on Microprocessors and Microsystems (MICPRO)
- International Journal of High Performance Systems Architecture (IJHPSA)
- International Journal on Design Automation for Embedded Systems (DAES)
- IEEE/ACM Design Automation Conference (DAC)
- IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE)
- IEEE International Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
- IEEE International Parallel & Distributed Processing Symposium (IPDPS)
- IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
- IEEE/ACM International Conference on Embedded Software (EMSOFT)
- IEEE International Conference on Field Programmable Logic and Applications (FPL)
- IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)
- IEEE International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)
- IEEE International Symposium on Circuits and Systems (ISCAS)

Memberships
- ACM   *2015 – present*
- IEEE and IEEE Computer Society   *2008 – present*

Presentations

Invited Talks at Conferences and Workshops
- "High-Level Synthesis: problem solved or open challenge?" at the IEEE International Conference on Field-Programmable Technology (FPT 2017), Melbourne, Australia, December 13, 2017 (**keynote presentation**).
- "Bridging the Gap between Software and Hardware Designers" at the symposium on Parallel Computing with FPGAs (ParaFPGA 2017), held in conjunction with ParCo 2017, Bologna, Italy, September 12, 2017 (**keynote presentation**).
- "Accelerator Memory Design for Heterogeneous System-on-Chip Architectures" at the Memory Architecture and Organization Workshop (MeAOW 2014), held in conjunction with the Embedded System Week (ESWEEK 2014), New Delhi, India, October 16, 2014.
- "Emerging challenges and trends in hardware acceleration for adaptive systems" at the Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHA'N'GE 2014), held in conjunction with the 51st Design Automation Conference (DAC 2014), San Francisco, CA, USA, June 1, 2014.
- "A2B: a Framework for the Fast Prototyping of Reconfigurable Systems" at the Workshop on Reconfigurable Computing (WRC 2013), Berlin, Germany, January 21, 2013.
- "On the Automatic Creation of Custom Standard-Cell Libraries" at the Workshop on Methods and tools to cope with the design challenges in the next generations of technologies, Milano, Italy, May 16, 2012.
- "A Design Exploration Framework for Mapping and Scheduling onto Heterogeneous MPSoCs" at the 3rd Workshop on Mapping Applications to MPSoCs, St. Goar, Germany, June 29-30, 2010.

Conference Tutorials
- "Bambu: An open-source framework for research in high-level synthesis" at the IEEE International Conference on

Field-Programmable Technology (FPT 2017), Melbourne, Australia, December 14, 2017.
- "Designing Multi-Bank Memories for Heterogeneous Architectures" at the ACM/IEEE Embedded Systems Week (ESWEEK 2017), Seoul, South Korea, October 15, 2017.
- "Bambu: An open-source framework for research in high-level synthesis" at the IEEE International Conference on Field-Programmable Logic and Applications (FPL 2017), Ghent, Belgium, September 7, 2017.

Academic Seminars
- "Optimizing private local memories in heterogeneous architectures" at University of California Irvine (UCI), Irvine, CA, USA, June 14, 2017.
- "Designing and Optimizing Hardware Accelerators with Private Local Memories" at Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, May 24, 2017.
- "TaintHLS: Enabling Dynamic Information Flow Tracking in Hardware Accelerators" at New York University (NYU), New York, NY, USA, November 2, 2016.
- "System-Level Memory Optimization for Heterogeneous System-on-Chip Architectures" at Università della Svizzera italiana (USI), Lugano, Switzerland, January 16, 2015.
- "Design Challenges and Techniques for Heterogeneous Reconfigurable Systems" at École Polytechnique, Montréal, QC, Canada, September 26, 2013.
- "On the Automatic Synthesis of Hardware Accelerators for Improving Embedded Systems" at Columbia University, New York, NY, USA, May 23, 2013.
- "Accelerating research in reconfigurable computing: the FASTER approach" at Massachusetts Institute of Technology, Boston, MA, USA, May 22, 2013.

Industrial Seminars
- "PandA-Bambu: A free software framework for the High-Level Synthesis of Complex Applications" at European Space Research and Technology Centre (ESA-ESTEC), Noordwijk, The Netherlands, April 12, 2012.
- "Field Programmable Gate Array (FPGA): design and testability" at Alenia AerMacchi, Venegono Inferiore (VA), Italy, February 3, 2008.

References

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Lugano, January 10, 2018

Signature

Christian Pilato