Paolo Mantovani

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Experience

Jun 2021 – present **Google Research (New York, NY)**, *Senior Software Engineer*.

- `Google Brain Architecture`: As part of the Brain computer architecture team in Google Research, I am contributing to the design and implementation of hardware to accelerate Google's data center applications.

Jun 2017 – June 2021 **Columbia University (New York, NY)**, *Associate Research Scientist*.

- `ESP`: I was the technical lead for the development and implementation of the hardware architecture and design methodology of ESP, an open source platform for heterogeneous system-on-chip design that provides automated flows for the integration of domain-specific accelerators and general purpose processors, including some open source RISC-V cores. With more than 1,400 commits and 30 forks on GitHub, ESP is a rapidly evolving tool for the design of innovative and efficient SoCs. The repository has contributors from several research institution, including Columbia, Harvard, Illinois, IBM Research and PNNL www.esp.cs.columbia.edu.
- `BISC`: I advised the team and designed a real-time FPGA interface for the DARPA NESD project Bioelectronic Interfacing to Sensory Cortex. The BISC implantable chip can record spikes from neurons and stimulate the visual cortex with a required bandwidth of 100 Mbps across a custom RF board, an FPGA for data filtering and a point-to-point 802.11 WiFi channel. The BISC project is led by Columbia and involves Caltech, NYU, Duke, Baylor, University of Utah, Northwestern University, University of Oslo, together with Medtronic and Blackrock Microsystems.

Mar 2020 – Jun 2020 **Adecco for Google LLC, Infrastructure and Cloud (Sunnyvale, CA)**, *Temp Contractor*.

- Demonstration of a new system-on-chip architecture and design solution. As a deliverable, I implemented the RTL of a system that integrates one existing hardware IP block from Google and a new component of interest in the span of just three weeks.

Jun 2016 – Sep 2016 **D. E. Shaw Research (New York, NY)**, *Graduate Intern*.

- Exploration of novel formal verification techniques applied to the network of the Anton 3 supercomputer for molecular-dynamics simulations. I proved with formal methods the equivalence of high-level models for simulation against their corresponding optimized RTL implementation.

Jun 2015 – Sep 2015 **Intel Federal LLC (Hillsboro, OR)**, *Graduate Intern*.

- Design of a digital synchronizer for a large multi-clock domain interconnect as part of the "FastForward Processor" program supported by the United State Department of Energy

Sep 2011 – May 2017 **Columbia University (New York, NY)**, *Graduate Research Assistant*.

- Scalable hardware architecture, software stack and companion system-level-design methodology for future heterogeneous system-on-chip with specialized hardware accelerators. Adopting this combination of architecture and design methodology enables faster design cycles from algorithm to hardware implementation at a lower engineering cost.
- Fine-Grain on-Chip Power Management and Memory Optimization.
- IEEE-754 Floating Point Unit for single and double precision instructions.

Feb 2011 – Aug 2011 **Goma Elettronica SpA (Torino, Italy)**, *Hardware Engineer*.

- Full-custom design of a specialized recording system for aerospace applications. My design won the contract funded by Thales Alenia Space

May 2010 – Oct 2010 **VLSI Laboratory**, *Politecnico di Torino*, Torino (Italy).

- Design of a process-variations-aware core with variable latency units.
- Power driven optimization of a microprocessor.

Education

Sep 2011 – May 2017 **PhD in Computer Science**, *Columbia University*, New York (NY).
PhD awarded on Oct. 2017 with 4.2 GPA.

Sep 2008 – Nov 2010 **MS in Electronic Engineering**, *Politecnico di Torino*, Torino (Italy).
Graduated with honors.

Sep 2005 – Jul 2008 **BS in Electronic Engineering**, *Università di Bologna*, Bologna (Italy).
Graduated with honors.

Languages and Tools

Hardware	SystemC, SystemVerilog, VHDL, Verilog	Software	C/C++, Python, Bash, Tcl, Git, Make
Simulators	Mentor Graphics Modelsim and Questa Formal, Cadence Incisive, Synopsys VCS		
EDA tools	Cadence CtoS and Stratus, Synopsys Design Compiler, Xilinx Vivado and Vivado HLS		

Selected Publications

[1] Davide Giri, Kuan-Lin Chiu, Guy Eichler, Paolo Mantovani, and Luca P. Carloni. Accelerator integration for open-source soc design. *IEEE Micro (Special Issue: FPGAs in Computing)*, 2021.

[2] Paolo Mantovani, Davide Giri, Giuseppe Di Guglielmo, Luca Piccolboni, Joseph Zuckerman, Emilio G. Cota, Michele Petracca, Christian Pilato, and Luca P. Carloni. Agile SoC Development with Open ESP. In *International Conference on Computer-Aided Design (ICCAD)*, 2020.

[3] Paolo Mantovani, Robert Margelli, Davide Giri, and Luca P. Carloni. HL5: A 32-bit RISC-V Processor Designed with High-Level Synthesis. In *Custom Integrated Circuits Conference (CICC)*, 2020.

[4] Davide Giri, Kuan-lin Chiu, Giuseppe Di Guglielmo, Paolo Mantovani, and Luca P. Carloni. Esp4ml: Platform-based design of systems-on-chip for embedded machine learning. In *Conference on Design, Automation and Test in Europe, DATE*, March 2020.

[5] Luca P. Carloni, Emilio G. Cota, Giuseppe Di Guglielmo, Davide Giri, Jihye Kwon, Paolo Mantovani, Luca Piccolboni, and Michele Petracca. Teaching heterogeneous computing with system-level design methods. In *Workshop on Computer Architecture Education*, WCAE'19, pages 4:1–4:8. ACM, 2019.

[6] Davide Giri, Paolo Mantovani, and Luca P. Carloni. Accelerators and coherence: An soc perspective. *IEEE Micro*, 38(6):36–45, Nov 2018.

[7] Davide Giri, Paolo Mantovani, and Luca P. Carloni. Noc-based support of heterogeneous cache-coherence models for accelerators. In *International Symposium on Networks-on-Chip*, NOCS, 2018.

[8] Young Jin Yoon, Paolo Mantovani, and Luca P. Carloni. System-level design of networks-on-chip for systems-on-chip. In *International Symposium on Networks-on-Chip*, NOCS, 2017.

[9] Luca Piccolboni, Paolo Mantovani, Giuseppe Di Guglielmo, and Luca P. Carloni. Cosmos: Coordination of high-level synthesis and memory optimization for hardware accelerators. *ACM Transactions on Embedded Computing Systems*, 16(5s):150, 2017.

[10] Luca Piccolboni, Paolo Mantovani, Giuseppe Di Guglielmo, and Luca P. Carloni. COSMOS: Coordination of high-level synthesis and memory optimization for hardware accelerators. In *International Conference on Hardware/Software Codesign and System Synthesis*, CODES, 2017.

[11] Christian Pilato, Paolo Mantovani, Giuseppe Di Guglielmo, and Luca P. Carloni. System-level optimization of accelerator local memory for heterogeneous systems-on-chip. *IEEE Transactions on Computer-Aided Design*, 36, 2017.

[12] Paolo Mantovani, Emilio G. Cota, Christian Pilato, Giuseppe Di Guglielmo, and Luca P. Carloni. Handling large data sets for high-performance embedded applications in heterogeneous systems-on-chip. In *International Conference on Compilers, Architectures and Synthesis for Embedded Systems*, CASES, 2016.

[13] Paolo Mantovani, Emilio G. Cota, Kevin Tien, Christian Pilato, Giuseppe Di Guglielmo, Ken Shepard, and Luca P. Carloni. An fpga-based infrastructure for fine-grained dvfs analysis in high-performance embedded systems. In *Design Automation Conference*, DAC, 2016.

[14] Paolo Mantovani, Giuseppe Di Guglielmo, and Luca P. Carloni. High-level synthesis of accelerators in embedded scalable platforms. In *Asia and South Pacific Design Automation Conference*, ASP-DAC, 2016.

[15] Emilio G Cota, Paolo Mantovani, Giuseppe Di Guglielmo, and Luca P. Carloni. An analysis of accelerator coupling in heterogeneous architectures. In *Design Automation Conference*, DAC, 2015.

[16] Emilio G. Cota, Paolo Mantovani, Michele Petracca, Mario R. Casu, and Luca P. Carloni. Accelerator memory reuse in the dark silicon era. *Computer Architecture Letters*, 2014.