# NSF Funds Prof. Nowick's Research of On-Chip Networks



Computer Science Professor Steven Nowick (http://www.cs.columbia.edu/%7Enowick/) has won a National Science Foundation (NSF) grant for his research to develop low-power and high-performance interconnection networks-on-chips (NoCs), which will result in significant improvements in the way that diverse processors, memories, and other components on a chip communicate.

These NoCs have benefits for a wide variety of applications, including multimedia processors for graphics and imaging; embedded systems for automobiles, digital cameras, and aerospace; and high-performance, general-purpose parallel computers.

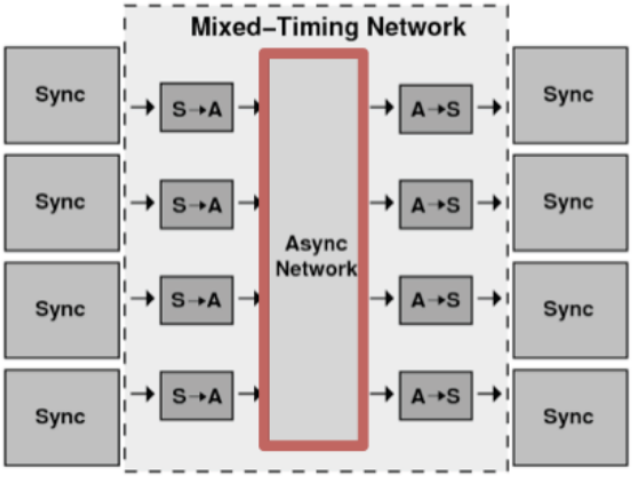
Conventional computer systems use a central clock that coordinates the flow of data that is keyed to the slowest component. Eliminating the clock allows each digital component to operate independently, at its own optimal speed.

"NoCs are used to organize complex chips, forming a regular interconnection network for components, processors and memories to communicate and pass information and computation," Nowick says. "The lack of a central, fixed-rate clock allows much lower overall system power and higher performance."

Nowick says the $450,000 NSF grant will enable him to develop a new generation of NoCs using clockless (i.e., asynchronous) digital components.

This new class of dynamically-adaptable on-chip digital networks will continually customize their operation to actual, observed communication traffic patterns. "Effectively," says Nowick, "the new NoCs will dynamically reconfigure themselves, on the fly, customized to the actual communication traffic."

The diagram below illustrates work underway by Professor Steven Nowick, right, developing clockless on-chip networks to ease assembly of complex digital systems.




Asynchronous on-chip network integrating synchronous components

The asynchronous communication fabric will also provide a flexible skeleton that has the ability to integrate diverse synchronous components operating at different clock rates (see illustration, right). In addition, the asynchronous on-chip network promises much greater tolerance of design variability and timing unpredictability, which are becoming critical challenges in advanced silicon technologies.

Nowick, who also chairs the Computer Engineering Program and has a joint appointment in the Department of Electrical Engineering, anticipates that this work will play a key role in advancing a paradigm shift in organizing complex systems, through the use of asynchrony, and that it will provide a new level of advancement to breaking through current bottlenecks in designing NoCs to organize complex digital systems.

*—Story by Jeff Ballinger (mailto:jlb2180@columbia.edu)*

**Posted:** Jun 29 2012

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