STEVEN MARK NOWICK

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RESEARCH INTERESTS

Asynchronous and Mixed Synchronous/Asynchronous Circuits, Computer-Aided Digital Design, Logic Synthesis, Low-Power and High-Performance Digital Systems, Parallel Processing.

PERSONAL INFORMATION

Date of birth: March 28, 1954
Citizenship: U.S.A.

EDUCATION

Stanford University, Stanford, CA.
Ph.D., Computer Science, March 1993.
Thesis Title: "Automatic Synthesis of Burst-Mode Asynchronous Controllers."
Thesis Advisor: David L. Dill

Columbia University, New York, NY.
Non-degree Computer Science program (1984-86).

Columbia University, New York, NY.
M.A., Music Composition, 1979.

Yale University, New Haven, CT.
B.A., Music, 1976, *magna cum laude*, with departmental honors.

EXPERIENCE

Computer Engineering Program, Columbia University.
Chair, July 2008 – .

Department of Computer Science, Columbia University.
Full Professor, March 2008 – present.

Computer Engineering Program, Columbia University.
Acting Chair, Jan 2000 – June 2000.

Department of Computer Science, Columbia University.
Associate Professor, July 1998 – March 2008.

Department of Computer Science, Columbia University.
Assistant Professor, January 1993 – June 1998.

Department of Computer Science, Stanford University.
Research Assistant, September 1986 – December 1992.

Hewlett-Packard Laboratories, Palo Alto, CA.
Researcher/Intern, Summers 1989, 1990.

Ford Aerospace, Western Development Laboratories, Palo Alto, CA.
Software Engineer, Summer 1987.

AWARDS AND HONORS

Best Paper Award
6th IEEE Async Symposium
(IEEE Int. Symp. on Advanced Research in Async. Circuits and Systems)
IEEE Computer Society; Eilat, Israel 2000.

Best Paper Award
Asynchronous circuits and systems mini-track
26th Hawaii International Conference on System Sciences
IEEE Computer Society; Maui, HI 1993.

Best Paper Award
Computer-Aided Design track
International Conference on Computer Design
IEEE Computer Society; Cambridge, MA 1991.

Best Paper Finalist (2 papers)
14th IEEE "Async" Symposium
(International Symposium on Asynchronous Circuits and Systems)
IEEE Computer Society; Newcastle-upon-Tyne, UK 2008.

Best Paper Finalist
9th IEEE "Async" Symposium
(International Symposium on Asynchronous Circuits and Systems)
IEEE Computer Society; Vancouver, BC, Canada 2003.

Best Paper Finalist
8th IEEE "Async" Symposium
(International Symposium on Asynchronous Circuits and Systems)
IEEE Computer Society; Manchester, UK 2002.

Best Paper Finalist
4th IEEE "Async" Symposium
(International Symposium on Advanced Research in Asynchronous Circuits and Systems)
IEEE Computer Society; La Jolla, CA 1998.

Invited Panelist: "Making the Most of Your CAREER Award"
1st NSF CAREER Program PI Meeting
Plenary Session, CISE Division
National Science Foundation, Arlington, VA 1999.

NSF Faculty Early Career Development ("CAREER") Award
Design Automation Program (formerly: Design, Tools and Test)
National Science Foundation, Arlington, VA, 1995.

Alfred P. Sloan Research Fellowship
Alfred P. Sloan Foundation, New York, NY, 1995.

NSF Research Initiation Award ("RIA")
Design Automation Program (formerly: Design, Tools and Test)
National Science Foundation, Arlington, VA, 1993.

RESEARCH SUPPORT

NSF proposal: "CSR-PSCE-T: Using Asynchrony to Enable Scalable and Resilient On-Chip Interconnection Networks for Chip Multiprocessors". PI: S. Nowick, co-PI's: L. Carloni, S. Sethumadhavan. Submitted 4/23/08 (*pending*): $1,500,000.

NSF proposal: "CPA-DA-T: Design and Tools for Easy-to-Program Massively Parallel On-Chip Systems: Deriving Scalability Through Asynchrony," PI: S. Nowick, co-PI: U. Vishkin (U. of Maryland). NSF Award No. CCF-0811504 (8/1/08-7/31/12): $921,686.

> *This award was one of only two large-scale "team" proposals awarded by NSF under the "Design Automation for Micro and Nano Systems" topical area for this CPA solicitation.* The goal of this proposal is to develop a first-of-its-kind partly-asynchronous/partly-synchronous high-end massively-parallel-on chip computer. In particular, a high-speed, low-power asynchronous communication fabric will be developed, to connect synchronous processors, and which is robust and flexible in the presence of timing variability and multiple clock rates and supports a 'plug-and-play' assembly of low-power complex parallel processors.

Initiatives in Science and Engineering (ISE) Grant, Columbia University, Office of the Executive Vice President of Research: "Designing a Flexible, High-Throughput Asynchronous Interconnect Fabric for Future Single-Chip Parallel Processors," (7/1/06-6/30/08): $185,530.

> *This competitive internal award, from the executive vice president of research at Columbia University, is for proposals which "test unusually creative ideas" that are "in too early a stage of data gathering to be viable for the usual funding agencies.*"

DARPA "CLASS" Project. I was brought onto this major multi-institution contract officially in Fall-05. The project currently extends to *March 2007*. **Funding award** for Nowick: **$502,000**.

> *This DARPA program is the largest US government research program for asynchronous digital design in the last 30 years.* Its goal

is to make asynchronous digital design viable for the commercial and military sectors. There were **approximately 20 large-scale proposals submitted,** and **only 1 contract funded,** headed by *Boeing* (PI), with participation of *Philips Semiconductors* (via its incubated asynchronous startup, called *Handshake Solutions*, two asynchronous startups and two smaller academic efforts. (This startup has been recently ranked one of the "top 50 startups to watch" by EE Times.)

The two goals of the project are: (i) building a large-scale asynchronous demonstration chip (for Boeing military applications), and compare its performance and cost to an equivalent synchronous chip; and (ii) provide a "legacy asynchronous CAD tool" for future asynchronous designs. **Total Contract: $14 million.**

I have been brought onto the project for its Phase 2/3, along with my former PhD student Montek Singh (currently an assistant professor at UNC), to play a key participating role in (a) *developing CAD tools* for designing asynchronous circuits for the project, and (b) *transferring my high-speed patented asynchronous circuit technology*, i.e. "Mousetrap" pipelines, into these tools. My *Columbia-patented* **Mousetrap** high-speed asynchronous pipeline circuits have already been incorporated into the Philips' asynchronous CAD tool being developed for the project. Some of them are being applied to the Boeing demo chip for the project. In addition, several CAD optimizations I have developed are being incorporated into an alternative "low-power" CAD tool developed through a Florida startup company, *Theseus Logic*.

Supplement to NSF ITR award: awarded summer 2003, for support of minority student development and research (Melinda Agyekum, female/African-American MS student, working with me on research on asynchronous digital design): $48,932.

NYS Microelectronics Design Center (MDC) Grant: "Design Techniques for Compressed Code Embedded Processors", (7/1/02-6/30/03): $20K.

NYS Microelectronics Design Center (MDC) Grant: "Dynamically-Adaptive Asynchronous Digital Systems", (7/1/01-6/30/02): $30K.

NSF medium-scale ITR award: "A CAD Framework for the Design and Optimization of Large-Scale Asynchronous Digital Systems". PI: S. Nowick (joint proposal with University of Southern California). NSF Award No. CCR-00-86036 (9/1/00-8/31/05): $1,612,809.

NSF medium-scale ITR award: "Asynchronous Digital Signal Processing for the Software Radio". co-PI: S. Nowick (joint proposal with Prof. Ken Shepard, EE Department). NSF Award No. CCR-00-86007 (9/1/00-8/31/03): $969,227.

Note: In 2000, only *62 medium-scale ITR awards were granted, out of 920 submitted proposals,* across all areas of information technol-

ogy. I was 1 of only 4 investigators nationally in 2000 to receive 2 medium-scale NSF ITR awards. (The ITR initiative is an outgrowth of President Clinton's *PITAC* advisory committee for national information technology, to fund "long-term risk-taking research".)

NSF Grant: "Methodologies and CAD Tools for the Design of Asynchronous Systems," PI: S. Nowick. NSF Award No. CCR-99-88241 (11/15/00-10/31/03): $200,895.

NYS Center for Advanced Technology (CAT): "The Design of Multi-Gigahertz Asynchronous Arithmetic Circuits for High-Speed Digital Signal Processing". PI: S. Nowick. *Award date:* July 10, 2000. Total: $70,000.

Sun Microsystems Gift: Research on Asynchronous Design. PI: S. Nowick. (4/00-4/00/01): $30,000.

NSF Research Experiences for Undergraduates *(REU)*, supplement to NSF Award No. CCR-97-34803 (6/1/99-8/31/99): $5,000.

Columbia University Seed Grant: "The Design of a Fast Hardware Accelerator for Genome Database Searches," PI: S. Nowick. Joint funding by (i) Office of the Vice Provost, Strategic Initiative Fund ($30,000), and (ii) Dean of the School of Engineering and Applied Science ($15,000) (9/98-8/99): $45,000.

NSF Grant: "High-Performance and Low-Power Asynchronous Datapaths: Design and Applications," PI: S. Nowick. NSF Award No. CCR-97-34803 (7/15/98-6/30/01): $335,000.

Supplement to NSF CAREER Award, funding for CAD software tool development. NSF Award No. MIP-9501880, Proposal MIP-9840302 (1/1/98-8/31/98): $20,763.

NSF Faculty Early Career Development (CAREER) Award, "Testability and Sequential Optimization of Asynchronous State Machines," NSF Award No. MIP-9501880 (9/1/95-8/31/98): $120,000.

Alfred P. Sloan Research Fellowship, Alfred P. Sloan Foundation, New York, NY (9/16/95-9/15/97): $30,000.

Grant for Joint Research in Asynchronous Design, IBM Corporation, T.J. Watson Research Center (2/95-1/96): $40,000.

NSF Grant: "Advanced Research in Asynchronous Circuits and Systems," NSF Award No. MIP-9406532 (11/94-7/95). PI: Erik Brunvand; co-PIs: Ganesh Gopalakrishnan, Steven M. Nowick. Grant to establish a new international symposium on asynchronous circuit design (held in Salt Lake City, Utah, November 1994). Total Budget: $12,320.

NSF Research Initiation Award (RIA), "The Design of High-Performance Asynchronous Controllers," NSF Award No. MIP-9308810 (9/93-8/96): $100,000.

NSF Research Experiences for Undergraduates *(REU)*, supplement to NSF RIA award (6/93-8/93): $5,000.

PATENTS

1. *Low Latency FIFO Circuit for Mixed Clock Systems,* Tiberiu Chelcea, Steven M. Nowick. **U.S. Patent #7,197,582** (March 27, 2007).
2. *Circuits and Methods for High-Capacity Asynchronous Pipeline Processing,* Montek Singh, Steven M. Nowick. **U.S. Patent #7,053,665** (May 31, 2006). [continuation of #6,867,620]
3. *Asynchronous Pipeline with Latch Controllers,* Montek Singh, Steven M. Nowick. **U.S. Patent #6,958,627** (October 25, 2005).
4. *Circuits and Methods for High-Capacity Asynchronous Pipeline,* Montek Singh, Steven M. Nowick. **U.S. Patent #6,867,620** (March 15, 2005).
5. *Variable-Length, High-Speed Asynchronous Decoder Circuit,*, Steven M. Nowick, Martin Benes, Andrew Wolfe. **U.S. Patent #6,865,668** (March 8, 2005).
6. *Low Latency FIFO Circuits for Mixed Asynchronous and Synchronous Systems,* Tiberiu Chelcea, Steven M. Nowick. **U.S. Patent #6,850,092** (Feb. 1, 2005).
7. *High-Throughput Asynchronous Dynamic Pipelines,* Montek Singh, Steven M. Nowick. **U.S. Patent #6,590,424** (July 8, 2003).
8. *High-Speed Asynchronous Decompression Circuit for Variable-Length Coded Data,* Steven M. Nowick, Martin Benes, Andrew Wolfe. **U.S. Patent #6,408,421** (June 18, 2002).

TECHNOLOGY TRANSFER

1. Asynchronous Controllers: NASA (Goddard Space Center).

In 2006, a manager at NASA/Goddard invited me to collaborate in designing a **prototype asynchronous measurement circuit for space applications,** using my asynchronous burst-mode controllers and Minimalist CAD tool. *The chip was jointly designed in 2006 by my NASA contact and myself, usng my Minimalist and other asynchronous tools.* The first chip has been fabricated (January 2007), and NASA has funded the development of a second chip (to be taped out in Summer 2007). NASA indicates that this work is receiving positive internal interest, and there is a real likelihood of its use by NASA in future space missions.

2. High-Speed Asynchronous Digital Pipelines: Boeing/Philips Semiconductors (DARPA "CLASS" Project).

From 2005-2007, as a participant in the DARPA CLASS project (led by Boeing Corporation – see "Research Support" above), our high-speed asynchronous "Mousetrap" pipelines have been used extensively. Columbia and UNC were

funded to: (a) manually design an experimental pipelined GCD circuit using our Mousetrap asynchronous pipelines; and (b) collaborate with Philips Semiconductors (through its incubated startup company, "Handshake Solutions") to incorporate our Mousetrap pipelines into an experimental version of their commercial asynchronous computer-aided design (CAD) tool flow. Both tasks were successfully completed. Boeing was satisfied with the circuit performance and ease of design in (a), and task (b) demonstrated the feasibility of developing an automated CAD tool flow using our circuits. There is a potential in the future to develop a commercial-strength version of a CAD flow, under direction from Handshake Solutions, which includes our high-speed Mousetrap asynchronous pipleines.

3. High-Speed Asynchronous Digital Pipelines: IBM T.J. Watson Research.

In Summer 2000, researcher from IBM T.J. Watson invited my PhD student, Montek Singh, to transfer our high-speed asynchronous pipeline technology to IBM. Montek spent from August-December 2000, in an IBM group, designing an experimental low-power chip for a pipelined FIR filter. They used our "high-capacity" pipelines, and Montek and the IBM group have reimplemented and taped-out an entire design in modern technology (0.18 micron). (He also designed some plain async FIFO's to calibrate their performance as well.) The chip was evaluated in April-June 2001; it was fully functional, meeting and exceeding basic synchronous performance and power requirements for the next process generation at IBM. In addition, the new design had had the advantage over synchronous ones of dynamically-variable latency, depending on input sample rate.

4. The CaSCADE Asynchronous Tool Framework.

The "CaSCADE" package is a new asynchronous design environment developed at Columbia University (under Steven Nowick) and USC (under Prof. Peter Beerel) ("CaSCADE" = Columbia University and University of Southern California Asynchronous Design Environment.) All the tools are freely available for downloads and use, targeting Linux platforms.

It includes 3 distinct CAD tools from my Columbia group: (i) **MINIMALIST v2.0,** for synthesis and optimization of asynchronous controllers; (ii) **ATN_OPT v0.1,** for synthesis and optimization of robust asynchronous threshold networks; and (iii) **DES Analyzer v0.1,** for performance analysis of concurrent systems.

Minimalist (multiple releases since the late 1990's) has been downloaded to over 100 sites in 18 countries. (For more details on "MINIMALIST", see item #5 below.)

This first release of our ATN_OPT and DES Analyzer tools has already resulted in *19 and 16 downloads* each, respectively (since November 2007). This new release of MINIMALIST has received over 30 downloads.

Each of these tools is available for download from the CaSCADE web page; most come with detailed tutorials and examples, as well installation and set-up

instructions:
(see http://www.cs.columbia.edu/~nowick/asynctools).

5. The MINIMALIST CAD Package. With several of my students, I have developed and released several versions of a large software CAD package for the synthesis of asynchronous controllers, called "MINIMALIST"
(see http://www.cs.columbia.edu/~nowick/asynctools). The most recent release, in November 2007, is version 2.0.

MINIMALIST is a complete package for the synthesis and optimization of high-speed asynchronous controllers. It includes a number of practical features: Verilog output, two-level and multi-level logic optimizers, auto-insertion of initialization circuitry, graphic displays, and a top-to-bottom verifier.

The tool has recently been used at NASA Goddard Space Flight Center (2006-2007) for the design of an experimental asynchronous space measurement chip (see item #1 above).

MINIMALIST has been **downloaded to**, and is currently being used at, over **100 sites in 18 countries**. These include leading universities, such as: *University of Tokyo* (Japan), *Indian Institute of Technology* (India), *Edinburgh University* (UK), *UCLA*, *University of Southern California* and *University of Utah* (USA), *Swiss Federal Institute of Technology* (Switzerland), *Technical University of Denmark* (Denmark), and *University of Athens* (Greece). It has also been downloaded to companies such as *Intel* and *Sun Microsystems*, and an early prototype was transferred to *IBM Corporation*. The package is being evaluated by two startup companies, *Theseus Logic* and *Cogency Technologies*, for possible commercial use. The tool was also **being taught in IIT Bombay** in an asynchronous design class in Spring-02, with over 40 students.

HFMIN, *IMPYMIN*, *Espresso-HF*. These are our individual tools for hazard-free logic minimization, which are widely used as standalone components. They have been incorporated into **academic CAD packages** developed by several other research groups, including the 3D system (Yun et al., UC San Diego), ATACS (Myers et al., University of Utah) and the ACK system (Gopalakrishnan et al., University of Utah).

These minimizers have also been used at a number of **companies.** At *Intel Corporation*, "hfmin" is part of their asynchronous CAD tool suite, where it was used in the design of the experimental high-performance instruction-length decoder chip (mid 1990's). The resulting chip was over 3 times faster than Intel's comparable synchronous version. Our tool was critical for the design of several of the control circuits. At *Hewlett-Packard Laboratories*, it was used in the design of an experimental low-power infrared communications chip, and at *AMD Corporation* in the design of an experimental SCSI controller.

6. High-Speed Asynchronous Datapaths: Sun Microsystems Labs.

Between 1999-2001, the asynchronous research group at Sun Microsystems, headed by Ivan Sutherland, used my *speculative completion* technique to design

a fast asynchronous adder in their experimental FleetZero chip (described in a March 2001 publication at IEEE Async Symposium).

RESEARCH PUBLICATIONS

JOURNAL ARTICLES

Under Review/in Revision/in Preparation:

1. M. Singh, J.A. Tierno, A. Rylyakov, S. Rylov, and S.M. Nowick, "An Adaptively-Pipelined Mixed Synchronous-Asynchronous Digital FIR Filter Chip Operating at 1.3 GigaHertz." Submitted to *IEEE Transactions on VLSI Systems* (April 2008).

2. P. McGee and S.M. Nowick, "Exact Time Separation of Events in Cyclic Concurrent Systems." To be submitted to *IEEE Transactions on Computer-Aided Design* (August 2008).

3. A. Mitra, W.F. McLaughlin and S.M. Nowick, "Efficient Asynchronous Protocol Converters for Two-Phase Delay-Insensitive Global Communication." Submitted to *IEEE Transactions on VLSI Systems* (June 2008).

4. S.M. Nowick and C.W. O'Donnell, "On the Existence of Hazard-free Multi-level Logic." To be submitted to *IEEE Transactions on Computer-Aided Design* (October 2008).

Published:

5. C. Jeong and S.M. Nowick, "Technology Mapping and Cell Merger for Asynchronous Threshold Networks." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 27:4, pp. 659-672 (April 2008).

6. M. Singh and S.M. Nowick, " MOUSETRAP: High-Speed Transition-Signaling Asynchronous Pipelines." *IEEE Transactions on VLSI Systems,* vol. 15:6, pp. 684-698 (June 2007).

7. M. Singh and S.M. Nowick, "The Design of High-Performance Dynamic Asynchronous Pipelines: Lookahead Style." *IEEE Transactions on VLSI Systems,* vol. 15:11, pp. 1256-1269 (November 2007).

8. M. Singh and S.M. Nowick, "The Design of High-Performance Dynamic Asynchronous Pipelines: High-Capacity Style." *IEEE Transactions on VLSI Systems,* vol. 15:11, pp. 1270-1283 (November 2007).

9. T. Chelcea and S.M. Nowick, "Robust Interfaces for Mixed-Timing Systems." *IEEE Transactions on VLSI Systems,* vol. 12:8, pp. 857-873 (August 2004).

10. Y.W. Li, G. Patounakis, K.L. Shepard and S.M. Nowick, "High-Throughput Asynchronous Datapath with Software-Controlled Voltage Scaling." *IEEE Journal of Solid-State Circuits,* vol. 39:4, pp. 704-708, April, 2004.

11. M. Singh and S.M. Nowick, "Synthesis for Logical Initializability of Synchronous Finite State Machines." *IEEE Transactions on VLSI Systems,* vol. 8:5, pp. 542-57 (October 2000).

12. M.B. Josephs, S.M. Nowick and C.H. van Berkel, "Modeling and Design of Asynchronous Circuits" (*invited paper*). *Proceedings of the IEEE,* vol. 87:2, pp. 234–242 (Feb. 1999).

13. C.H. van Berkel, M.B. Josephs and S.M. Nowick, "Scanning the Technology: Applications of Asynchronous Circuits" (*invited paper*). *Proceedings of the IEEE,* vol. 87:2, pp. 223–233 (Feb. 1999).

14. M. Theobald and S.M. Nowick, "Fast Heuristic and Exact Algorithms for Two-Level Hazard-Free Logic Minimization." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 17:11, pp. 1130-1147 (Nov. 1998).

15. L.A. Plana and S.M. Nowick, "Architectural Optimization for Low-Power Non-Pipelined Asynchronous Systems." *IEEE Transactions on VLSI Systems,* vol. 6:1, pp. 56-64 (March 1998).

16. S.M. Nowick, N.K. Jha and Fu-Chiung Cheng, "Synthesis of Asynchronous Circuits for Stuck-at and Robust Path Delay Fault Testability." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 16:12, pp. 1514-1521 (Dec. 1997).

17. S.M. Nowick, "Design of a Low-Latency Asynchronous Adder Using Speculative Completion." *IEE Proceedings – Computers and Digital Techniques,* vol. 143:5, pp. 301-307 (Sept. 1996).

18. S.M. Nowick and D.L. Dill, "Exact Two-Level Minimization of Hazard-Free Logic with Multiple-Input Changes." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 14:8, pp. 986-997 (Aug. 1995).

19. G. Gopalakrishnan, E. Brunvand, N. Michell and S.M. Nowick. "A Correctness Criterion for Asynchronous Circuit Validation and Optimization." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 13:11, pp. 1309-1318 (Nov. 1994).

20. S.M. Nowick, M.E. Dean, D.L. Dill and M. Horowitz, "The Design of a High-Performance Cache Controller: a Case Study in Asynchronous Synthesis." *Integration: the VLSI Journal,* vol. 15:3, pp. 241-262 (Oct. 1993).

21. D.L. Dill, S.M. Nowick and R.F. Sproull, "Specification and Automatic Verification of Self-Timed Queues." *Formal Methods in System Design,* vol. 1:1, pp. 29-60 (July 1992).

CONFERENCE PAPERS (published, fully refereed)

Submitted:

22. P.B. McGee and S.M. Nowick, "Harmonic Analysis of Concurrent Systems in Max-Plus Algebra." To be submitted to a conference (Fall-08).

Published:

23. P.B. McGee, M.Y. Agyekum, M.A. Mohamed and S.M. Nowick, "A Level-Encoded Transition Signaling Protocol for High-Throughput Asynchronous Global Communication." **Best Paper Finalist.** In *IEEE International Symposium on Asynchronous Circuits and Systems (Async-08),* Newcastle, UK (April 2008).

24. C. Jeong and S.M. Nowick, "Optimization for Timing-Robust Asynchronous Circuits Based on Eager Evaluation." **Best Paper Finalist.** In *IEEE International Symposium on Asynchronous Circuits and Systems (Async-08),* Newcastle, UK (April 2008).

25. P.B. McGee and S.M. Nowick, "An Efficient Algorithm for Time Separation of Events in Concurrent Systems." In *IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* San Jose, CA (November 2007).

26. A. Mitra, W.F. McLaughlin and S.M. Nowick, "Efficient Asynchronous Protocol Converters for Two-Phase Delay-Insensitive Global Communication." In *IEEE Int. Symp. on Asynchronous Circuits and Systems (Async-07),* Berkeley, CA (March 2007).

27. M. Agyekum and S.M. Nowick, "A Cycle-Based Decomposition Method for Burst-Mode Asynchronous Controllers." In *IEEE Int. Symp. on Asynchronous Circuits and Systems (Async-07),* Berkeley, CA (March 2007).

28. C. Jeong and S.M. Nowick, "Optimization of Robust Asynchronous Circuits by Local Input Completeness Relaxation." In *IEEE Asia and South-Pacific Design Automation Conference (ASPDAC-07),* Yokohama, Japan (Jan. 2007)

29. C. Jeong and S.M. Nowick, "Optimal Technology Mapping and Cell Merger for Asynchronous Threshold Networks", In *IEEE Int. Symp. on Asynchronous Circuits and Systems (Async-06),* Grenoble, France (March 2006).

30. F. Shi, Y. Makris, S.M. Nowick, and M. Singh, "Test Generation for Ultra-High-Speed Asynchronous Pipelines." In the *International Test Conference (ITC),* (Oct. 2005).

31. P.B. McGee and S.M. Nowick, "Efficient Performance Analysis of Asynchronous Systems Based on Periodicity." In the *IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS),* Jersey City, NJ (Sept. 2005).

32. P.B. McGee and S.M. Nowick, "A Lattice-Based Framework for the Classification and Design of Asynchronous Pipelines." In *DAC: ACM/IEEE Design Automation Conference,* Anaheim, CA (June 2005).

33. C. Jeong and S.M. Nowick, "Fast Hazard Detection in Combinational Circuits." In *DAC: ACM/IEEE Design Automation Conference,* San Diego, CA (June 2004).

34. S.M. Nowick and C.W. O'Donnell, "On the Existence of Hazard-free Multi-level Logic." *Async: IEEE International Symposium on Asynchronous Circuits and Systems,* Vancouver, BC, Canada (May 2003).

35. Y.W. Li, G. Patounakis, A. Jose, K.L. Shepard and S.M. Nowick, "Asynchronous Datapath with Software-Controlled On-Chip Adaptive Voltage Scaling for Multirate Signal Processing Applications." **Best Paper Finalist.** *Async: IEEE International Symposium on Asynchronous Circuits and Systems,* Vancouver, BC, Canada (May 2003).

36. T. Chelcea and S.M. Nowick, "Resynthesis and Peephole Transformations for the Optimization of Large-Scale Asynchronous Systems." *DAC: IEEE/ACM Design Automation Conference,* New Orleans, LA (June 2002).

37. M. Singh, J.A. Tierno, A. Rylyakov, S. Rylov, and S.M. Nowick, "An Adaptively-Pipelined Mixed Synchronous-Asynchronous Digital FIR Filter Chip Operating at 1.3 GigaHertz." **Best Paper Finalist.** *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* Manchester, UK (April 2002).

38. T. Chelcea, A. Bardsley, D. Edwards, S.M. Nowick, "A Burst-Mode Oriented Back-End for the Balsa

Synthesis System." *DATE: Proceedings of the Design, Automation and Test in Europe Conference,* Paris, France (March 2002).

39. R. Ozdag, M. Singh, P.A. Beerel, S.M. Nowick, "High-Speed Non-Linear Asynchronous Pipelines." *DATE: Proceedings of the Design, Automation and Test in Europe Conference,* Paris, France (March 2002).

40. J. Tierno, A. Rylyakov, S. Rylov, M. Singh, P. Aspadu, S.M. Nowick, M. Immediato, and S. Gowda, "A 1.3 GSample/s 10-tap Full-rate Variable-Latency Self-timed FIR with Clocked Interfaces." *ISSCC: International Solid State Circuits Conference,* Monterey, CA (February 2002).

41. M. Singh and S.M. Nowick, " MOUSETRAP: Ultra-High-Speed Transition-Signaling Asynchronous Pipelines." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Austin, TX (Sept. 2001).

42. M. Theobald and S.M. Nowick, "Transformations for the Synthesis and Optimization of Asynchronous Distributed Control." *DAC: Proceedings of the 38rd IEEE/ACM Design Automation Conference,* Las Vegas, NV (June 2001).

43. T. Chelcea and S.M. Nowick, "Robust Interfaces for Mixed-Timing Systems with Application to Latency-Insensitive Protocols." *DAC: Proceedings of the 38rd IEEE/ACM Design Automation Conference,* Las Vegas, NV (June 2001).

44. T. Chelcea and S.M. Nowick, "Low-Latency FIFO's for Mixed-Clock Systems." *WVLSI: Proceedings of the IEEE Computer Society Annual Workshop on VLSI,* Orlando, FL (April 2000).

45. M. Singh and S.M. Nowick, "Fine-Grain Pipelined Asynchronous Adders for High-Speed DSP Applications." *WVLSI: Proceedings of the IEEE Computer Society Annual Workshop on VLSI,* Orlando, FL (April 2000).

46. M. Singh and S.M. Nowick, "High-Throughput Asynchronous Pipelines for Fine-Grain Dynamic Datapaths." **Best Paper Award.** *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* Eilat, Israel (April 2000).

47. T. Chelcea and S.M. Nowick, "Low-Latency Asynchronous FIFO's using Token Rings." *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* Eilat, Israel (April 2000).

48. R.M. Fuhrer and S.M. Nowick, "OPTIMISTA: State Minimization of Asynchronous FSMs for Optimum Output Logic." *ICCAD: Proceedings of the IEEE International Conference on Computer-Aided Design,* San Jose, CA (Nov. 1999).

49. M. Benes, S.M. Nowick and A. Wolfe, "A Fast Asynchronous Huffman Decoder for Compressed-Code Embedded Processors." *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* San Diego, CA, pp. 43–56 (April 1998).

50. M. Theobald and S.M. Nowick, "An Implicit Method for Hazard-Free Two-Level Logic Minimization." **Best Paper Finalist.** *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* San Diego, CA, pp. 58–69 (April 1998).

51. R.M. Fuhrer and S.M. Nowick, "OPTIMIST: State Minimization for Optimal 2-Level Logic Implementation." *ICCAD: Proceedings of the IEEE/ACM International Conference on Computer-Aided Design,* San Jose, CA, pp. 308–315 (Nov. 1997).

52. M. Benes, A. Wolfe and S.M. Nowick, "A High-Speed Asynchronous Decompression Circuit for Embedded Processors." *ARVLSI: Proceedings of the 17th Conference on Advanced Research in VLSI,* Ann Arbor, Michigan, pp. 219-236 (March 1997).

53. S.M. Nowick, K.Y. Yun, P.A. Beerel and A.E. Dooply, "Speculative Completion for the Design of High-Performance Asynchronous Dynamic Adders." *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* Eindhoven, Netherlands, pp. 210–223 (March 1997).

54. S.M. Nowick and M. Theobald, "Synthesis of Low-Power Asynchronous Circuits in a Specified Environment." *ISLPED: IEEE International Symposium on Low Power Electronics and Design,* Monterey, CA, pp. 92–95 (March 1997).

55. M. Singh and S.M. Nowick, "Synthesis for Logical Initializability of Synchronous Finite State Machines." *Proceedings of the 10th International Conference on VLSI Design,* Hyderabad, India, pp. 76–80 (January 1997).

56. M. Singh and S.M. Nowick, "Synthesis-for-Initializability of Asynchronous Sequential Machines." *ITC: Proceedings of the IEEE International Test Conference,* Washington, DC, pp. 232–241 (Oct. 1996).

57. L.A. Plana and S.M. Nowick, "Concurrency-Oriented Optimization for Low-Power Asynchronous Systems." *ISLPED: IEEE International Symposium on Low Power Electronics and Design,* Monterey, CA, pp. 151–156 (Aug. 1996).

58. S.M. Nowick, M. Theobald and T. Wu, "Espresso-HF: A Heuristic Hazard-Free Minimizer for Two-Level Logic." *DAC: Proceedings of the 33rd IEEE/ACM Design Automation Conference,* Las Vegas, NV, pp. 71–76 (June 1996).

59. P. Kudva, G. Gopalakrishnan, H. Jacobson and S.M. Nowick, "Synthesis of Hazard-Free Customized CMOS Complex-Gate Networks Under Multiple-Input Changes." *DAC: Proceedings of the 33rd IEEE/ACM Design Automation Conference,* Las Vegas, NV, pp. 77–82 (June 1996).

60. P.A. Beerel, K.Y. Yun, S.M. Nowick and P. Yeh, "Estimation and Bounding of Energy Consumption in Burst-Mode Control Circuits." *ICCAD: IEEE/ACM International Conference on Computer-Aided Design,* San Jose, CA, pp. 26–33 (Nov. 1995).

61. R.M. Fuhrer, B. Lin and S.M. Nowick, "Symbolic Hazard-Free Minimization and Encoding of Asynchronous Finite State Machines." *ICCAD: Proceedings of the IEEE/ACM International Conference on Computer-Aided Design,* San Jose, CA, pp. 604–611 (Nov. 1995).

62. R.M. Fuhrer, B. Lin and S.M. Nowick, "Algorithms for the Optimal State Assignment of Asynchronous State Machines." *ARVLSI: Proceedings of the 16th Conference on Advanced Research in VLSI,* Chapel Hill, NC, pp. 59–75 (March 1995).

63. S.M. Nowick, N.K. Jha and F.-C. Cheng, "Synthesis of Asynchronous Circuits for Stuck-at and Robust Path Delay Fault Testability." *Proceedings of the 8th International Conference on VLSI Design,* New Delhi, India, pp. 171–176 (Jan. 1995).

64. S.M. Nowick and B. Coates, "UCLOCK: Automated Design of High-Performance Unclocked State Machines." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 434-441 (Oct. 1994).

65. K.Y. Yun, D.L. Dill and S.M. Nowick, "Practical Generalizations of Asynchronous State Machines." *EDAC: Proceedings of the European Conference on Design Automation,* Paris, France, pp. 525–530 (Jan. 1993).

66. S.M. Nowick, M.E. Dean, D.L. Dill and M. Horowitz, "The Design of a High-Performance Cache Controller: a Case Study in Asynchronous Synthesis." **Best Paper Award,** Asynchronous Circuits and Systems Minitrack/ **Best Paper Finalist,** Architecture Track. *HICSS: Proceedings of the IEEE Hawaii International Conference on System Sciences, vol. I* Maui, HI, pp. 419–427 (Jan. 1993).

67. S.M. Nowick and D.L. Dill, "Exact Two-Level Minimization of Hazard-Free Logic with Multiple-Input Changes." *ICCAD: Proceedings of the IEEE/ACM International Conference on Computer-Aided Design,* Santa Clara, CA, pp. 626–630 (Nov. 1992).

68. S.M. Nowick, K.Y. Yun and D.L. Dill, "Practical Asynchronous Controller Design." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 341–345 (Oct. 1992).

69. K.Y. Yun, D.L. Dill and S.M. Nowick, "Synthesis of 3D Asynchronous State Machines." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 346–350 (Oct. 1992).

70. S.M. Nowick and D.L. Dill, "Automatic Synthesis of Locally-Clocked Asynchronous State Machines." *ICCAD: Proceedings of the IEEE International Conference on Computer-Aided Design,* Santa Clara, CA, pp. 318–321 (Nov. 1991).

71. S.M. Nowick and D.L. Dill, "Synthesis of Asynchronous State Machines Using a Local Clock." **Best Paper Award,** CAD track. *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 192–197 (Oct. 1991).

72. S.M. Nowick and D.L. Dill, "Practicality of State-Machine Verification of Speed-Independent Circuits." *ICCAD: Proceedings of the IEEE International Conference on Computer-Aided Design,* Santa Clara, CA, pp. 266–269 (Nov. 1989).

73. D.L. Dill, S.M. Nowick and R.F. Sproull, "Automatic Verification of Speed-Independent Circuits with Petri Net Specifications." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 212–216 (Oct. 1989).

INVITED CONFERENCE PAPERS (published, not refereed)

74. E. Brunvand, S.M. Nowick and K.Y. Yun, "Practical Advances in Asynchronous Design and Asynchronous/Synchronous Interfaces." Invited survey article. *DAC: Proceedings of the 36th ACM/IEEE Design Automation Conference,* New Orleans, LA (June 1999).

75. E. Brunvand, S.M. Nowick and K.Y. Yun, "Practical Advances in Asynchronous Design." Invited survey article. *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Austin, Texas, pp. 662-668 (Oct. 1997).

BOOKS

76. R.M. Fuhrer and S.M. Nowick, *Sequential Optimization of Asynchronous and Synchronous Finite-State Machines: Algorithms and Tools,* Kluwer Academic Publishers, Boston, MA (2001). ISBN 0-7923-7425-8.

BOOK CONTRIBUTIONS (published)

77. L. Lavagno and S.M. Nowick, "Asynchronous Control Circuits." Chapter 10 of *Logic Synthesis and Verification,* (S. Hassoun and T. Sasao, eds.), Kluwer Academic, Boston, MA (pp. 255-284).

78. A. Davis and S.M. Nowick, "An Introduction to Asynchronous Circuit Design." Chapter in *The Encyclopedia of Computer Science and Technology,* vol. 38 (A. Kent and J.G. Williams, eds.), Marcel Dekker, New York (February 1998).

79. A.L. Davis and S.M. Nowick, "Asynchronous Circuit Design: Motivation, Background and Methods." Chapter in *Asynchronous Digital Circuit Design,* G. Birtwistle and A. Davis editors, Springer-Verlag (Workshops in Computing Series, 1995), pp. 1-49.

80. D.L. Dill, S.M. Nowick and R.F. Sproull, "Specification and Automatic Verification of Self-Timed Queues." Chapter in *Formal Verification of Hardware Design (IEEE Tutorial Series),* M. Yoeli editor (Computer Science Press of IEEE, 1991). (Originally appeared as Stanford University Technical Report, Computer Systems Laboratory, CSL-TR-89-387, August 1989.)

81. S.M. Nowick and D.L. Dill, "Automatic Verification." Chapter in *Synchronization Design for Digital Systems,* T. H.-Y. Meng, Kluwer Academic (1990).

WORKSHOP PAPERS (fully refereed, limited distribution in workshop proceedings)

82. C. Jeong and S.M. Nowick, "Optimization for Timing-Robust Asynchronous Circuits Based on Eager Evaluation." Presentation in the *ACM/IEEE International Workshop on Logic and Synthesis (IWLS-07),* San Diego, CA (June 2007).

83. C. Jeong and S.M. Nowick, "Technology Mapping for Robust Asynchronous Threshold Networks", Presentation in *ACM Workshop on Timing Issues (TAU-06),* (Feb. 2006) (and full-length paper included in non-published workshop proceedings).

84. C.-H. Li and S.M. Nowick, "An Architecture-Oriented Approach to Code Compression for Embedded Processors." Presentation in *IEEE Workshop on Application-Specific Processors (WASP-05),* (Sept. 22, 2005), affiliated with CODES-05 symposium (and full-length paper included in non-published workshop proceedings).

85. P.B. McGee and S.M. Nowick, "A Unified Lattice-Based Framework for the Classification and Design of Asynchronous Pipelines." Presented at *ACM/SIGDA Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU),* San Francisco, CA (Feb.-Mar. 2005).

86. T. Chelcea and S.M. Nowick, "Resynthesis and Peephole Transformations for the Optimization of Large-Scale Asynchronous Systems." *IWLS: IEEE/ACM International Workshop on Logic and Synthesis,* poster presentation. New Orleans, LA (June 2002).

87. S.M. Nowick, "A Burst-Mode Oriented Back-End for the Balsa Synthesis System." Presented at the *2nd ACiD-WG Workshop (5th funding framework), of the European Community*, Munich, Germany (Jan. 2002).

88. M. Singh and S.M. Nowick, "MOUSETRAP: Ultra-High-Speed Transition-Signaling Asynchronous Pipelines." Presented at *ACM/SIGDA Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU),* Austin, TX (Dec. 2000).

89. M. Theobald and S.M. Nowick, "Control Synthesis and Optimization of Asynchronous Systems Through Transformations." Presented at *ACM International Workshop on Logic Synthesis (IWLS),* Dana Point, CA (May 31-June 2, 2000).

90. R.M. Fuhrer, S.M. Nowick, M. Theobald, N.K. Jha, and L. Plana, "MINIMALIST: An Environment for the Synthesis and Verification of Burst-Mode Asynchronous Machines." Poster presentation at *International Workshop on Logic Synthesis (IWLS),* Lake Tahoe, CA (June 1998).

91. R.M. Fuhrer and S.M. Nowick, "Exact Optimal State Minimization for 2-Level Output Logic." Presented at *International Workshop on Logic Synthesis (IWLS),* Lake Tahoe, CA (June 1998).

92. M. Singh and S.M. Nowick, "State Assignment for Initializability of Synchronous Finite State Machines." Presented at *IEEE International Test Synthesis Workshop (ITSW),* Santa Barbara, CA (March 1996).

93. R.M. Fuhrer, B. Lin and S.M. Nowick, "Symbolic Hazard-Free Minimization and Encoding of Asynchronous Finite State Machines." Presented at *International Workshop on Logic Synthesis (IWLS),* Lake Tahoe, CA (May 1995).

94. S.M. Nowick and B. Coates, "Automated Design of High-Performance Unclocked State Machines." Presented at *ACM/SIGDA Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU),* Malente, Germany, (Sept. 1993).

95. S.M. Nowick and D.L. Dill, "Asynchronous State Machine Synthesis Using a Local Clock." Presented at *International Workshop on Logic Synthesis (IWLS),* Research Triangle Park, NC (May 1991).

WORKSHOP PAPERS (not refereed, limited distribution in workshop proceedings)

96. M. Singh and S.M. Nowick, "Gate-Level Pipelines for High Throughput," The 6th UK Asynchronous Forum, University of Manchester, July 12-13, 1999.

97. E. Brunvand, S.M. Nowick and K.Y. Yun, "Practical Advances in Asynchronous Design and in Asynchronous/Synchronous Interfaces." Invited survey article. *TAU-99: Seventh ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems,* Monterey, CA (1999).

PROFESSIONAL ACTIVITIES

JOURNAL ACTIVITIES

Associate Editor, IEEE Transactions on Computer-Aided Design, 2003-2009.

Associate Editor, IEEE Transactions on VLSI Systems, 2001-2007.

Guest Editor, IEEE Transactions on Computer-Aided Design, special section of best papers from IWLS-02 workshop (vol 22:6, June 2003).

Guest Editor, Proceedings of the IEEE, special issue on asynchronous circuits and systems, vol. 87, number 2, February 1999.

CONFERENCE ACTIVITIES

Program Committee, Topic Area Chair, Logic and Technology-Dependent Synthesis for Deep-Submicron Circuits, *IEEE/ACM Design, Automation and Test in Europe Conference,* Nice, France (March 2009).

As topic area chair, I am responsible for handling all submissions in this area, and selecting approximately 10 subcommittee members, and leading a subcommittee evaluation, in the leading European digital CAD and design conference.

Program Committee, Topic Area Co-Chair, Logic and Technology-Dependent Synthesis for Deep-Submicron Circuits, *IEEE/ACM Design, Automation and Test in Europe Conference,* Munich, Germany (March 2008).

As topic co-chair, along with my topic chair, I am responsible for handling all submissions in this area, with approximately 10 subcommittee members, in the leading European digital CAD and design conference.

Program Track Chair, Tools and Methodology Track, *IEEE International Conference on Computer Design (ICCD),* San Jose, CA (October 2005).

As track chair, I am holding the position of a Program Committee Subchair responsible for *one-fifth* of the conference's program committee. The position is semi-autonomous: I selected a co-track chair, and 24 track program committee members. My track committee handled 81 paper submissions, in its own independent program committee meeting which I ran on June 20-21, 2005.

General Co-Chair, *11th IEEE International Symposium on Asynchronous Circuits and Systems* ("Async-05" Symposium), Columbia University, New York, NY (April 2005).

I was general co-chair, local arrangements co-chair, and host of the 11th Async Symposium at Columbia University. The symposium had over 100 attendees, and 60 paper submissions, and 21 accepted papers. Invited speakers included:

(i) *Bob Colwell (keynote),* former manager of several recent Pentium projects, and chief Intel architect; and (ii) *Ivan Sutherland,* Turing award winner, and inventor of computer graphics.

Program Chair, *11th IEEE/ACM International Workshop on Logic and Synthesis* ("IWLS" Workshop), New Orleans, LA (June 2002).

Program Co-Chair, *5th IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems* ("Async-99" Symposium), Barcelona, Spain (April 1999).

Focus Group Chair, *10th ACM International Workshop on Logic and Synthesis* ("IWLS" Workshop), Lake Tahoe, CA (June 2001).

Best Paper Award Chair, *7th IEEE International Symposium on Asynchronous Circuits and Systems* ("Async-01" Symposium), Salt Lake City, UT (March 2001).

Co-Founder/Program Committee Co-Chair, *1st IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems* ("Async-94" Symposium), Salt Lake City, UT, November 1994.

I co-founded this international symposium series with 3 colleagues from University of Utah (E. Brunvand, A.L. Davis, G. Gopalakrishnan). We obtained an NSF grant (see above) to help establish the symposium series. We also obtained sponsorship of IEEE Computer Society and IEEE Technical Committee on VLSI, and cooperation with IFIP Working Groups 10.2 and 10.5.

The symposium was a success, with nearly 100 attendees. There were 74 paper submissions and 25 accepted papers. Proceedings were published by IEEE Computer Society.

The series itself has maintained excellent momentum. The 2nd Symposium (Japan 1996), 3rd Symposium (Netherlands 1997), 4th Symposium (San Diego 1998) and 5th Symposium (Spain 1999) each had 95-115 attendees and 58-70 paper submissions.

FUNDING AGENCIES

Invited Participant/Speaker: DARPA Workshop on Clockless Logic. Arlington, VA, August 8, 2002. DARPA convened an exploratory workshop to consider a major new funding initiative in the area of asynchronous (i.e., clockless) digital circuits. I was an invited participant and speaker, one of only about 5 speakers from academia. The result of the meeting was positive: in early 2003, DARPA announced a significant new funding initiative in clockless logic.

Invited Presenter/Panelist: "Making the Most of Your CAREER Award."

1st NSF CAREER Program PI Meeting, CISE Division (*Plenary Session*), National Science Foundation (1/11/99).

NSF ITR Award Grant Review Panelist, CISE Division, National Science Foundation (4/29-4/30/04).

NSF CAREER Award Review Panelist, CISE Division, National Science Foundation (10/25/01).

NSF Grant Review Panelist, CISE Division, National Science Foundation (3/4-3/5/99).

MEDIA INTERVIEWS

The New York Times, *Circuits Section,* "What's Next" Column, (August 22, 2002). *"Faster Chips That March to Their Own Improvised Beat."* (URL: http://www.cs.columbia.edu/ nowick/22NEXT.pdf)

Technology Review Magazine *(cover story)* (based in MIT): October 2001, vol. 104:8 (pp. 36-41). *"It's Time for Clockless Chips."*
(URL: http://www.cs.columbia.edu/async/misc/technologyreview_oct_01_2001.html)

PROGRAM COMMITTEES

Program Committee Member, **DAC:** *IEEE/ACM Design Automation Conference* (2002-2004)

Program Committee Member, **ICCAD:** *IEEE/ACM International Conference on Computer-Aided Design* (1998-1999)

Program Committee Member, **DATE:** *IEEE/ACM Design, Automation and Test in Europe Conference* (2000-2002, 2005-2007)

Program Committee Member, **ICCD:** *IEEE International Conference on Computer Design* (1995-1999, 2005-2007)

Program Committee Member, **Async:** *IEEE International Symposium on Asynchronous Circuits and Systems* (1994, 1996-2000, 2002, 2004, 2006-2007)

Steering Committee Member, **Async:** *IEEE International Symposium on Asynchronous Circuits and Systems* (1994-2007)

Program Committee Member, **IWLS-07:** *IEEE/ACM International Workshop on Logic and Synthesis* (1999-2007)

Program Committee Member, **ARVLSI:** *Conference on Advanced Research in VLSI* (1997, 1999, 2001)

Program Committee Member, **VLSI Design:** *IEEE International Conference on VLSI Design* (1998)

Program Committee Member, **TAU:** *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems* (1997)

Program Committee Member, **GLVLSI:** *IEEE Great Lakes Symposium on VLSI* (1997)

Program Committee Member, **Israel Workshop on Asynchronous VLSI Circuits and Systems** (1995)

INVITED TALKS: Conferences and Workshops

Invited Speaker: Clockless Logic Symposium, Washington University. I was one of 6 invited speakers at a special anniversary symposium at Washington University (March 2004), celebrating the 150th anniversary of the university and the 30th anniversary of the completion of the asynchronous 'Macromodules Project'. Ivan Sutherland gave the opening technical talk.

See Washington University's web page for publicity: *"Symposium Gathers Computing Greats to Decide Whether to Go Clockless"*, http://news-info.wustl.edu/tips/page/normal/727.html and http://cse.seas.wustl.edu/clockless. The symposium was attended by approximately 400 people, and opened by the former University Chancellor.

2002 Summer School on Asynchronous Design, TIMA Institute, Grenoble, France. Invited to give intensive half-day lab course on my MINIMALIST CAD package (presented four times), as well as introductory tutorial on hazard-free logic synthesis. Grenoble, France, July 2002.

2002 IEEE International Symposium on Computer Architecture (ISCA), "GALS Session" Keynote. Workshop on Complexity-Effective Design. Talk on mixed-timing interfaces, May 2002.

2nd ACiD-WG Workshop (5th funding framework), of the European Community: "MINIMALIST: A CAD Environment for the Synthesis and Optimization of Burst-Mode Asynchronous Controllers." Munich, Germany, 1/29/02.

Async-00: Sixth IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems, "Synthesis of Burst-Mode Asynchronous Controllers and the MINIMALIST CAD Package," S.M. Nowick. Invited Tutorial and Hands-On Session (2 hours, presented twice). Eilat, Israel 4/3/00.

DAC-99: 36th ACM/IEEE Design Automation Conference, "Practical Advances in Asynchronous Design and Asynchronous/Synchronous Interfaces," E. Brunvand, S.M. Nowick and K.Y. Yun. Embedded Tutorial. Organizer: S.M. Nowick. New Orleans, LA, 6/22/99.

TAU-99: Seventh ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, "Practical Advances in Asynchronous Design and Asynchronous/Synchronous Interfaces," E. Brunvand, S.M. Nowick and K.Y. Yun. Invited tutorial. Organizer: S.M. Nowick. Monterey, CA, 3/8/99.

Third ACiD-WG Workshop (ACiD = Asynchronous Circuit Design), Newcastle upon Tyne, UK, 1/17-1/19/99. Sponsored by the European Union "Esprit" Project. **Invited tutorial (2 parts):**

- "Burst-Mode: Specification, Synthesis, and Applications," 1/18/99.
- "Burst-Mode: Optimization Algorithms and the MINIMALIST CAD Package," 1/18/99.

ICCD-97: IEEE International Conference on Computer Design, "Practical Advances in Asynchronous Design," E. Brunvand, S.M. Nowick and K.Y. Yun. Embedded tutorial. Austin, TX, 10/15/97.

1995 Israel Workshop on Asynchronous VLSI Circuits and Systems. Invited tutorial and workshop presentations. Sea of Galilee, Israel, 3/19-3/22/95.

1994 IEEE Workshop on Computer Elements, "Automated Design of High-Performance Asynchronous State Machines." Vail, CO, 6/26-6/29/94.

1993 Winter Workshop on VLSI, "The Design of a High-Performance Cache Controller: a Case Study in Asynchronous Synthesis." Asilomar Conference Center, Pacific Grove, CA, 2/9/93.

INVITED TALKS: Universities and Industry

NASA Goddard Space Flight Center, (invited by Wes Powell, associate director of microelectronics). "Advances in Designing Clockless Digital Systems." Greenbelt, MD, 1/22/08.

Princeton University, Department of Electrical and Computer Engineering, "MOUSETRAP: Designing High-Speed Asynchronous Digital Pipelines." Princeton, NJ, 12/4/06.

Cooper Union, Department of Electrical Engineering, "MOUSETRAP: Designing High-Speed Asynchronous Digital Pipelines." New York, NY, 11/15/06.

IBM T.J. Watson Research Center, "Efficient Performance Analysis of Asynchronous and Mixed-Timing Systems." Yorktown Heights, NY, 12/12/05.

University of Maryland, ECE Department, "Automated Compilation of Asynchronous Digital Systems." College Park, MD, 11/14/05.

University of Manchester, Department of Computer Science, (Manchester, UK). 3 talks (9/02, 10/02, 2/03).

University of California, Berkeley, EECS Electronic Systems Design Seminar Series, "Low-Latency Interfaces for Mixed-Timing Domains." Berkeley, CA, 11/28/01.

University of Michigan, EECS Department VLSI Seminar Series, "MOUSETRAP: Designing High-Speed Asynchronous Digital Pipelines." Ann Arbor, MI, 11/19/01.

Theseus Logic, Inc. "Synthesis of Burst-Mode Asynchronous Controllers, and the MINIMALIST CAD Package." Sunnyvale, CA, 3/6/00.

Columbia University, Department of Computer Science, "Asynchronous Circuits: Recent Advances in the Design of Clockless Systems." NY, NY, 9/27/99.

University of Rochester, Department of Electrical and Computer Engineering, "Asynchronous Circuits: an Introduction and Case Study — a Fast Huffman Decoder for Compressed-Code Embedded Processors." Rochester, NY, 5/21/99.

Stanford University, Computer Systems Laboratory, "Asynchronous Circuits: an Introduction and Case Study — a Fast Huffman Decoder for Compressed-Code Embedded Processors." Stanford, CA, 5/18/99.

Princeton University, Department of Electrical and Computer Engineering, "Asynchronous Circuits: an Introduction and Case Study — a Fast Huffman Decoder for Compressed-Code Embedded Processors." Princeton, NJ, 4/28/99.

University of Michigan, Department of Electrical and Computer Engineering, "Asynchronous Circuits: an Introduction and Case Study — a Fast Huffman Decoder for Compressed-Code Embedded Processors." Ann Arbor, MI, 4/15/99.

University of Texas, Departments of Computer Science and Electrical/Computer Engineering, "Algorithms and Tools for the Synthesis, Optimization and Testability of Asynchronous Controllers." Austin, TX, 4/9/99.

University of Illinois, Department of Electrical and Computer Engineering, "Algorithms and Tools for the Synthesis, Optimization and Testability of Asynchronous Controllers." Urbana, IL, 4/5/99.

University of Utah, Department of Computer Science, "Recent Advances in CAD Tools and Algorithms for Asynchronous and Synchronous Controllers." Salt Lake City, UT, 3/24/99.

Intel Corporation, "Synthesis of Burst-Mode Asynchronous Controllers, and the MINIMALIST CAD Package." Santa Clara, CA, 3/12/99.

Intel Corporation, Strategic CAD Laboratory, "Recent Advances in CAD Tools and Algorithms for Asynchronous and Synchronous Controllers." Hillsboro, OR, 3/10/99.

Philips Research Laboratories, "Current Research in Asynchronous Design at Columbia University: an Overview." Eindhoven, The Netherlands, 1/27/99.

South Bank University, Centre for Concurrent Systems and VLSI, "A Fast Asynchronous Huffman Decoder for Compressed-Code Embedded Processors." London, UK, 1/25/99.

University of Manchester, Department of Computer Science, "Current Research in Asynchronous Design at Columbia University: an Overview." Manchester, UK, 1/22/99.

Stanford University, Stanford "CAD Day" presentation, "MINIMALIST: An Environment for Synthesis and Testability of Burst-Mode Asynchronous Machines." Stanford, CA, 11/12/98.

University of California, San Diego, Department of Electrical and Computer Engineering, “The Design of Low-Power and High-Performance Asynchronous Systems.” La Jolla, CA, 6/6/97.

University of California, Los Angeles, Department of Computer Science, “The Design of Low-Power and High-Performance Asynchronous Systems.” Los Angeles, CA, 6/5/97.

University of Utah, Department of Computer Science, “The Design of High-Performance Asynchronous Systems.” Salt Lake City, UT, 1/10/97.

NEC Research Laboratory, “The Design of High-Performance Asynchronous Datapaths.” Princeton, NJ, 12/10/96.

Sun Laboratories, “The Design of High-Performance Asynchronous Datapaths.” Palo Alto, CA, 11/8/96.

Intel Corporation, “The Design of High-Performance Asynchronous Datapaths.” Santa Clara, CA, 11/7/96.

University of California, Irvine, Department of Computer Science, “The Design of High-Performance Asynchronous Datapaths.” Irvine, CA, 11/5/96.

University of Aizu, Department of Computer Science, (Aizu-Wakamatsu, Japan).
Invited lecture series:

- “A CAD Framework for the Design, Optimization and Testability of Asynchronous Controllers,” 3/27/96.
- “Burst-Mode Sequential Machines: Basic Synthesis Algorithms and Optimal State Assignment,” 3/27/96.
- “Hazard-Free Combinational Synthesis: Logic Minimization and Testability,” 3/25/96.

IBM T.J. Watson Research Center, “A CAD Framework for the Design, Optimization and Testability of Asynchronous Controllers.” Yorktown Heights, NY, 1/26/96.

University of Utah, Department of Computer Science “Symbolic Hazard-Free Minimization and Encoding of Asynchronous Finite State Machines.” Salt Lake City, UT, 5/30/95.

IMEC Laboratories, “Automatic Synthesis of Burst-Mode Asynchronous Controllers”. Leuven, Belgium, 9/7/93.

University of Calgary, Department of Electrical Engineering, “Automated Design of High-Performance Unclocked State Machines”. Calgary, Alberta, Canada, 9/3/93.

Stanford University, Department of Computer Science, “Automated Design of High-Performance Unclocked State Machines”. Stanford, CA, 8/20/93.

University of Washington, Department of Computer Science, “Automated Design of High-Performance Unclocked State Machines”. Seattle, WA, 8/19/93.

University of Utah, Department of Computer Science “Exact Two-Level Minimization of Hazard-Free Logic with Multiple-Input Changes”. Salt Lake City, UT, 5/10/93.

Princeton University, Department of Electrical Engineering, “Automatic Synthesis of Burst-Mode Asynchronous Controllers”. Princeton, NJ, 5/4/93.

University of Waterloo, Department of Computer Science “Automatic Synthesis of Burst-Mode Asynchronous Controllers”. Waterloo, Ontario, Canada, 4/30/93.

HaL Computers, “Automatic Synthesis of Locally-Clocked Asynchronous State Machines”. Campbell, CA, 2/28/92.

University of Utah, Department of Computer Science, “Automatic Synthesis of Locally-Clocked Asynchronous State Machines”. Salt Lake City, UT, 11/26/91.

Cirrus Logic,“Synthesis of Asynchronous State Machines Using a Local Clock”. Milpitas, CA, 9/6/91.

JOURNAL AND CONFERENCE REFEREEING

IEEE Transactions on Computers; IEEE Transactions on Computer-Aided Design; IEEE Transactions on Circuits and Systems; IEEE Transactions on VLSI Systems; INTEGRATION: the VLSI journal; IEEE Design and Test of Computers; IEE Electronic Letters (UK); VLSI conference; International Conference on Computer-Aided Design; International Conference on Computer Design; Design Automation Conference; Hawaii International Conference on System Sciences; NSF proposals.

DEPARTMENTAL

CURRENT PHD STUDENTS

Melinda Agyekum (September 2004 - present)

Peggy McGee (September 2003 - present)

FORMER PHD STUDENTS

Cheoljoo Jeong (May 2002 - December 2008) Thesis defense: 10/22/07; thesis deposit: 12/19/07. (Currently a senior design engineer at Cadence Design Systems, Santa Clara, CA.)

Tiberiu Chelcea (September 1997 - present). Thesis defense: 12/8/03. (Currently a Research Scientist in the department of computer science at Carnegie-Mellon University.)

Montek Singh (September 1994 - December 2001.) Thesis defense: 12/12/01; thesis deposit: 1/3/02. (Currently a tenured associate professor of computer science at University of North Carolina, Chapel Hill.)

Michael Theobald (September 1994 - present). Thesis defense: 12/18/01. (Currently a researcher at D.E. Shaw Laboratory; formerly a Research Scientist in the department of computer science at Carnegie-Mellon University, working with Prof. Ed Clarke.)

Robert M. Fuhrer (December 1993 - December 1998). Thesis defense: 12/14/98; thesis deposit: 5/7/99. (Currently at IBM Research, T.J. Watson.)

Moustafa Mohamed (September 2006 - October 2007) (withdrew from program)

Cheng-Hong Li (September 2002 - September 2004) (transferred to Luca Carloni)

FORMER MS STUDENTS

Michael Horak (June 2007 - August 2008)
(co-chair of MS thesis committee, University of Maryland, College Park)

Walter Dearing (January - August 2007)

Melinda Agyekum (September 2002 - June 2004)

Amitava Mitra (September 2002 - December 2003)

PHD THESIS COMMITTEES

Cheoljoo Jeong (CS), "Synthesis and Optimization of Robust Asynchronous Threshold Networks" (12/19/07 deposit); advisor: Prof. Steven Nowick.

Yee William Li (EE), "Self-Timed Techniques in Digital Signal Processing" (5/24/05); advisor: Prof. Kenneth Shepard (EE).

Tiberiu Chelcea (CS), "Design and Optimization of Large-Scale Asynchronous and Mixed-Timing Systems" (12/8/03); advisor: Prof. Steven Nowick.

S. Henry Li (EE), "Low-Energy Communication Processor with Dynamic Variable Power-Supply Scaling"(2/1/02); advisor: Prof. Charles Zukowski.

Michael Theobald (CS), "Efficient Algorithms for the Design of Asynchronous Control Circuits" (12/18/01); advisor: Prof. Steven Nowick.

Montek Singh (CS), "High-Speed Asynchronous Digital Pipelines" (12/12/01); advisor: Prof. Steven Nowick.

Euiseok Kim (*Kwangju Institute of Science and Technology (K-JIST)*, South Korea), "A Study on High-Level Synthesis of Asynchronous VLSI Systems" (6/16/01); advisor: Prof. D.-I. Lee. (Invited as *External Reviewer*.)

Shao-Yi Wang (EE), "Energy Reduction in CMOS Logic Arrays Through Partitioning" (1/24/01); advisor: Prof. Charles Zukowski.

J.W.J.M. Rutten (EE, *Technical University of Eindhoven*, The Netherlands), "Synthesis of Asynchronous Burst-Mode Finite State Machines" (4/19/00); advisor: Prof. Jochen Jess. (Invited as *2nd Promoter*.)

Robert M. Fuhrer (CS), "Sequential Optimization of Asynchronous and Synchronous Finite-State Machines: Algorithms and Tools" (12/14/98); advisor: Prof. Steven M. Nowick.

Fu-Chiung (John) Cheng (CS), "Synthesizing Iterative Functions into High Performance Delay-Insensitive Tree Circuits" (4/22/98); advisor: Prof. Stephen Unger.

Hui Lei (CS), "Uncovering and Exploiting the Intrinsic Correlations between File References" (12/17/97); advisor: Prof. Dan Duchamp.

Luis Plana (CS), "Contributions to the Design of Asynchronous Macromodular Systems" (12/16/97); advisor: Prof. Stephen Unger.

Christophe R. Tretz (EE), "Sizing and Topology in SOI and Bulk Low-Power High-Speed CMOS Circuits" (5/16/97); advisor: Prof. Charles Zukowski.

Ping-Chang Yen (IEOR), "On the Architecture of Object-Oriented Scheduling Systems" (8/29/95); advisor: Prof. Michael Pinedo.

Danilo Florissi (CS), "Isochronets: A High-Speed Network Switching Architecture" (4/21/95); advisor: Prof. Yechiam Yemini.

Bill Schilit (CS), "Context-Aware Software Reconfiguration Supporting Mobile Distributed Computing" (12/12/94); advisor: Prof. Dan Duchamp.

Hong Shi (EE), "Design, Analysis, and Optimization of Broadband ATM Switches Implemented in VLSI" (6/30/94); advisor: Prof. Omar Wing.

Gary L. Dare (EE), "Accuracy Management for Delay-Oriented Control in Mixed-Mode Simulation of Digital VLSI Circuits" (12/14/93); advisor: Prof. Charles Zukowski.

Carl Tait (CS), "A File System for Mobile Computing" (4/20/93); advisor: Prof. Dan Duchamp.

PHD THESIS PROPOSAL COMMITTEES

Cheoljoo Jeong (CS), "Optimization Techniques for Robust Asynchronous Threshold Networks (5/26/06); advisor: Prof. Steven Nowick.

Tiberiu Chelcea (CS), "Design and Optimization Techniques for Large-Scale Asynchronous and Mixed-Timing Systems" (5/20/02); advisor: Prof. Steven Nowick.

Montek Singh (CS), "Optimization of Self-Timed Pipelines and Large-Scale Systems" (4/6/99); advisor: Prof. Steven Nowick.

Michael Theobald (CS), "Efficient Algorithms for the Design of Asynchronous Control Circuits" (9/23/98); advisor: Prof. Steven Nowick.

Fu-Chiung (John) Cheng (CS), "Synthesizing Iterative Functions into High Performance Delay-Insensitive Tree Circuits" (5/16/97); advisor: Prof. Stephen Unger.

Luis Plana (CS), "Contributions to the Design of Asynchronous Macromodular Systems" (2/20/97); advisor: Prof. Stephen Unger.

Hui Lei (CS), "Uncovering and Exploiting the Intrinsic Correlations between File References" (10/1/96); advisor: Prof. Dan Duchamp.

Robert Fuhrer (CS), "Sequential Optimization of Asynchronous Controllers: Algorithms, Tools and Applications" (5/2/95); advisor: Prof. Steven Nowick.

Danilo Florissi (CS), "Isochronets: A High-Speed Network Switching Architecture" (5/3/93); advisor: Prof. Yechiam Yemini.

DOCTORAL QUALIFYING EXAMINATIONS

Ben Nathanson (EE), "The Design of Self-Timed Pipelines" (12/14/93); advisor: Prof. Steven Nowick.

UNDERGRADUATE RESEARCH PROJECTS

Charles O'Donnell (May 2002-May 2003) Collaborated on a research project on the existence criteria for hazard-free multi-level logic implementations. The

result was an accepted co-authored paper at IEEE Async-03 Symposium; we are currently working on a followup journal submission. Charles has just been accepted into the MIT PhD program. Charles also won the *Theodore Bashkow Award* from the Columbia University CS Department for best undergraduate research project (May 2003).

Alexander Shapiro (January 1999-May 2000) (Supported partially by an NSF REU award.) Alexander received the *Theodore Bashkow award* in May 2000, for the computer science department senior who has excelled in independent projects.

Paul Goldstein (Spring 1996)

Andre Avzaradel (Spring 1996)

Tao Wu (Summer 1994). (Supported by NSF REU award; research resulted in published conference paper, 1996 Design Automation Conference.)