STEVEN MARK NOWICK

Office:
Department of Computer Science
Room 508 Computer Science Building
Columbia University
1214 Amsterdam Avenue
New York, NY 10027
Tel.: (212) 939-7056
FAX: (212) 666-0140

Internet: *nowick@cs.columbia.edu*
URL: *http://www.cs.columbia.edu/~nowick*

RESEARCH INTERESTS

Asynchronous and mixed-timing digital circuits, scalable networks-on-chip (NoC's) for shared-memory parallel processors and embedded systems, ultra-low energy digital systems, computer-aided digital design, Internet-of-Things, and low-power and robust global communication.

PERSONAL INFORMATION

Date of birth: March 28, 1954
Citizenship: U.S.A.

EDUCATION

Stanford University, Stanford, CA.
Ph.D., Computer Science, March 1993.
Thesis Title: "Automatic Synthesis of Burst-Mode Asynchronous Controllers."
Thesis Advisor: David L. Dill

Columbia University, New York, NY.
Non-degree Computer Science program (1984-86).

Columbia University, New York, NY.
M.A., Music Composition, 1979.

Yale University, New Haven, CT.
B.A., Music, 1976, *magna cum laude*, with departmental honors.

EXPERIENCE

Computer Engineering Program, Columbia University
Chair, July 2008 – June 2013.

Department of Computer Science, Columbia University
Full Professor, March 2008 – present.

Department of Computer Science, Columbia University
Associate Professor, July 1998 – March 2008.

Computer Engineering Program, Columbia University
Acting Chair, Jan 2000 – June 2000.

Department of Computer Science, Columbia University
Assistant Professor, January 1993 – June 1998.

Department of Computer Science, Stanford University
Research Assistant, September 1986 – December 1992.

Hewlett-Packard Laboratories, Palo Alto, CA.
Researcher/Intern, Summers 1989, 1990.

Ford Aerospace, Western Development Laboratories, Palo Alto, CA.
Software Engineer, Summer 1987.

AWARDS AND HONORS

SEAS Alumni Distinguished Faculty Teaching Award
Columbia Engineering, Columbia University, 2011.

IEEE Fellow
IEEE, Circuits and Systems Society (CAS), 2009.

ACM Senior Member
Association of Computing Machinery, 2009.

Alfred P. Sloan Research Fellowship
Alfred P. Sloan Foundation, New York, NY, 1995.

NSF Faculty Early Career Development ("CAREER") Award
Design Automation Program (formerly: Design, Tools and Test)
National Science Foundation, Arlington, VA, 1995.

NSF Research Initiation Award ("RIA")
Design Automation Program (formerly: Design, Tools and Test)
National Science Foundation, Arlington, VA, 1993.

Best Paper Award
Logic and Circuit Design track
30th IEEE International Conference on Computer Design
IEEE Computer Society; Montreal, Canada 2012.

Best Paper Award
6th IEEE Async Symposium
(IEEE Int. Symp. on Advanced Research in Async. Circuits and Systems)
IEEE Computer Society; Eilat, Israel 2000.

Best Paper Award
Asynchronous circuits and systems mini-track
26th Hawaii International Conference on System Sciences
IEEE Computer Society; Maui, HI 1993.

Best Paper Award
Computer-Aided Design track
IEEE International Conference on Computer Design
IEEE Computer Society; Cambridge, MA 1991.

Best Paper Finalist
21st IEEE "Async" Symposium
(International Symposium on Asynchronous Circuits and Systems)
IEEE Computer Society; Mountain View, CA 2015.

Best Paper Finalist
ACM/IEEE Design, Automation and Test in Europe (DATE) Conference
EDA Consortium; Grenoble, France 2013.

Best Paper Finalist (2 papers)
14th IEEE "Async" Symposium
(International Symposium on Asynchronous Circuits and Systems)
IEEE Computer Society; Newcastle-upon-Tyne, UK 2008.

Best Paper Finalist
9th IEEE "Async" Symposium
(International Symposium on Asynchronous Circuits and Systems)
IEEE Computer Society; Vancouver, BC, Canada 2003.

Best Paper Finalist
8th IEEE "Async" Symposium
(International Symposium on Asynchronous Circuits and Systems)
IEEE Computer Society; Manchester, UK 2002.

Best Paper Finalist
4th IEEE "Async" Symposium
(International Symposium on Advanced Research in Asynchronous Circuits and Systems)
IEEE Computer Society; La Jolla, CA 1998.

Invited Panelist: "Making the Most of Your CAREER Award"
1st NSF CAREER Program PI Meeting
Plenary Session, CISE Division
National Science Foundation, Arlington, VA 1999.

RESEARCH SUPPORT *(LARGER GRANTS)*

NSF Medium-Scale Award: *SHF:Medium:Power-Adaptive, Event-Driven Data Conversion and Signal Processing Using Asynchronous Digital Techniques,"* PI: Y. Tsividis (Columbia EE Dept.), co-PI: S.M. Nowick. NSF solicitation 09-555 (NSF CCF/SHF). NSF Award No. CCF-0964606 (7/1/10-6/30/15).
Award amount: $1,062,605. My portion: $500,000 (approximately).

NSF Medium-Scale Award: *"CPA-DA-T: Design and Tools for Easy-to-Program Massively Parallel On-Chip Systems: Deriving Scalability Through Asynchrony,"* PI: S. Nowick, co-PI: U. Vishkin (U. of Maryland). NSF Award No. CCF-0811504 (8/1/08-7/31/13).
Award amount: $921,686. My portion: $461,000.

> **This award was one of only two large-scale "team" proposals awarded** *by NSF under the "Design Automation for Micro and Nano Systems" topical area for CCF solicitation 07-587 in 2008.* The goal of this proposal is to develop a first-of-its-kind partly-asynchronous, partly-synchronous high-end massively-parallel-on chip computer. In particular, a high-speed, low-power asynchronous communication fabric will be developed, to connect synchronous processors, and which

is robust and flexible in the presence of timing variability and multiple clock rates and supports a 'plug-and-play' assembly of low-power complex parallel processors.

DARPA "CLASS" Project. I was brought onto this major multi-institution contract officially in Fall-05 (though I made initial contributions as an advisor throughout early 2005). The project was completed in *March 2007*.
Total project contract: $14,000,000. Subcontract award amount (Nowick): $502,000.

This DARPA program is the largest US government research program for asynchronous digital design in the last 30 years. Its goal is to make asynchronous digital design viable for the commercial and military sectors. There were **approximately 20 large-scale proposals submitted,** and **only 1 contract funded,** headed by *Boeing* (PI), with participation of *Philips Semiconductors* (via its incubated asynchronous startup, called *Handshake Solutions*, two asynchronous startups and two smaller academic efforts. (This startup has been recently ranked one of the "top 50 startups to watch" by EE Times.)

The two goals of the project are: (i) building a large-scale asynchronous demonstration chip (for Boeing military applications), and compare its performance and cost to an equivalent synchronous chip; and (ii) provide a "legacy asynchronous CAD tool" for future asynchronous designs.

I was brought onto the project for its Phase 2/3, along with my former PhD student Montek Singh (currently an assistant professor at UNC), to play a key participating role in (a) *developing CAD tools* for designing asynchronous circuits for the project, and (b) *transferring my high-speed patented asynchronous circuit technology,* i.e. "Mousetrap" pipelines, into these tools. My *Columbia-patented* **Mousetrap** high-speed asynchronous pipeline circuits were incorporated into the Philips' asynchronous CAD tool being developed for the project. Some of them are being applied to the Boeing demo chip for the project. In addition, several CAD optimizations I have developed were incorporated into an alternative "low-power" CAD tool developed through a Florida startup company, *Theseus Logic*.

NSF Medium-Scale ITR Award: *"A CAD Framework for the Design and Optimization of Large-Scale Asynchronous Digital Systems"*. PI: S. Nowick (joint proposal with University of Southern California). NSF Award No. CCR-00-86036 (9/1/00-8/31/05).
Award amount: $1,612,809. My portion: $850,000 (approximately).

NSF Medium-Scale ITR Award: *"Asynchronous Digital Signal Processing for the Software Radio"*. co-PI: S. Nowick (joint proposal with Prof. Ken Shepard, EE Department). NSF Award No. CCR-00-86007 (9/1/00-8/31/03).
Award amount: $969,227. My portion: $400,000 (approximately).

Note: In 2000, **only 62 medium-scale ITR awards were granted, out of 920 submitted proposals,** across all areas of information technology. *I was 1 of only 4 investigators nationally in 2000 to receive 2 medium-scale NSF ITR awards.* The ITR initiative is an outgrowth of President Clinton's *PITAC* advisory committee for national information technology, to fund "long-term risk-taking research".

RESEARCH SUPPORT *(MEDIUM/ SMALL GRANTS)*

NSF Grant: "SHF:Small:An Asynchronous Network-on-Chip Methodology for Cost-Effective and Fault-Tolerant Heterogeneous SoC Architectures" PI: S.M. Nowick. NSF Award No. CCF-1527796 (8/1/15-7/31/18). *Award amount:* $420,000. *My portion:* $420,000.

NSF Grant: "SHF:Small:Designing Low-Latency and Robust Interconnection Networks with Fine-Grain Dynamic Adaptivity Using Asynchronous Techniques" PI: S.M. Nowick. NSF Award No. CCF-1219013 (7/1/12-6/30/16). *Award amount:* $450,000. *My portion:* $450,000.

Initiatives in Science and Engineering (ISE) Grant, Columbia University, Office of the Executive Vice President of Research: "Designing a Flexible, High-Throughput Asynchronous Interconnect Fabric for Future Single-Chip Parallel Processors," (7/1/06-6/30/08): $185,530.

This competitive internal award, from the executive vice president of research at Columbia University, is for proposals which "test unusually creative ideas" that are "in too early a stage of data gathering to be viable for the usual funding agencies."

Supplement to NSF ITR award: awarded summer 2003, for support of minority student development and research (Melinda Agyekum, female/African-American MS student, working with me on research on asynchronous digital design): $48,932.

NYS Microelectronics Design Center (MDC) Grant: "Design Techniques for Compressed Code Embedded Processors", (7/1/02-6/30/03): $20K.

NYS Microelectronics Design Center (MDC) Grant: "Dynamically-Adaptive Asynchronous Digital Systems", (7/1/01-6/30/02): $30K.

NSF Grant: "Methodologies and CAD Tools for the Design of Asynchronous Systems," PI: S. Nowick. NSF Award No. CCR-99-88241 (11/15/00-10/31/03): $200,895.

NYS Center for Advanced Technology (CAT): "The Design of Multi-Gigahertz Asynchronous Arithmetic Circuits for High-Speed Digital Signal Processing". PI: S. Nowick. *Award date:* July 10, 2000. Total: $70,000.

Sun Microsystems Gift: Research on Asynchronous Design. PI: S. Nowick. (4/00-4/00/01): $30,000.

NSF Research Experiences for Undergraduates *(REU)*, supplement to NSF Award No. CCR-97-34803 (6/1/99-8/31/99): $5,000.

Columbia University Seed Grant: "The Design of a Fast Hardware Accelerator for Genome Database Searches," PI: S. Nowick. Joint funding by (i) Office of the Vice Provost, Strategic Initiative Fund ($30,000), and (ii) Dean of the School of Engineering and Applied Science ($15,000) (9/98-8/99): $45,000.

NSF Grant: "High-Performance and Low-Power Asynchronous Datapaths: Design and Applications," PI: S. Nowick. NSF Award No. CCR-97-34803 (7/15/98-6/30/01): $335,000.

Supplement to NSF CAREER Award, funding for CAD software tool development. NSF Award No. MIP-9501880, Proposal MIP-9840302 (1/1/98-8/31/98): $20,763.

NSF Faculty Early Career Development (CAREER) Award, "Testability and Sequential Optimization of Asynchronous State Machines," NSF Award No. MIP-9501880 (9/1/95-8/31/98): $120,000.

Alfred P. Sloan Research Fellowship, Alfred P. Sloan Foundation, New York, NY (9/16/95-9/15/97): $30,000.

Grant for Joint Research in Asynchronous Design, IBM Corporation, T.J. Watson Research Center (2/95-1/96): $40,000.

NSF Grant: "Advanced Research in Asynchronous Circuits and Systems," NSF Award No. MIP-9406532 (11/94-7/95). PI: Erik Brunvand; co-PIs: Ganesh Gopalakrishnan, Steven M. Nowick. Grant to establish a new international symposium on asynchronous circuit design (held in Salt Lake City, Utah, November 1994). Total Budget: $12,320.

NSF Research Initiation Award (RIA), "The Design of High-Performance Asynchronous Controllers," NSF Award No. MIP-9308810 (9/93-8/96): $100,000.

NSF Research Experiences for Undergraduates *(REU)*, supplement to NSF RIA award (6/93-8/93): $5,000.

PATENTS

Pending:

- *Bi-Modal Arbitration Nodes for a Low-Latency Adaptive Asynchronous Interconnection Network and Methods for Using the Same,* S.M. Nowick, G.D. Gill, S. Attarde.
  Application No. PCT/US12/29069 (filed March 14, 2012).

Issued:

1. *Asynchronous Digital Circuits Including Arbitration and Routing Primatives for Asynchronous and Mixed-Timing Networks,* Steven M. Nowick, Michael N. Horak, Matthew Carlberg. **U.S. Patent #8,766,667** (July 1, 2014).

2. *Asynchronous Digital Circuits Including Arbitration and Routing Primitives for Asynchronous and Mixed-Timing Networks,* Steven M. Nowick, Michael N. Horak, Matthew Carlberg. **U.S. Patent #8,362,802** (January 29, 2013).

3. *Methods and Media for Forming a Bound Network,* Cheoljoo Jeong, Steven M. Nowick. **U.S. Patent #7,840,915** (November 23, 2010).

4. *Methods, Media and Means for Forming Asynchronous Logic Networks,* Cheoljoo Jeong, Steven M. Nowick. **U.S. Patent #7,729,893** (June 1, 2010).

5. *Low Latency FIFO Circuit for Mixed Clock Systems,* Tiberiu Chelcea, Steven M. Nowick. **U.S. Patent #7,197,582** (March 27, 2007).

6. *Circuits and Methods for High-Capacity Asynchronous Pipeline Processing,* Montek Singh, Steven M. Nowick. **U.S. Patent #7,053,665** (May 31, 2006). [continuation of #6,867,620]

7. *Asynchronous Pipeline with Latch Controllers,* Montek Singh, Steven M. Nowick. **U.S. Patent #6,958,627** (October 25, 2005).

8. *Circuits and Methods for High-Capacity Asynchronous Pipeline,* Montek Singh, Steven M. Nowick. **U.S. Patent #6,867,620** (March 15, 2005).

9. *Variable-Length, High-Speed Asynchronous Decoder Circuit,*, Steven M. Nowick, Martin Benes, Andrew Wolfe. **U.S. Patent #6,865,668** (March 8, 2005).

10. *Low Latency FIFO Circuits for Mixed Asynchronous and Synchronous Systems,* Tiberiu Chelcea, Steven M. Nowick. **U.S. Patent #6,850,092** (Feb. 1, 2005).

11. *High-Throughput Asynchronous Dynamic Pipelines,* Montek Singh, Steven M. Nowick. **U.S. Patent #6,590,424** (July 8, 2003).

12. *High-Speed Asynchronous Decompression Circuit for Variable-Length Coded Data,* Steven M. Nowick, Martin Benes, Andrew Wolfe. **U.S. Patent #6,408,421** (June 18, 2002).

CAD TOOL RELEASES

1. THE "CaSCADE" ASYNCHRONOUS TOOL FRAMEWORK.

The "CaSCADE" package is a new asynchronous design environment developed at Columbia University (under Steven Nowick) and USC (under Prof. Peter Beerel) ("CaSCADE" = Columbia University and University of Southern California Asynchronous Design Environment.) All the tools are freely available for downloads and use, targeting Linux platforms. The goal of this package is to provide substantial tool support for automated synthesis, optimization and validation of asynchronous circuits and systems.

The CaSCADE package includes 3 distinct CAD tools from my Columbia group: (i) **MINIMALIST v2.0,** for synthesis and optimization of asynchronous controllers; (ii) **ATN_OPT v0.1,** for synthesis and optimization of robust asynchronous threshold networks; and (iii) **DES Analyzer v0.1,** for performance analysis of concurrent systems.

The new v2.0 release of MINIMALIST, as part of the CaSCADE package, has received **42 downloads** since November 2007, to over **10 countries**. This initial release of our ATN_OPT and DES Analyzer tools, also part of the CaSCADE package, has resulted in, respectively, **27 and 26 downloads**, to **9 and 10 countries**, since November 2007.

The CaSCADE tool release was written up in **EE Times (Europe),** *"Asynchronous EDA Tools Available for Free Download,"* Peter Clarke, 12/11/2007 (URL: http://www.eetimes.eu/204801096).

Each of these tools is available for download from the CaSCADE web page; see http://www.cs.columbia.edu/~nowick/asynctools. Each includes detailed tutorials, benchmark examples, graphic interfaces, convenient scripts, and support for commercial hardware description languages (VHDL and/or Verilog).

Download sites for these tools include government agencies such as *NASA Goddard*; research laboratories such as *ETRI* (South Korea); as well as leading universities, such as: *University of Tokyo* (Japan); *Indian Institute of Technology (Madras)* (India); *Edinburgh University, University of Newcastle-upon-Tyne* and *Manchester University* (UK); *UCLA, Cornell, University of Southern California, UC Davis* and *University of Utah* (USA); *EPFL* (Switzerland); *Technical University of Denmark* (Denmark); *Politecnico di Milano* (Italy); *University of Athens* (Greece); *Iran University of Science and Technology* (Iran); *Universidade de Sao Paulo* (Brazil); and *Shanghai Jiao Tong University* (China).

For more details on "MINIMALIST", see item #2 below.

2. THE MINIMALIST CAD PACKAGE. With several of my students, I have developed and released several versions of a large software CAD package for the synthesis of asynchronous controllers, called "MINIMALIST" (see http://www.cs.columbia.edu/~nowick/asynctools). The most recent release, in November 2007, is version 2.0 (see #4. above).

Minimalist (in multiple releases since the late 1990's) has been downloaded to over 100 sites in 18 countries.

MINIMALIST is a complete package for the synthesis and optimization of high-speed asynchronous controllers. It includes a number of practical features: Verilog output, two-level and multi-level logic optimizers, auto-insertion of initialization circuitry, graphic displays, and a top-to-bottom verifier.

The tool has recently been used in collaboration with the NASA Goddard Space Flight Center (2006-2007) for the design of an experimental asynchronous space measurement chip (see item #1 above).

Minimalist, and its logic minimization sub-component, has also been downloaded to companies such as *Intel* and *Sun Microsystems*, and an early prototype was transferred to *IBM Corporation*. The tool was also **being taught in IIT Bombay** in an asynchronous design class in Spring-02, with over 40 students.

HFMIN, IMPYMIN, Espresso-HF. These are our individual tools for hazard-free logic minimization, which are widely used as standalone components. They

have been incorporated into **academic CAD packages** developed by several other research groups, including the 3D system (Yun et al., UC San Diego), ATACS (Myers et al., University of Utah) and the ACK system (Gopalakrishnan et al., University of Utah).

These minimizers have also been used at a number of **companies.** At *Intel Corporation,* "hfmin" is part of their asynchronous CAD tool suite, where it was used in the design of the experimental high-performance instruction-length decoder chip (mid 1990's). The resulting chip was over 3 times faster than Intel's comparable synchronous version. Our tool was critical for the design of several of the control circuits. At *Hewlett-Packard Laboratories,* it was used in the design of an experimental low-power infrared communications chip, and at *AMD Corporation* in the design of an experimental SCSI controller.

TECHNOLOGY TRANSFER

1. Asynchronous Controllers: NASA (Goddard Space Center).
In 2006, a manager at NASA/Goddard invited me to collaborate in designing a **prototype asynchronous measurement circuit for space applications,** using my asynchronous burst-mode controllers and Minimalist CAD tool. *The chip was jointly designed in 2006 by my NASA contact and myself, usng my Minimalist and other asynchronous tools.* The first chip has been fabricated (January 2007), and NASA has funded the development of a second chip (to be taped out in Summer 2007). NASA indicates that this work is receiving positive internal interest, and there is a potential for its use by NASA in future space missions.

2. High-Speed Asynchronous Digital Pipelines: Boeing/Philips Semiconductors (DARPA "CLASS" Project).
From 2005-2007, as a participant in the DARPA CLASS project (led by Boeing Corporation – see "Research Support" above), our high-speed asynchronous "Mousetrap" pipelines have been used extensively. Columbia and UNC were funded to: (a) manually design an experimental pipelined GCD circuit using our Mousetrap asynchronous pipelines; and (b) collaborate with Philips Semiconductors (through its incubated startup company, "Handshake Solutions") to incorporate our Mousetrap pipelines into an experimental version of their commercial asynchronous computer-aided design (CAD) tool flow. Both tasks were successfully completed. Boeing was satisfied with the circuit performance and ease of design in (a), and task (b) demonstrated the feasibility of developing an automated CAD tool flow using our circuits. There is a potential in the future to develop a commercial-strength version of a CAD flow, under direction from Handshake Solutions, which includes our high-speed Mousetrap asynchronous pipelines.

3. High-Speed Asynchronous Digital Pipelines: IBM T.J. Watson Research.
In Summer 2000, researcher from IBM T.J. Watson invited my PhD student, Montek Singh, to transfer our high-speed asynchronous pipeline technology to IBM. Montek spent from August-December 2000, in an IBM group, designing an experimental low-power chip for a pipelined FIR filter. They used our "high-capacity" pipelines, and Montek and the IBM group have reimplemented and taped-out an entire design in modern technology (0.18 micron). (He also designed some plain async FIFO's to calibrate their performance as well.) The chip was evaluated in April-June 2001; it was fully functional, meeting and exceed-

ing basic synchronous performance and power requirements for the next process generation at IBM. In addition, the new design had had the advantage over synchronous ones of dynamically-variable latency, depending on input sample rate.

4. High-Speed Asynchronous Datapaths: Sun Microsystems Labs.
Between 1999-2001, the asynchronous research group at Sun Microsystems, headed by Ivan Sutherland, used my *speculative completion* technique to design a fast asynchronous adder in their experimental FleetZero chip (described in a March 2001 publication at IEEE Async Symposium).

RESEARCH PUBLICATIONS

JOURNAL ARTICLES

Submitted/Under Review:

1. Y. Chen, W. Wei, M. Seok and S.M. Nowick, "Ultra-Low-Voltage Asynchronous Dynamic Pipeline Design with Adaptive Keeper Control." To be submitted to *IEEE Transactions on VLSI Systems* (2015).

Published:

2. C. Vezyrtzis, Y. Tsividis and S.M. Nowick, "Improving the Energy Efficiency of Pipelined Delay Lines Through Adaptive Granularity." *IEEE Transactions on VLSI Systems,* vol. 23:10, pp. 2009-2022 (October 2015).

3. S.M. Nowick and M. Singh, "Asynchronous Design – Part 1: Overview and Recent Advances." *IEEE Design and Test,* vol. 22:3, pp. 5-18 (May/June 2015).

4. S.M. Nowick and M. Singh, "Asynchronous Design – Part 2: Systems and Methodologies." *IEEE Design and Test,* vol. 22:3, pp. 19-28 (May/June 2015).

5. C. Vezyrtzis, W. Jiang, S.M. Nowick and Y. Tsividis, "A Flexible, Event-Driven Digital Filter with Frequency Response Independent of Input Sample Rate." *IEEE Journal of Solid-State Circuits,* vol. 49:10, pp. 2292-2304 (October 2014).

6. M.Y. Agyekum and S.M. Nowick, "Error-Correcting Unordered Codes and Hardware Support for Robust Global Communication." *IEEE Transactions on Computer-Aided Design,* vol. 31:1, pp. 75-88 (January 2012).

7. M. Singh and S.M. Nowick, "Introduction to Special Issue on Asynchrony in System Design." *ACM Journal on Emerging Technologies in Computing Systems,* vol. 7:4, pp. 14:1-14:2 (December 2011).

8. S.M. Nowick and M. Singh, "High-Performance Asynchronous Pipelines: an Overview." *IEEE Design and Test of Computers,* special issue on asynchronous design, vol. 28:5, pp. 8-22 (September/October 2011).

9. M.N. Horak, S.M. Nowick, M. Carlberg and U. Vishkin, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." *IEEE Transactions on Computer-Aided Design,* special section on networks-on-chip, vol. 30:4, pp. 494-507 (April 2011).

10. M. Singh, J.A. Tierno, A. Rylyakov, S. Rylov, and S.M. Nowick, "An Adaptively-Pipelined Mixed Synchronous-Asynchronous Digital FIR Filter Chip Operating at 1.3 GigaHertz." *IEEE Transactions on VLSI Systems,* vol. 18:7, pp. 1043-1056 (July 2010).

11. A. Mitra, W.F. McLaughlin and S.M. Nowick, "Efficient Asynchronous Protocol Converters for Two-Phase Delay-Insensitive Global Communication." *IEEE Transactions on VLSI Systems,* vol. 17:7, pp. 923-928 (July 2009).

12. C. Jeong and S.M. Nowick, "Technology Mapping and Cell Merger for Asynchronous Threshold Networks." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 27:4, pp. 659-672 (April 2008).

13. M. Singh and S.M. Nowick, " MOUSETRAP: High-Speed Transition-Signaling Asynchronous Pipelines." *IEEE Transactions on VLSI Systems,* vol. 15:6, pp. 684-698 (June 2007).

14. M. Singh and S.M. Nowick, "The Design of High-Performance Dynamic Asynchronous Pipelines: Lookahead Style." *IEEE Transactions on VLSI Systems,* vol. 15:11, pp. 1256-1269 (November 2007).

15. M. Singh and S.M. Nowick, "The Design of High-Performance Dynamic Asynchronous Pipelines: High-Capacity Style." *IEEE Transactions on VLSI Systems,* vol. 15:11, pp. 1270-1283 (November 2007).

16. T. Chelcea and S.M. Nowick, "Robust Interfaces for Mixed-Timing Systems." *IEEE Transactions on VLSI Systems,* vol. 12:8, pp. 857-873 (August 2004).

17. Y.W. Li, G. Patounakis, K.L. Shepard and S.M. Nowick, "High-Throughput Asynchronous Datapath with Software-Controlled Voltage Scaling." *IEEE Journal of Solid-State Circuits,* vol. 39:4, pp. 704-708 (April 2004).

18. M. Singh and S.M. Nowick, "Synthesis for Logical Initializability of Synchronous Finite State Machines." *IEEE Transactions on VLSI Systems,* vol. 8:5, pp. 542-57 (October 2000).

19. M.B. Josephs, S.M. Nowick and C.H. van Berkel, "Modeling and Design of Asynchronous Circuits" (*invited paper*). *Proceedings of the IEEE,* vol. 87:2, pp. 234–242 (February 1999).

20. C.H. van Berkel, M.B. Josephs and S.M. Nowick, "Scanning the Technology: Applications of Asynchronous Circuits" (*invited paper*). *Proceedings of the IEEE,* vol. 87:2, pp. 223–233 (February 1999).

21. M. Theobald and S.M. Nowick, "Fast Heuristic and Exact Algorithms for Two-Level Hazard-Free Logic Minimization." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 17:11, pp. 1130-1147 (November 1998).

22. L.A. Plana and S.M. Nowick, "Architectural Optimization for Low-Power Non-Pipelined Asynchronous Systems." *IEEE Transactions on VLSI Systems,* vol. 6:1, pp. 56-64 (March 1998).

23. S.M. Nowick, N.K. Jha and Fu-Chiung Cheng, "Synthesis of Asynchronous Circuits for Stuck-at and Robust Path Delay Fault Testability." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 16:12, pp. 1514-1521 (December 1997).

24. S.M. Nowick, "Design of a Low-Latency Asynchronous Adder Using Speculative Completion." *IEE Proceedings – Computers and Digital Techniques,* vol. 143:5, pp. 301-307 (September 1996).

25. S.M. Nowick and D.L. Dill, "Exact Two-Level Minimization of Hazard-Free Logic with Multiple-Input Changes." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 14:8, pp. 986-997 (August 1995).

26. G. Gopalakrishnan, E. Brunvand, N. Michell and S.M. Nowick. "A Correctness Criterion for Asynchronous Circuit Validation and Optimization." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 13:11, pp. 1309-1318 (November 1994).

27. S.M. Nowick, M.E. Dean, D.L. Dill and M. Horowitz, "The Design of a High-Performance Cache Controller: a Case Study in Asynchronous Synthesis." *Integration: the VLSI Journal,* vol. 15:3, pp. 241-262 (October 1993).

28. D.L. Dill, S.M. Nowick and R.F. Sproull, "Specification and Automatic Verification of Self-Timed

Queues." *Formal Methods in System Design,* vol. 1:1, pp. 29-60 (July 1992).

CONFERENCE PAPERS (published, fully refereed)

Published:

29. J. Demme, B. Rajendran, S.M. Nowick and S. Sethumadhavan, "Increasing Reconfigurability with Memristive Interconnects." In *Proceedings of the ACM/IEEE International Conference on Computer Design (ICCD-15),* New York, NY (October 2015).

30. W. Jiang, K. Bhardwaj, G. Lacourba and S.M. Nowick, "A Lightweight Early Arbitration Method for Low-Latency Asynchronous 2D-Mesh NoC's." In *Proceedings of the ACM/IEEE Design Automation Conference (DAC-15),* San Francisco, CA (June 2015).

31. G. Miorandi, D. Bertozzi and S.M. Nowick, "Increasing Impartiality and Robustness in High- Performance N-Way Asynchronous Arbiters." **Best Paper Finalist.** In *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems (Async-15),* Mountain View, CA (May 2015).

32. G. Miorandi, A. Ghiribaldi, S. Nowick and D. Bertozzi, "Crossbar Replication vs. Sharing for Virtual Channel Flow Control in Asynchronous NoCs: a Comparative Study." In *Proceedings of the 22nd IFIP/IEEE International Conference on Very Large Scale Integration and System-on-Chip (VLSI-SoC-14),* Playa del Carmen, Mexico (October 2014).

33. G. Faldamis, W. Jiang, G. Gill and S.M. Nowick, "A Low-Latency Asynchronous Interconnection Network with Early Arbitration Resolution." In *Proceedings of the ACM/IEEE Asia and South Pacific Design Automation Conference (ASPDAC-14),* SunTec, Singapore (January 2014).

34. C. Vezyrtzis, S.M. Nowick and Y. Tsividis, "A Flexible, Clockless Digital Filter." In *Proceedings of the European Solid State Circuits Conference (ESSCIRC-13),* Bucharest, Romania (September 2013).

35. Y. Chen, M. Seok and S.M. Nowick, "Robust and Energy-Efficient Asynchronous Dynamic Pipelines for Ultra-Low-Voltage Operation Using Adaptive Keeper Control." In *Proceedings of the IEEE International Symposium on Low Power Electronics and Design (ISLPED-13),* Beijing, China (September 2013).

36. J. Liu, S.M. Nowick and M. Seok, "Soft MOUSETRAP: a Bundled-Data Asynchronous Pipeline Scheme Tolerant to Random Variations at Ultra-Low Supply Voltages." In *Proceedings of the IEEE International Symposium on Asynchronous Circuits and Systems (Async-13),* Santa Monica, CA (May 2013).

37. A. Ghiribaldi, D. Bertozzi and S.M. Nowick, "A Transition-Signaling Bundled Data NoC Switch Architecture for Cost-Effective GALS Multicore Systems." **Best Paper Finalist.** In *Proceedings of the ACM/IEEE Design, Automation and Test in Europe Conference (DATE-13),* Grenoble, France (March 2013).

38. C. Vezyrtzis, Y. Tsividis and S.M. Nowick, "Designing Pipelined Delay Lines with Dynamically-Adaptive Granularity for Low-Energy Applications." **Best Paper Award,** Logic and Circuit Design Track. *Proceedings of the IEEE International Conference on Computer Design (ICCD-12),* Montreal, Canada (October 2012).

39. G. Gill, S.S. Attarde, G. Lacourba and S.M. Nowick, "A Low-Latency Adaptive Asynchronous Interconnection Network Using Bi-Modal Router Nodes." In *Proceedings of the ACM Symposium on Networks-on-Chip (NOCS-11),* Pittsburgh, PA (May 2011).

40. M.Y. Agyekum and S.M. Nowick, "A Delay-Insensitive Bus-Invert Code and Hardware Support for Robust Global Communication." In *Proceedings of the ACM/IEEE Design, Automation and Test in Europe Conference (DATE-11),* Grenoble, France (March 2011).

41. M.Cannizzaro, W. Jiang and S.M. Nowick, "Practical Completion Detection for 2-of-N Delay-Insensitive Codes." In *Proceedings of the IEEE International Conference on Computer Design (ICCD-10),* Amsterdam, The Netherlands (October 2010).

42. M.N. Horak, S.M. Nowick, M. Carlberg and U. Vishkin, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." In *Proceedings of the ACM Symposium on Networks-on-Chip (NOCS-10),* Grenoble, France (May 2010).

43. M.Y. Agyekum and S.M. Nowick, "An Error-Correcting Unordered Code and Hardware Support for Robust Global Communication." In *Proceedings of the ACM/IEEE Design, Automation and Test in Europe Conference (DATE-10),* Dresden, Germany (March 2010).

44. P.B. McGee, M.Y. Agyekum, M.A. Mohamed and S.M. Nowick, "A Level-Encoded Transition Signaling Protocol for High-Throughput Asynchronous Global Communication." **Best Paper Finalist.** In *IEEE International Symposium on Asynchronous Circuits and Systems (Async-08),* Newcastle, UK (April 2008).

45. C. Jeong and S.M. Nowick, "Block-Level Relaxation for Timing-Robust Asynchronous Circuits Based on Eager Evaluation." **Best Paper Finalist.** In *IEEE International Symposium on Asynchronous Circuits and Systems (Async-08),* Newcastle, UK (April 2008).

46. P.B. McGee and S.M. Nowick, "An Efficient Algorithm for Time Separation of Events in Concurrent Systems." In *IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* San Jose, CA (November 2007).

47. A. Mitra, W.F. McLaughlin and S.M. Nowick, "Efficient Asynchronous Protocol Converters for Two-Phase Delay-Insensitive Global Communication." In *IEEE Int. Symp. on Asynchronous Circuits and Systems (Async-07),* Berkeley, CA (March 2007).

48. M. Agyekum and S.M. Nowick, "A Cycle-Based Decomposition Method for Burst-Mode Asynchronous Controllers." In *IEEE Int. Symp. on Asynchronous Circuits and Systems (Async-07),* Berkeley, CA (March 2007).

49. C. Jeong and S.M. Nowick, "Optimization of Robust Asynchronous Circuits by Local Input Completeness Relaxation." In *IEEE Asia and South-Pacific Design Automation Conference (ASPDAC-07),* Yokohama, Japan (January 2007)

50. C. Jeong and S.M. Nowick, "Optimal Technology Mapping and Cell Merger for Asynchronous Threshold Networks", In *IEEE Int. Symp. on Asynchronous Circuits and Systems (Async-06),* Grenoble, France (March 2006).

51. F. Shi, Y. Makris, S.M. Nowick, and M. Singh, "Test Generation for Ultra-High-Speed Asynchronous Pipelines." In the *International Test Conference (ITC),* (October 2005).

52. P.B. McGee and S.M. Nowick, "Efficient Performance Analysis of Asynchronous Systems Based on Periodicity." In the *IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS),* Jersey City, NJ (September 2005).

53. P.B. McGee and S.M. Nowick, "A Lattice-Based Framework for the Classification and Design of

Asynchronous Pipelines." In *DAC: ACM/IEEE Design Automation Conference,* Anaheim, CA (June 2005).

54. C. Jeong and S.M. Nowick, "Fast Hazard Detection in Combinational Circuits." In *DAC: ACM/IEEE Design Automation Conference,* San Diego, CA (June 2004).

55. S.M. Nowick and C.W. O'Donnell, "On the Existence of Hazard-free Multi-level Logic." *Async: IEEE International Symposium on Asynchronous Circuits and Systems,* Vancouver, BC, Canada (May 2003).

56. Y.W. Li, G. Patounakis, A. Jose, K.L. Shepard and S.M. Nowick, "Asynchronous Datapath with Software-Controlled On-Chip Adaptive Voltage Scaling for Multirate Signal Processing Applications." **Best Paper Finalist.** *Async: IEEE International Symposium on Asynchronous Circuits and Systems,* Vancouver, BC, Canada (May 2003).

57. T. Chelcea and S.M. Nowick, "Resynthesis and Peephole Transformations for the Optimization of Large-Scale Asynchronous Systems." *DAC: IEEE/ACM Design Automation Conference,* New Orleans, LA (June 2002).

58. M. Singh, J.A. Tierno, A. Rylyakov, S. Rylov, and S.M. Nowick, "An Adaptively-Pipelined Mixed Synchronous-Asynchronous Digital FIR Filter Chip Operating at 1.3 GigaHertz." **Best Paper Finalist.** *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* Manchester, UK (April 2002).

59. T. Chelcea, A. Bardsley, D. Edwards, S.M. Nowick, "A Burst-Mode Oriented Back-End for the Balsa Synthesis System." *DATE: Proceedings of the Design, Automation and Test in Europe Conference,* Paris, France (March 2002).

60. R. Ozdag, M. Singh, P.A. Beerel, S.M. Nowick, "High-Speed Non-Linear Asynchronous Pipelines." *DATE: Proceedings of the Design, Automation and Test in Europe Conference,* Paris, France (March 2002).

61. J. Tierno, A. Rylyakov, S. Rylov, M. Singh, P. Ampadu, S.M. Nowick, M. Immediato, and S. Gowda, "A 1.3 GSample/s 10-tap Full-rate Variable-Latency Self-timed FIR with Clocked Interfaces." *ISSCC: International Solid State Circuits Conference,* Monterey, CA (February 2002).

62. M. Singh and S.M. Nowick, " MOUSETRAP: Ultra-High-Speed Transition-Signaling Asynchronous Pipelines." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Austin, TX (September 2001).

63. M. Theobald and S.M. Nowick, "Transformations for the Synthesis and Optimization of Asynchronous Distributed Control." *DAC: Proceedings of the 38rd IEEE/ACM Design Automation Conference,* Las Vegas, NV (June 2001).

64. T. Chelcea and S.M. Nowick, "Robust Interfaces for Mixed-Timing Systems with Application to Latency-Insensitive Protocols." *DAC: Proceedings of the 38rd IEEE/ACM Design Automation Conference,* Las Vegas, NV (June 2001).

65. T. Chelcea and S.M. Nowick, "Low-Latency FIFO's for Mixed-Clock Systems." *WVLSI: Proceedings of the IEEE Computer Society Annual Workshop on VLSI,* Orlando, FL (April 2000).

66. M. Singh and S.M. Nowick, "Fine-Grain Pipelined Asynchronous Adders for High-Speed DSP Applications." *WVLSI: Proceedings of the IEEE Computer Society Annual Workshop on VLSI,* Orlando,

FL (April 2000).

67. M. Singh and S.M. Nowick, "High-Throughput Asynchronous Pipelines for Fine-Grain Dynamic Datapaths." **Best Paper Award.** *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* Eilat, Israel (April 2000).

68. T. Chelcea and S.M. Nowick, "Low-Latency Asynchronous FIFO's using Token Rings." *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* Eilat, Israel (April 2000).

69. R.M. Fuhrer and S.M. Nowick, "OPTIMISTA: State Minimization of Asynchronous FSMs for Optimum Output Logic." *ICCAD: Proceedings of the IEEE International Conference on Computer-Aided Design,* San Jose, CA (November 1999).

70. M. Benes, S.M. Nowick and A. Wolfe, "A Fast Asynchronous Huffman Decoder for Compressed-Code Embedded Processors." *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* San Diego, CA, pp. 43–56 (April 1998).

71. M. Theobald and S.M. Nowick, "An Implicit Method for Hazard-Free Two-Level Logic Minimization." **Best Paper Finalist.** *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* San Diego, CA, pp. 58–69 (April 1998).

72. R.M. Fuhrer and S.M. Nowick, "OPTIMIST: State Minimization for Optimal 2-Level Logic Implementation." *ICCAD: Proceedings of the IEEE/ACM International Conference on Computer-Aided Design,* San Jose, CA, pp. 308–315 (November 1997).

73. M. Benes, A. Wolfe and S.M. Nowick, "A High-Speed Asynchronous Decompression Circuit for Embedded Processors." *ARVLSI: Proceedings of the 17th Conference on Advanced Research in VLSI,* Ann Arbor, Michigan, pp. 219-236 (March 1997).

74. S.M. Nowick, K.Y. Yun, P.A. Beerel and A.E. Dooply, "Speculative Completion for the Design of High-Performance Asynchronous Dynamic Adders." *Async: IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems,* Eindhoven, Netherlands, pp. 210–223 (March 1997).

75. S.M. Nowick and M. Theobald, "Synthesis of Low-Power Asynchronous Circuits in a Specified Environment." *ISLPED: IEEE International Symposium on Low Power Electronics and Design,* Monterey, CA, pp. 92–95 (March 1997).

76. M. Singh and S.M. Nowick, "Synthesis for Logical Initializability of Synchronous Finite State Machines." *Proceedings of the 10th International Conference on VLSI Design,* Hyderabad, India, pp. 76–80 (January 1997).

77. M. Singh and S.M. Nowick, "Synthesis-for-Initializability of Asynchronous Sequential Machines." *ITC: Proceedings of the IEEE International Test Conference,* Washington, DC, pp. 232–241 (October 1996).

78. L.A. Plana and S.M. Nowick, "Concurrency-Oriented Optimization for Low-Power Asynchronous Systems." *ISLPED: IEEE International Symposium on Low Power Electronics and Design,* Monterey, CA, pp. 151–156 (August 1996).

79. S.M. Nowick, M. Theobald and T. Wu, "Espresso-HF: A Heuristic Hazard-Free Minimizer for Two-Level Logic." *DAC: Proceedings of the 33rd IEEE/ACM Design Automation Conference,* Las Vegas,

NV, pp. 71–76 (June 1996).

80. P. Kudva, G. Gopalakrishnan, H. Jacobson and S.M. Nowick, "Synthesis of Hazard-Free Customized CMOS Complex-Gate Networks Under Multiple-Input Changes." *DAC: Proceedings of the 33rd IEEE/ACM Design Automation Conference,* Las Vegas, NV, pp. 77–82 (June 1996).

81. P.A. Beerel, K.Y. Yun, S.M. Nowick and P. Yeh, "Estimation and Bounding of Energy Consumption in Burst-Mode Control Circuits." *ICCAD: IEEE/ACM International Conference on Computer-Aided Design,* San Jose, CA, pp. 26–33 (November 1995).

82. R.M. Fuhrer, B. Lin and S.M. Nowick, "Symbolic Hazard-Free Minimization and Encoding of Asynchronous Finite State Machines." *ICCAD: Proceedings of the IEEE/ACM International Conference on Computer-Aided Design,* San Jose, CA, pp. 604–611 (November 1995).

83. R.M. Fuhrer, B. Lin and S.M. Nowick, "Algorithms for the Optimal State Assignment of Asynchronous State Machines." *ARVLSI: Proceedings of the 16th Conference on Advanced Research in VLSI,* Chapel Hill, NC, pp. 59–75 (March 1995).

84. S.M. Nowick, N.K. Jha and F.-C. Cheng, "Synthesis of Asynchronous Circuits for Stuck-at and Robust Path Delay Fault Testability." *Proceedings of the 8th International Conference on VLSI Design,* New Delhi, India, pp. 171–176 (January 1995).

85. S.M. Nowick and B. Coates, "UCLOCK: Automated Design of High-Performance Unclocked State Machines." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 434-441 (October 1994).

86. K.Y. Yun, D.L. Dill and S.M. Nowick, "Practical Generalizations of Asynchronous State Machines." *EDAC: Proceedings of the European Conference on Design Automation,* Paris, France, pp. 525–530 (January 1993).

87. S.M. Nowick, M.E. Dean, D.L. Dill and M. Horowitz, "The Design of a High-Performance Cache Controller: a Case Study in Asynchronous Synthesis." **Best Paper Award,** Asynchronous Circuits and Systems Minitrack/ **Best Paper Finalist,** Architecture Track. *HICSS: Proceedings of the IEEE Hawaii International Conference on System Sciences, vol. I* Maui, HI, pp. 419–427 (January 1993).

88. S.M. Nowick and D.L. Dill, "Exact Two-Level Minimization of Hazard-Free Logic with Multiple-Input Changes." *ICCAD: Proceedings of the IEEE/ACM International Conference on Computer-Aided Design,* Santa Clara, CA, pp. 626–630 (November 1992).

89. S.M. Nowick, K.Y. Yun and D.L. Dill, "Practical Asynchronous Controller Design." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 341–345 (October 1992).

90. K.Y. Yun, D.L. Dill and S.M. Nowick, "Synthesis of 3D Asynchronous State Machines." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 346–350 (October 1992).

91. S.M. Nowick and D.L. Dill, "Automatic Synthesis of Locally-Clocked Asynchronous State Machines." *ICCAD: Proceedings of the IEEE International Conference on Computer-Aided Design,* Santa Clara, CA, pp. 318–321 (November 1991).

92. S.M. Nowick and D.L. Dill, "Synthesis of Asynchronous State Machines Using a Local Clock." **Best**

Paper Award, CAD track. *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 192–197 (Oct. 1991).

93. S.M. Nowick and D.L. Dill, "Practicality of State-Machine Verification of Speed-Independent Circuits." *ICCAD: Proceedings of the IEEE International Conference on Computer-Aided Design,* Santa Clara, CA, pp. 266–269 (November 1989).

94. D.L. Dill, S.M. Nowick and R.F. Sproull, "Automatic Verification of Speed-Independent Circuits with Petri Net Specifications." *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Cambridge, MA, pp. 212–216 (October 1989).

INVITED CONFERENCE PAPERS (published, not refereed)

95. E. Brunvand, S.M. Nowick and K.Y. Yun, "Practical Advances in Asynchronous Design and Asynchronous/Synchronous Interfaces." Invited survey article. *DAC: Proceedings of the 36th ACM/IEEE Design Automation Conference,* New Orleans, LA (June 1999).

96. E. Brunvand, S.M. Nowick and K.Y. Yun, "Practical Advances in Asynchronous Design." Invited survey article. *ICCD: Proceedings of the IEEE International Conference on Computer Design,* Austin, Texas, pp. 662-668 (October 1997).

BOOKS

97. R.M. Fuhrer and S.M. Nowick, *Sequential Optimization of Asynchronous and Synchronous Finite-State Machines: Algorithms and Tools,* Kluwer Academic Publishers, Boston, MA (2001). ISBN 0-7923-7425-8.

BOOK CONTRIBUTIONS (published)

98. Y. Tsividis, M. Kurchuk, P. Martinez-Nuevo, S.M. Nowick, S. Patil, B. Schell and C. Vezyrtzis, "Event-Based Data Acquisition and Digital Signal Processing in Continuous Time." Chapter of *Event-Based Control and Signal Processing* (M. Miskowicz, ed.), CRC/Taylor & Francis *(to appear, 2015).*

99. L. Lavagno and S.M. Nowick, "Asynchronous Control Circuits." Chapter 10 of *Logic Synthesis and Verification* (S. Hassoun and T. Sasao, eds.), Kluwer Academic, Boston, MA (pp. 255-284).

100. A. Davis and S.M. Nowick, "An Introduction to Asynchronous Circuit Design." Chapter in *The Encyclopedia of Computer Science and Technology,* vol. 38 (A. Kent and J.G. Williams, eds.), Marcel Dekker, New York (February 1998).

101. A.L. Davis and S.M. Nowick, "Asynchronous Circuit Design: Motivation, Background and Methods." Chapter in *Asynchronous Digital Circuit Design,* G. Birtwistle and A. Davis editors, Springer-Verlag (Workshops in Computing Series, 1995), pp. 1-49.

102. D.L. Dill, S.M. Nowick and R.F. Sproull, "Specification and Automatic Verification of Self-Timed Queues." Chapter in *Formal Verification of Hardware Design (IEEE Tutorial Series)*, M. Yoeli editor (Computer Science Press of IEEE, 1991). (Originally appeared as Stanford University Technical Report, Computer Systems Laboratory, CSL-TR-89-387, August 1989.)

103. S.M. Nowick and D.L. Dill, "Automatic Verification." Chapter in *Synchronization Design for Digital Systems,* T. H.-Y. Meng, Kluwer Academic (1990).

WORKSHOP PAPERS (fully refereed, limited distribution in workshop proceedings)

104. M.Y. Agyekum and S.M. Nowick, "A Delay-Insensitive Bus-Invert Encoding Scheme", Presentation in the *ACM/IEEE International Workshop on Logic and Synthesis (IWLS-10),* Irvine, CA (June 2010).

105. M.Cannizzaro, W. Jiang and S.M. Nowick, "Practical Completion Detection for 2-of-N Delay-Insensitive Codes", Presentation in the *ACM/IEEE International Workshop on Logic and Synthesis (IWLS-10),* Irvine, CA (June 2010).

106. M.Y. Agyekum and S.M. Nowick, "An Error-Correcting Unordered Code for Robust Asynchronous Global Communication." Presentation in the *4th Annual Austin Conference on Integrated Systems and Circuits (ACISC-09),* Austin, TX (October 2009).

107. C. Jeong and S.M. Nowick, "Optimization for Timing-Robust Asynchronous Circuits Based on Eager Evaluation." Presentation in the *ACM/IEEE International Workshop on Logic and Synthesis (IWLS-07),* San Diego, CA (June 2007).

108. C. Jeong and S.M. Nowick, "Technology Mapping for Robust Asynchronous Threshold Networks", Presentation in *ACM Workshop on Timing Issues (TAU-06),* (February 2006) (and full-length paper included in non-published workshop proceedings).

109. C.-H. Li and S.M. Nowick, "An Architecture-Oriented Approach to Code Compression for Embedded Processors." Presentation in *IEEE Workshop on Application-Specific Processors (WASP-05),* (September 22, 2005), affiliated with CODES-05 symposium (and full-length paper included in non-published workshop proceedings).

110. P.B. McGee and S.M. Nowick, "A Unified Lattice-Based Framework for the Classification and Design of Asynchronous Pipelines." Presented at *ACM/SIGDA Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU),* San Francisco, CA (February-March 2005).

111. T. Chelcea and S.M. Nowick, "Resynthesis and Peephole Transformations for the Optimization of Large-Scale Asynchronous Systems." *IWLS: IEEE/ACM International Workshop on Logic and Synthesis,* poster presentation. New Orleans, LA (June 2002).

112. S.M. Nowick, "A Burst-Mode Oriented Back-End for the Balsa Synthesis System." Presented at the *2nd ACiD-WG Workshop (5th funding framework), of the European Community*, Munich, Germany (January 2002).

113. M. Singh and S.M. Nowick, "MOUSETRAP: Ultra-High-Speed Transition-Signaling Asynchronous Pipelines." Presented at *ACM/SIGDA Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU),* Austin, TX (December 2000).

114. M. Theobald and S.M. Nowick, "Control Synthesis and Optimization of Asynchronous Systems Through Transformations." Presented at *ACM International Workshop on Logic Synthesis (IWLS),* Dana Point, CA (May 31-June 2, 2000).

115. R.M. Fuhrer, S.M. Nowick, M. Theobald, N.K. Jha, and L. Plana, "MINIMALIST: An Environment for the Synthesis and Verification of Burst-Mode Asynchronous Machines." Poster presentation at *International Workshop on Logic Synthesis (IWLS),* Lake Tahoe, CA (June 1998).

116. R.M. Fuhrer and S.M. Nowick, "Exact Optimal State Minimization for 2-Level Output Logic." Presented at *International Workshop on Logic Synthesis (IWLS),* Lake Tahoe, CA (June 1998).

117. M. Singh and S.M. Nowick, "State Assignment for Initializability of Synchronous Finite State Machines." Presented at *IEEE International Test Synthesis Workshop (ITSW),* Santa Barbara, CA (March 1996).

118. R.M. Fuhrer, B. Lin and S.M. Nowick, "Symbolic Hazard-Free Minimization and Encoding of Asynchronous Finite State Machines." Presented at *International Workshop on Logic Synthesis (IWLS),* Lake Tahoe, CA (May 1995).

119. S.M. Nowick and B. Coates, "Automated Design of High-Performance Unclocked State Machines." Presented at *ACM/SIGDA Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU),* Malente, Germany, (September 1993).

120. S.M. Nowick and D.L. Dill, "Asynchronous State Machine Synthesis Using a Local Clock." Presented at *International Workshop on Logic Synthesis (IWLS),* Research Triangle Park, NC (May 1991).

WORKSHOP PAPERS (not refereed, limited distribution in workshop proceedings)

121. M. Singh and S.M. Nowick, "Gate-Level Pipelines for High Throughput," The 6th UK Asynchronous Forum, University of Manchester, July 12-13, 1999.

122. E. Brunvand, S.M. Nowick and K.Y. Yun, "Practical Advances in Asynchronous Design and in Asynchronous/Synchronous Interfaces." Invited survey article. *TAU-99: Seventh ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems,* Monterey, CA (1999).

PROFESSIONAL ACTIVITIES

JOURNAL ACTIVITIES

Associate Editor, IEEE Design and Test Magazine, 2015-.

Associate Editor, IEEE Transactions on VLSI Systems (TVLSI), 2015-.

Associate Editor, ACM Journal on Emerging Technologies in Computing Systems (JETC), 2010- (renewed for two 3-year terms).

Associate Editor, IEEE Transactions on Computer-Aided Design (TCAD), 2003-2011 (renewed for four 2-year terms).

Associate Editor, IEEE Transactions on VLSI Systems (TVLSI), 2001-2007 (renewed for three 2-year terms).

Guest Co-Editor, ACM Journal on Emerging Technologies in Computing Systems (JETC), special issue on asynchrony in system design, vol. 7:4, December 2011.

Guest Editor, IEEE Transactions on Computer-Aided Design, special section of best papers from IWLS-02 workshop (vol 22:6, June 2003).

Guest Editor, Proceedings of the IEEE, special issue on asynchronous circuits and systems, vol. 87, number 2, February 1999.

PROFESSIONAL SOCIETY ACTIVITIES

Selection Committee Chair, ACM/SIGDA "Outstanding PhD Dissertation in EDA Award" (2012-2013). This award is provided by the Association of Computing Machinery (ACM), the leading computer science professional society, through its special interest group in electronic design automation (SIGDA), for the Best Dissertation Award in this research area. I am chair of the award committee, which selects the *best international dissertation* in electronic design automation (one of the key areas of the ACM).

Selection Committee Member, ACM/IEEE "A. Richard Newton Technical Impact Award in Electronic Design Automation" (2014-2015). This annual award, provided jointly by the Association of Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE), is to honor an outstanding technical contribution with the greatest impact on the field of electronic design automation. It considers papers that are least 10 years old. *This is the leading award in electronic design automation for long-term technical impact of an individual publication.*

Member, IEEE Fellows Evaluation Committee, *Computer Society* (2012). I was invited to serve as a member of this committee, which contributes to selecting IEEE Fellows from a pool of international nominations.

GOVERNMENT AGENCY ACTIVITIES

Invited Participant: NSF Workshop on Ultra-Low Latency Wireless Networks (2015). I was invited to participate in a 2-day national study group, sponsored by NSF, on the future of wireless technology to achieve extreme low-latency communication, both for macro-level networks as well as micro-level on-chip networks. I participated in a white paper documenting the outcomes of the workshop, that is expected to be used by NSF for defining future funding initiatives in this area. The workshop had under 40 attendees. Phoenix, AZ, 3/26-27/15 (http://inlab.lab.asu.edu/nsf/#).

Invited Participant: NSF/DARPA/DOE/NASA Workshop on System-on-Chip Design for High-Performance Computing ("SoC for HPC") (2014). I was invited to participate, and give a talk on my research, at an invitation-only 2-day national study group, sponsored by NSF, DARPA, DOE, NASA, and Sandia and Lawrence Berkeley National Laboratories, on the future of designing cost-effective high-performance parallel computers for both big data and consumer applications. The workshop had under 35 attendees, with only 10 invited from academia. Denver, CO, 8/26-27/14 (https://sites.google.com/a/lbl.gov/socforhpc/).

EXTERNAL REVIEW BOARDS/VISITING COMMITTEES

Member, Boston University, ECE Department Visiting Committee. Member of standing committee which serves as an external review panel, to evaluate and support the department's growth (first site visit, 9/14-9/15/09).

CONFERENCE ACTIVITIES

Topic Area Co-Chair (2015): DATE Conference, Program Committee, "Network on Chip" area, *IEEE/ACM Design, Automation and Test in Europe Conference,* Grenoble, France (March 2015).

As topic area co-chair, I am responsible for handling approximately 60 paper submissions per year in this area, and selecting approximately 18 subcommittee members, and leading a sub-committee evaluation, in one of the top international digital CAD and design conferences.

Selection Committee Member (2014): William J. McCalla Best Paper Award, ICCAD Conference, *ACM/IEEE International Conference on Computer-Aided Design,* San Jose, CA (November 2014).

This is one the leading international conference on digital design and automation. I was invited to join the small (4 member) committee to select one of the two Best Paper awards.

Subcommittee Chair (2011-2013): DAC Conference, Program Committee, "High-Level and Logic Synthesis, Circuit-Level Optimization, and FPGA" area, *IEEE/ACM Design Automation Conference.*

This is the leading international conference on digital design and automation. It receives several hundred paper submissions each year. The program committee

is divided into 14 core research subcommittees (plus 6 new subcommittees in embedded systems). I was invited to be chair (2012-13) and co-chair (2011) of one subcommittee, which handles the wide area of *high-level and logic synthesis, circuit-level optimization and FPGA's.* I am responsible for leading the evaluation and final selection of all papers in this area.

Selection Committee Member (2010): Best Paper Award, DAC Conference, *IEEE/ACM Design Automation Conference,* Anaheim, CA (June 2010).

This is the leading international conference on digital design and automation. I was invited to join the small (5 member) subcommittee to select the Best Paper award.

Topic Area Chair (2009-10)/Co-Chair (2008): DATE Conference, Program Committee, "Logic and Technology-Dependent Synthesis for Deep-Submicron Circuits" area, *IEEE/ACM Design, Automation and Test in Europe Conference,* Nice, France (March 2009, March 2010).

As topic area chair/co-chair, I am responsible for handling approximately 30 paper submissions per year in this area, and selecting approximately 10 sub-committee members, and leading a sub-committee evaluation, in one of the top international digital CAD and design conferences.

Track Chair (2005): ICCD Conference, Program Committee, "Tools and Methodology" track, *IEEE International Conference on Computer Design (ICCD),* San Jose, CA (October 2005).

As track chair, I am holding the position of a Program Committee Subchair responsible for *one-fifth* of the conference's program committee. The position is semi-autonomous: I selected a co-track chair, and 24 track program committee members. My track committee handled 81 paper submissions, in its own independent program committee meeting which I ran on June 20-21, 2005.

General Co-Chair (2005): Async Symposium, *11th IEEE International Symposium on Asynchronous Circuits and Systems* ("Async-05" Symposium), Columbia University, New York, NY (April 2005).

I was general co-chair, local arrangements co-chair, and host of the 11th Async Symposium at Columbia University. The symposium had over 100 attendees, and 60 paper submissions, and 21 accepted papers. Invited speakers included: (i) *Bob Colwell (keynote),* former manager of several recent Pentium projects, and chief Intel architect; and (ii) *Ivan Sutherland,* Turing award winner, and inventor of computer graphics.

Program Chair (2002): IWLS Workshop, *11th IEEE/ACM International Workshop on Logic and Synthesis* ("IWLS" Workshop), New Orleans, LA (June 2002).

Focus Group Chair (2001): IWLS Workshop, *10th ACM International Workshop on Logic and Synthesis* ("IWLS" Workshop), Lake Tahoe, CA (June 2001).

Best Paper Award Chair (2001): Async Symposium, *7th IEEE International*

Symposium on Asynchronous Circuits and Systems ("Async-01" Symposium), Salt Lake City, UT (March 2001).

Program Co-Chair (1999): Async Symposium, *5th IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems* ("Async-99" Symposium), Barcelona, Spain (April 1999).

Co-Founder/Program Committee Co-Chair (1994): Async Symposium, *1st IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems* ("Async-94" Symposium), Salt Lake City, UT, November 1994.

I co-founded this international symposium series with 3 colleagues from University of Utah (E. Brunvand, A.L. Davis, G. Gopalakrishnan). We obtained an NSF grant (see above) to help establish the symposium series. We also obtained sponsorship of IEEE Computer Society and IEEE Technical Committee on VLSI, and cooperation with IFIP Working Groups 10.2 and 10.5.

The symposium was a success, with nearly 100 attendees. There were 74 paper submissions and 25 accepted papers. Proceedings were published by IEEE Computer Society.

The series itself has maintained excellent momentum. The 2nd Symposium (Japan 1996), 3rd Symposium (Netherlands 1997), 4th Symposium (San Diego 1998) and 5th Symposium (Spain 1999) each had 95-115 attendees and 58-70 paper submissions.

FUNDING AGENCIES

Invited Participant/Speaker: DARPA Workshop on Clockless Logic. Arlington, VA, August 8, 2002. DARPA convened an exploratory workshop to consider a major new funding initiative in the area of asynchronous (i.e., clockless) digital circuits. I was an invited participant and speaker, one of only about 5 speakers from academia. The result of the meeting was positive: in early 2003, DARPA announced a significant new funding initiative in clockless logic.

Invited Presenter/Panelist: "Making the Most of Your CAREER Award." 1st NSF CAREER Program PI Meeting, CISE Division (*Plenary Session*), National Science Foundation (1/11/99).

NSF Grant Review Panelist, CISE Division, National Science Foundation (5/21-5/22/14).

NSF Grant Review Panelist, CISE Division, National Science Foundation (3/14-3/15/13).

NSF Grant Review Panelist, CISE Division, National Science Foundation (3/7-3/8/11).

NSF Grant Review Panelist, CISE Division, National Science Foundation (4/12-4/13/10).

NSF Grant Review Panelist, CISE Division, National Science Foundation (3/26-3/27/09).

NSF ITR Award Grant Review Panelist, CISE Division, National Science Foundation (4/29-4/30/04).

NSF CAREER Award Review Panelist, CISE Division, National Science Foundation (10/25/01).

NSF Grant Review Panelist, CISE Division, National Science Foundation (3/4-3/5/99).

MEDIA INTERVIEWS

Cisco's "The Network" (Cisco's technology news site), *"The Internet of Everything Goes To School,"* Anne Waxman, 1/28/2015. Story on educational programs at Columbia and other leading schools, on the Internet-of-Things. (URL: http://newsroom.cisco.com/feature-content?type=webcontent&articleId=1576720)

EE Times (Europe), *"Asynchronous EDA Tools Available for Free Download,"* Peter Clarke, 12/11/2007. Story on release of our "CaSCADE" asynchronous tool package, including 3 of our CAD tools. (URL: http://www.eetimes.eu/204801096)

The New York Times, *Circuits Section,* "What's Next" Column, (August 22, 2002). *"Faster Chips That March to Their Own Improvised Beat."* (URL: http://www.cs.columbia.edu/ nowick/22NEXT.pdf)

Technology Review Magazine *(cover story)* (based in MIT): October 2001, vol. 104:8 (pp. 36-41). *"It's Time for Clockless Chips."*
(URL: http://www1.cs.columbia.edu/ nowick/technology-review-article-10-01.pdf)

PROGRAM COMMITTEES

Program Committee Member, **DAC:** *IEEE/ACM Design Automation Conference* (2002-2004, 2011-2013)

Program Committee Member, **DATE:** *IEEE/ACM Design, Automation and Test in Europe Conference* (2000-2002, 2005-2016)

Program Committee Member, **ICCAD:** *IEEE/ACM International Conference on Computer-Aided Design* (1998-1999)

Program Committee Member, **ICCD:** *IEEE International Conference on Computer Design* (1995-1999, 2005-2007)

Program Committee Member, **NOCS:** *ACM Symposium on Networks-on-Chip* (2010-2016)

Program Committee Member, **Async:** *IEEE International Symposium on Asynchronous Circuits and Systems* (1994, 1996-2000, 2002, 2004, 2006-2016)

Steering Committee Member, **Async:** *IEEE International Symposium on Asynchronous Circuits and Systems* (1994-2007, 2009-2012)

Program Committee Member, **INA-OCMC:** *International Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip* (held in conjunction with the HiPEAC Conference) (2012-2015)

Program Committee Member, **IWLS:** *IEEE/ACM International Workshop on Logic and Synthesis* (1999-2016)

Program Committee Member, **ARVLSI:** *Conference on Advanced Research in VLSI* (1997, 1999, 2001)

Program Committee Member, **VLSI Design:** *IEEE International Conference on VLSI Design* (1998)

Program Committee Member, **FMGALS:** *Formal Methods in GALS Design* (2009)

Program Committee Member, **TAU:** *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems* (1997)

Program Committee Member, **GLVLSI:** *IEEE Great Lakes Symposium on VLSI* (1997)

Program Committee Member, **Israel Workshop on Asynchronous VLSI Circuits and Systems** (1995)

INVITED TALKS: Distinguished Lectures and Keynotes

17th ACM/IEEE System Level Interconnection Prediction (SLIP) Workshop, "Asynchronous and GALS NoC's for Scalable High-Performance Computer Systems." **Keynote Talk**, San Francisco, CA, 6/6/15.

Texas A&M University, Department of Electrical and Computer Engineering, "Designing a Low-Power and Low-Latency Network-on-Chip Switch Architecture for Cost-Effective GALS Multicore Systems." **Computer Engineering Eminent Scholar Seminar series** (invited talk). College Station, TX, 4/2/13.

2002 IEEE International Symposium on Computer Architecture (ISCA), "GALS Session" Keynote. Workshop on Complexity-Effective Design. Invited talk on mixed-timing interfaces, May 2002.

INVITED TALKS: Conferences and Workshops

Invited Speaker: EPFL Workshop on Logic Synthesis and Verification. The workshop included only invited speakers who are leading researchers in the field, to summarize and define the state-of-art and future innovative directions. "Optimization of Robust Asynchronous Threshold Networks Using Local Relaxation Techniques." Ecole Polytechnique Federale de Lausanna, Lausanne, Switzerland, 12/10-12/11/15.

Invited Speaker: NSF/DARPA/DOE/NASA Workshop on System-on-Chip Design for High-Performance Computing ("SoC for HPC"). Invited to give a talk at an invitation-only national study group, sponsored by NSF, DARPA, DOE, NASA, and Sandia and Lawrence Berkeley National Laboratories, on the future of designing cost-effective high-performance parallel computers for both big data and consumer applications. Denver, CO, 8/26/14.

Invited Speaker: Clockless Logic Symposium, Washington University. I was one of 6 invited speakers at a special anniversary symposium at Washington

University (March 2004), celebrating the 150th anniversary of the university and the 30th anniversary of the completion of the asynchronous 'Macromodules Project'. Ivan Sutherland gave the opening technical talk.

See Washington University's web page for publicity: *"Symposium Gathers Computing Greats to Decide Whether to Go Clockless"*, http://news-info.wustl.edu/tips/page/normal/727.html and http://cse.seas.wustl.edu/clockless. The symposium was attended by approximately 400 people, and opened by the former University Chancellor.

2002 Summer School on Asynchronous Design, TIMA Institute, Grenoble, France. Invited to give intensive half-day lab course on my MINIMALIST CAD package (presented four times), as well as introductory tutorial on hazard-free logic synthesis. Grenoble, France, July 2002.

2nd ACiD-WG Workshop (5th funding framework), of the European Community: "MINIMALIST: A CAD Environment for the Synthesis and Optimization of Burst-Mode Asynchronous Controllers." Munich, Germany, 1/29/02.

Async-00: Sixth IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems, "Synthesis of Burst-Mode Asynchronous Controllers and the MINIMALIST CAD Package," S.M. Nowick. Invited Tutorial and Hands-On Session (2 hours, presented twice). Eilat, Israel 4/3/00.

DAC-99: 36th ACM/IEEE Design Automation Conference, "Practical Advances in Asynchronous Design and Asynchronous/Synchronous Interfaces," E. Brunvand, S.M. Nowick and K.Y. Yun. Embedded Tutorial. Organizer: S.M. Nowick. New Orleans, LA, 6/22/99.

TAU-99: Seventh ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, "Practical Advances in Asynchronous Design and Asynchronous/Synchronous Interfaces," E. Brunvand, S.M. Nowick and K.Y. Yun. Invited tutorial. Organizer: S.M. Nowick. Monterey, CA, 3/8/99.

Third ACiD-WG Workshop (ACiD = Asynchronous Circuit Design), Newcastle upon Tyne, UK, 1/17-1/19/99. Sponsored by the European Union "Esprit" Project. **Invited tutorial (2 parts):**

- "Burst-Mode: Specification, Synthesis, and Applications," 1/18/99.
- "Burst-Mode: Optimization Algorithms and the MINIMALIST CAD Package," 1/18/99.

ICCD-97: IEEE International Conference on Computer Design, "Practical Advances in Asynchronous Design," E. Brunvand, S.M. Nowick and K.Y. Yun. Embedded tutorial. Austin, TX, 10/15/97.

1995 Israel Workshop on Asynchronous VLSI Circuits and Systems. Invited tutorial and workshop presentations. Sea of Galilee, Israel, 3/19-3/22/95.

1994 IEEE Workshop on Computer Elements, "Automated Design of High-Performance Asynchronous State Machines." Vail, CO, 6/26-6/29/94.

1993 Winter Workshop on VLSI, "The Design of a High-Performance Cache Controller: a Case Study in Asynchronous Synthesis." Asilomar Conference Center, Pacific Grove, CA, 2/9/93.

INVITED TALKS: Universities and Industry

D.E. Shaw Research, "Designing a Low-Power and Low-Latency Network-on-Chip Switch Architecture for Cost-Effective GALS Multicore Systems." New York, NY, 10/14/15.

Intel, "Asynchronous and GALS NoC's for Scalable High-Performance Computing Systems." Joint presentation with Prof. Davide Bertozzi (University of Ferrara, Ferrara Italy). Hillsboro, OR, 10/9/15.

AMD Research, "Designing a Low-Power and Low-Latency Network-on-Chip Switch Architecture for Cost-Effective GALS Multicore Systems." Boxborough, MA (also broadcast to multiple AMD sites), 11/18/13.

Texas A&M University, Department of Electrical and Computer Engineering, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." College Station, TX, 11/12/13.

IBM T.J. Watson Research Center, "Designing a Low-Power and Low-Latency Network-on-Chip Switch Architecture for Cost-Effective GALS Multicore Systems." Yorktown Heights, NY, 11/1/13.

AMD Research, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Boxborough, MA (by telecom), 5/7/13.

University of Texas (Austin), Department of Electrical and Computer Engineering, "Designing a Low-Power and Low-Latency Network-on-Chip Switch Architecture for Cost-Effective GALS Multicore Systems." Austin, TX, 4/1/13.

University of Massachusetts (Amherst), Department of Electrical and Computer Engineering, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Amherst, MA, 10/21/11.

Universita di Bologna, DEIS, "Trends in Electronics" series, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Bologna, Italy, 3/22/11.

Ecole Polytechnique Federale de Lausanne (EPFL), Institute of Electrical Engineering and Integrated Systems Center, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Lausanne, Switzerland, 3/21/11.

CEA-LETI, Minatec, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Grenoble, France, 3/18/11.

Georgia Institute of Technology, School of Electrical and Computer Engineering, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Atlanta, GA, 2/7/11.

Carnegie-Mellon University, Department of Electrical and Computer Engineering, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Pittsburgh, PA, 12/3/10.

Stanford University, Department of Electrical Engineering, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Stanford, CA, 5/21/10.

Portland State University, Department of Electrical and Computer Engineering, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Portland, OR, 5/20/10.

Duke University, Department of Electrical and Computer Engineering, colloquium series, "A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors." Durhum, NC, 4/14/10.

University of Toronto, Department of Electrical and Computer Engineering, "Recent Advances in Designing Clockless Digital Systems." Toronto, Ontario, Canada, 11/3/09.

Columbia University, EE Department, CISL Seminar Series, "Recent Advances in Designing Clockless Digital Circuits." New York, NY, 11/21/08.

NASA Goddard Space Flight Center, (invited by Wes Powell, associate director of microelectronics). "Advances in Designing Clockless Digital Systems." Greenbelt, MD, 1/22/08.

Princeton University, Department of Electrical and Computer Engineering, "MOUSETRAP: Designing High-Speed Asynchronous Digital Pipelines." Princeton, NJ, 12/4/06.

Cooper Union, Department of Electrical Engineering, "MOUSETRAP: Designing High-Speed Asynchronous Digital Pipelines." New York, NY, 11/15/06.

IBM T.J. Watson Research Center, "Efficient Performance Analysis of Asynchronous and Mixed-Timing Systems." Yorktown Heights, NY, 12/12/05.

University of Maryland, ECE Department, "Automated Compilation of Asynchronous Digital Systems." College Park, MD, 11/14/05.

University of Manchester, Department of Computer Science, (Manchester, UK). 3 talks (9/02, 10/02, 2/03).

University of California, Berkeley, EECS Electronic Systems Design Seminar Series, "Low-Latency Interfaces for Mixed-Timing Domains." Berkeley, CA, 11/28/01.

University of Michigan, EECS Department VLSI Seminar Series, "MOUSETRAP: Designing High-Speed Asynchronous Digital Pipelines." Ann Arbor, MI, 11/19/01.

Theseus Logic, Inc. "Synthesis of Burst-Mode Asynchronous Controllers, and the MINIMALIST CAD Package." Sunnyvale, CA, 3/6/00.

Columbia University, Department of Computer Science, "Asynchronous Circuits: Recent Advances in the Design of Clockless Systems." NY, NY, 9/27/99.

University of Rochester, Department of Electrical and Computer Engineering, "Asynchronous Circuits: an Introduction and Case Study — a Fast Huffman Decoder for Compressed-Code Embedded Processors." Rochester, NY, 5/21/99.

Stanford University, Computer Systems Laboratory, "Asynchronous Circuits: an Introduction and Case Study — a Fast Huffman Decoder for Compressed-Code Embedded Processors." Stanford, CA, 5/18/99.

Princeton University, Department of Electrical and Computer Engineering, "Asynchronous Circuits: an Introduction and Case Study — a Fast Huffman Decoder for Compressed-Code Embedded Processors." Princeton, NJ, 4/28/99.

University of Michigan, Department of Electrical and Computer Engineering, "Asynchronous Circuits: an Introduction and Case Study — a Fast Huffman Decoder for Compressed-Code Embedded Processors." Ann Arbor, MI, 4/15/99.

University of Texas, Departments of Computer Science and Electrical/Computer Engineering, "Algorithms and Tools for the Synthesis, Optimization and Testability of Asynchronous Controllers." Austin, TX, 4/9/99.

University of Illinois, Department of Electrical and Computer Engineering, "Algorithms and Tools for the Synthesis, Optimization and Testability of Asynchronous Controllers." Urbana, IL, 4/5/99.

University of Utah, Department of Computer Science, "Recent Advances in CAD Tools and Algorithms for Asynchronous and Synchronous Controllers." Salt Lake City, UT, 3/24/99.

Intel Corporation, "Synthesis of Burst-Mode Asynchronous Controllers, and the MINIMALIST CAD Package." Santa Clara, CA, 3/12/99.

Intel Corporation, Strategic CAD Laboratory, "Recent Advances in CAD Tools and Algorithms for Asynchronous and Synchronous Controllers." Hillsboro, OR, 3/10/99.

Philips Research Laboratories, "Current Research in Asynchronous Design at Columbia University: an Overview." Eindhoven, The Netherlands, 1/27/99.

South Bank University, Centre for Concurrent Systems and VLSI, "A Fast Asynchronous Huffman Decoder for Compressed-Code Embedded Processors." London, UK, 1/25/99.

University of Manchester, Department of Computer Science, "Current Research in Asynchronous Design at Columbia University: an Overview." Manchester, UK, 1/22/99.

Stanford University, Stanford "CAD Day" presentation, "MINIMALIST: An Environment for Synthesis and Testability of Burst-Mode Asynchronous Machines." Stanford, CA, 11/12/98.

University of California, San Diego, Department of Electrical and Computer Engineering, "The Design of Low-Power and High-Performance Asynchronous Systems." La Jolla, CA, 6/6/97.

University of California, Los Angeles, Department of Computer Science, "The Design of Low-Power and High-Performance Asynchronous Systems." Los Angeles, CA, 6/5/97.

University of Utah, Department of Computer Science, "The Design of High-Performance Asynchronous Systems." Salt Lake City, UT, 1/10/97.

NEC Research Laboratory, "The Design of High-Performance Asynchronous Datapaths." Princeton, NJ, 12/10/96.

Sun Laboratories, "The Design of High-Performance Asynchronous Datapaths." Palo Alto, CA, 11/8/96.

Intel Corporation, "The Design of High-Performance Asynchronous Datapaths." Santa Clara, CA, 11/7/96.

University of California, Irvine, Department of Computer Science, "The Design of High-Performance Asynchronous Datapaths." Irvine, CA, 11/5/96.

University of Aizu, Department of Computer Science, (Aizu-Wakamatsu, Japan).
Invited lecture series:

- "A CAD Framework for the Design, Optimization and Testability of Asynchronous Controllers," 3/27/96.
- "Burst-Mode Sequential Machines: Basic Synthesis Algorithms and Optimal State Assignment," 3/27/96.
- "Hazard-Free Combinational Synthesis: Logic Minimization and Testability," 3/25/96.

IBM T.J. Watson Research Center, "A CAD Framework for the Design, Optimization and Testability of Asynchronous Controllers." Yorktown Heights, NY, 1/26/96.

University of Utah, Department of Computer Science "Symbolic Hazard-Free Minimization and Encoding of Asynchronous Finite State Machines." Salt Lake City, UT, 5/30/95.

IMEC Laboratories, "Automatic Synthesis of Burst-Mode Asynchronous Controllers". Leuven, Belgium, 9/7/93.

University of Calgary, Department of Electrical Engineering, "Automated Design of High-Performance Unclocked State Machines". Calgary, Alberta, Canada, 9/3/93.

Stanford University, Department of Computer Science, "Automated Design of High-Performance Unclocked State Machines". Stanford, CA, 8/20/93.

University of Washington, Department of Computer Science, "Automated Design of High-Performance Unclocked State Machines". Seattle, WA, 8/19/93.

University of Utah, Department of Computer Science "Exact Two-Level Minimization of Hazard-Free Logic with Multiple-Input Changes". Salt Lake City, UT, 5/10/93.

Princeton University, Department of Electrical Engineering, "Automatic Synthesis of Burst-Mode Asynchronous Controllers". Princeton, NJ, 5/4/93.

University of Waterloo, Department of Computer Science "Automatic Synthesis of Burst-Mode Asynchronous Controllers". Waterloo, Ontario, Canada, 4/30/93.

HaL Computers, "Automatic Synthesis of Locally-Clocked Asynchronous State Machines". Campbell, CA, 2/28/92.

University of Utah, Department of Computer Science, "Automatic Synthesis of Locally-Clocked Asynchronous State Machines". Salt Lake City, UT, 11/26/91.

Cirrus Logic,"Synthesis of Asynchronous State Machines Using a Local Clock". Milpitas, CA, 9/6/91.

JOURNAL AND CONFERENCE REFEREEING

IEEE Transactions on Computers; IEEE Transactions on Computer-Aided Design; IEEE Transactions on Circuits and Systems; IEEE Transactions on VLSI Systems; INTEGRATION: the VLSI journal; IEEE Design and Test of Computers; IEE Electronic Letters (UK); VLSI conference; International Conference on Computer-Aided Design; International Conference on Computer Design; Design Automation Conference; Hawaii International Conference on System Sciences; NSF proposals.

DEPARTMENTAL

CURRENT PHD STUDENTS

Kshitij Bhardwaj (September 2012- present)

Weiwei Jiang (September 2009- present)

Kunal Mahajan (September 2014- present)

FORMER POST-DOCTORAL RESEARCH SCIENTISTS

Gennette Gill (February 2010 - August 2011)

FORMER PHD STUDENTS

Christos Vezyrtzis (EE) (September 2009 - July 2013). Thesis defense: 5/3/13; thesis deposit: 7/29/13. (Currently Research Staff Member, IBM T.J. Watson Research Center, Yorktown, NY.) (co-advisor: Prof. Yannis Tsividis, Columbia EE Department)

Melinda Agyekum (September 2004 - October 2010). Thesis defense: 10/29/10. (Currently a program manager, Enterprise Storage Backend, Google Corporation, New York, NY.)

Peggy McGee (September 2003 - 2010). Thesis defense: 8/5/09. (Currently a senior R&D design engineer in the Power Compiler group at Synopsys Corporation, Sunnyvale, CA.)

Cheoljoo Jeong (May 2002 - December 2008). Thesis defense: 10/22/07; thesis deposit: 12/19/07. (Currently a senior design engineer at Cadence Design Systems, Santa Clara, CA.)

Tiberiu Chelcea (September 1997 - 2004). Thesis defense: 12/8/03. (Currently a Research Scientist in the department of computer science at Carnegie-Mellon University.)

Montek Singh (September 1994 - December 2001). Thesis defense: 12/12/01; thesis deposit: 1/3/02. (Currently a tenured associate professor of computer science at University of North Carolina, Chapel Hill.)

Michael Theobald (September 1994 - present). Thesis defense: 12/18/01. (Currently a researcher at D.E. Shaw Laboratory; formerly a Research Scientist in the department of computer science at Carnegie-Mellon University, working with Prof. Ed Clarke.)

Robert M. Fuhrer (December 1993 - December 1998). Thesis defense: 12/14/98; thesis deposit: 5/7/99. (Currently at IBM Research, T.J. Watson.)

Moustafa Mohamed (September 2006 - October 2007) (withdrew from program)

Cheng-Hong Li (September 2002 - September 2004) (transferred to Luca Carloni)

Yu Chen (September 2012 - December 2013) (transferred to Yannis Tsividis)

FORMER MS STUDENTS: WITH THESIS

Marco Cannizzaro (April 2009 - October 2009) (*funded*)
(co-MS advisor/co-chair of MS thesis committee, Politecnico di Torino, Italy)

Michael Horak (June 2007 - August 2008)
(co-MS advisor/co-chair of MS thesis committee, University of Maryland, College Park)

FORMER MS STUDENTS: OTHER

Ankit Pradhan (January - May 2014)

Clementine Barbet (September 2013 - May 2014)

Kiran Kumar Mada (September - December 2013)

Adil Sadik (September 2012 - December 2012)

Georgios Faldamis (September 2011 - December 2012)

Sumedh Attarde (September 2010 - May 2011)

Geoffray Lacourba (September 2010 - August 2011)

Weiwei Jiang (EE) (June - August 2009) (*funded*)

Harsh Parekh (Comp Eng) (January - August 2009) (*funded*)

Srikanth Viswanathan (Comp Eng) (January - August 2009) (*funded*)

Ashwath Narasimhan (Comp Eng) (January - May 2009)

Roopa Kakarlapudi (Comp Eng) (January - May 2009)

Walter Dearing (January - August 2007)

Melinda Agyekum (September 2002 - June 2004)

Amitava Mitra (September 2002 - December 2003)

PHD THESIS COMMITTEES

Hung-Yi Li (CS), "Supervised Design-Space Exploration" (6/2/15 defense); advisor: Prof. Luca Carloni.

John Demme (CS), "Overcoming the Intuition Wall: Measurement and Analysis in Computer Architecture" (1/22/14 defense); advisor: Prof. Simha Sethumadhavan.

Melinda Y. Agyekum (CS), "Designing Delay-Insensitive Codes for Robust Global Asynchronous Communication" (10/29/10 defense); advisor: Prof. Steven Nowick.

Navid Toosizadeh *ECE Department, University of Toronto*, " Enhanced Synchronous Design Using Asynchronous Techniques" (11/3/09 defense); advisor: Prof. S. Zaky.

Cheng-Hong Li (CS), "Methods for Performance Optimization of Latency-Insensitive Systems"(7/22/09 defense); advisor: Prof. Luca Carloni.

Peggy B. McGee (CS), "On the Timing Behavior of Concurrent Digital Systems: Analysis, Tools and Applications" (8/5/09 defense); advisor: Prof. Steven Nowick.

Aydin O. Balkan *ECE Department, University of Maryland, College Park*, " Mesh-of-Trees Interconnection Network for an Explicitly Multi-Threaded Parallel Computer Architecture" (7/16/08 defense); advisor: Prof. Uzi Vishkin.

Cheoljoo Jeong (CS), "Synthesis and Optimization of Robust Asynchronous Threshold Networks" (12/19/07 deposit); advisor: Prof. Steven Nowick.

Yee William Li (EE), "Self-Timed Techniques in Digital Signal Processing" (5/24/05); advisor: Prof. Kenneth Shepard (EE).

Tiberiu Chelcea (CS), "Design and Optimization of Large-Scale Asynchronous and Mixed-Timing Systems" (12/8/03); advisor: Prof. Steven Nowick.

S. Henry Li (EE), "Low-Energy Communication Processor with Dynamic Variable Power-Supply Scaling"(2/1/02); advisor: Prof. Charles Zukowski.

Michael Theobald (CS), "Efficient Algorithms for the Design of Asynchronous Control Circuits" (12/18/01); advisor: Prof. Steven Nowick.

Montek Singh (CS), "High-Speed Asynchronous Digital Pipelines" (12/12/01); advisor: Prof. Steven Nowick.

Euiseok Kim (*Kwangju Institute of Science and Technology (K-JIST),* South Korea), "A Study on High-Level Synthesis of Asynchronous VLSI Systems" (6/16/01); advisor: Prof. D.-I. Lee. (Invited as *External Reviewer*.)

Shao-Yi Wang (EE), "Energy Reduction in CMOS Logic Arrays Through Partitioning" (1/24/01); advisor: Prof. Charles Zukowski.

J.W.J.M. Rutten (EE, *Technical University of Eindhoven,* The Netherlands), "Synthesis of Asynchronous Burst-Mode Finite State Machines" (4/19/00); advisor: Prof. Jochen Jess. (Invited as *2nd Promoter*.)

Robert M. Fuhrer (CS), "Sequential Optimization of Asynchronous and Synchronous Finite-State Machines: Algorithms and Tools" (12/14/98); advisor: Prof. Steven M. Nowick.

Fu-Chiung (John) Cheng (CS), "Synthesizing Iterative Functions into High Performance Delay-Insensitive Tree Circuits" (4/22/98); advisor: Prof. Stephen Unger.

Hui Lei (CS), "Uncovering and Exploiting the Intrinsic Correlations between File References" (12/17/97); advisor: Prof. Dan Duchamp.

Luis Plana (CS), "Contributions to the Design of Asynchronous Macromodular Systems" (12/16/97); advisor: Prof. Stephen Unger.

Christophe R. Tretz (EE), "Sizing and Topology in SOI and Bulk Low-Power High-Speed CMOS Circuits" (5/16/97); advisor: Prof. Charles Zukowski.

Ping-Chang Yen (IEOR), "On the Architecture of Object-Oriented Scheduling Systems" (8/29/95); advisor: Prof. Michael Pinedo.

Danilo Florissi (CS), "Isochronets: A High-Speed Network Switching Architecture" (4/21/95); advisor: Prof. Yechiam Yemini.

Bill Schilit (CS), "Context-Aware Software Reconfiguration Supporting Mobile Distributed Computing" (12/12/94); advisor: Prof. Dan Duchamp.

Hong Shi (EE), "Design, Analysis, and Optimization of Broadband ATM Switches Implemented in VLSI" (6/30/94); advisor: Prof. Omar Wing.

Gary L. Dare (EE), "Accuracy Management for Delay-Oriented Control in Mixed-Mode Simulation of Digital VLSI Circuits" (12/14/93); advisor: Prof. Charles Zukowski.

Carl Tait (CS), "A File System for Mobile Computing" (4/20/93); advisor: Prof. Dan Duchamp.

MS THESIS COMMITTEES

Marco Cannizzaro *Politecnico di Torino, Italy*, "Efficient Twoo-Phase Delay-Insensitive Codes for Global Communication and Asynchronous Hardware Support" (2/1/10 defense); co-advisors: Profs. Luciano Lavagno (Politecnico di Torino) and Steven M. Nowick (Columbia University).

Michael N. Horak *ECE Department, University of Maryland, College Park*, " A High-Throughput, Low-Power Asynchronous Mesh-of-Trees Interconnection Network for the Explicit Multi-Threading (XMT) Parallel Architecture" (7/16/08 defense); co-advisors: Profs. Uzi Vishkin (U. of Maryland) and Steven M. Nowick (Columbia University).

PHD THESIS PROPOSAL COMMITTEES

Hung-Yi Li (CS), "Computer-Aided Design-Space Exploration for System-on-Chip Design" (2/12/15); advisor: Prof. Luca Carloni.

Weiwei Jiang (CS), "High-Performance and Reliable Networks-on-Chip Using Asynchronous and Synchronous Approaches" (2/11/15); advisor: Prof. Steven Nowick.

John Demme (CS), "Overcoming the Intuition Wall: Automated Characterization in Computer Architecture" (5/17/13); advisor: Prof. Simha Sethumadhavan.

Young Jin Yoon (CS), "A Fully Integrated Network-on-Chip Design Framework for Future Heterogeneous Systems-on-Chip" (12/10/12); advisor: Prof. Luca Carloni.

Christos Vezyrtzis (EE), "Continuous-Time and Companding DSP's" (11/19/09); co-advisors: Profs. Steven Nowick and Yannis Tsividis (EE).

Melinda Y. Agyekum (CS), "Designing Delay-Insensitive Codes for Reliable and Timing-Robust Global Communication" (12/23/08); advisor: Prof. Steven Nowick.

Peggy B. McGee (CS), "On the Timing Behavior of Concurrent Digital Systems: Analysis, Tools and Applications" (2/27/08); advisor: Prof. Steven Nowick.

Cheng-Hong Li (CS), "Methods for Performance Optimization and Validation of Latency-Insensitive Systems" (11/25/07); advisor: Prof. Luca Carloni.

Cheoljoo Jeong (CS), "Optimization Techniques for Robust Asynchronous Threshold Networks (5/26/06); advisor: Prof. Steven Nowick.

Cristian Soviani (CS), "EDA for High-Performance Pipelines on FPGA's" (4/20/06); advisor: Prof. Stephen Edwards.

Tiberiu Chelcea (CS), "Design and Optimization Techniques for Large-Scale Asynchronous and Mixed-Timing Systems" (5/20/02); advisor: Prof. Steven Nowick.

Montek Singh (CS), "Optimization of Self-Timed Pipelines and Large-Scale Systems" (4/6/99); advisor: Prof. Steven Nowick.

Michael Theobald (CS), "Efficient Algorithms for the Design of Asynchronous Control Circuits" (9/23/98); advisor: Prof. Steven Nowick.

Fu-Chiung (John) Cheng (CS), "Synthesizing Iterative Functions into High Performance Delay-Insensitive Tree Circuits" (5/16/97); advisor: Prof. Stephen Unger.

Luis Plana (CS), "Contributions to the Design of Asynchronous Macromodular Systems" (2/20/97); advisor: Prof. Stephen Unger.

Hui Lei (CS), "Uncovering and Exploiting the Intrinsic Correlations between File References" (10/1/96); advisor: Prof. Dan Duchamp.

Robert Fuhrer (CS), "Sequential Optimization of Asynchronous Controllers: Algorithms, Tools and Applications" (5/2/95); advisor: Prof. Steven Nowick.

Danilo Florissi (CS), "Isochronets: A High-Speed Network Switching Architecture" (5/3/93); advisor: Prof. Yechiam Yemini.

DOCTORAL QUALIFYING EXAMINATIONS

Ben Nathanson (EE), "The Design of Self-Timed Pipelines" (12/14/93); advisor: Prof. Steven Nowick.

UNDERGRADUATE RESEARCH PROJECTS

David Hughes (January-May 2011) and **William Liu** (January-May 2011). Both David and William worked with me on the problem of designing and optimizing error-correcting codes for asynchronous delay-insensitive (DI) communication. Their starting point is a set of code families by my former PhD student, Melinda Agyekum. The two project students learned background on asynchronous design and DI codes. They have then worked to optimize and extend these codes for better error coverage and coding density. Such DI codes are important for complex digital systems, since they are resilient to timing deviations during transmission. This project will continue in Fall 2011.

Matthew Carlberg (January 2006-March 2007) and **Steven Callender** (July-October 2007). Both Matt and Steven worked intensively with me on designing and optimizing asynchronous digital pipeline components for a high-throughput low-power asynchronous interconnection network for shared memory parallel processors. *The results of Matthew's work were included in a co-authored paper at IEEE NOCS-10 Symposium, and as part of a US patent application filed in 2009.* Both Matt and Steven are now PhD students in the EECS Department at UC Berkeley.

Bill McLaughlin (EE) (January-May 2006) Collaborated on a research project on designing digital conversion circuits for asynchronous channel communication, to convert from two-phase channel protocols (using a level-encoded dual-rail [LEDR] encoding) to four-phase computation node protocols (using a dual-rail return-to-zero encoding). *The results were published in a co-authored paper at IEEE Async-07 Symposium, and in a journal article in IEEE Transactions on VLSI Systems (2009).*

Charles O'Donnell (May 2002-May 2003) Collaborated on a research project on the existence criteria for hazard-free multi-level logic implementations. *The results were published in a co-authored paper at IEEE Async-03 Symposium*. Charles also won the *Theodore Bashkow Award* from the Columbia University CS Department for best undergraduate research project (May 2003). Charles is now a PhD student in the MIT EECS PhD program.

Alexander Shapiro (January 1999-May 2000) (Supported partially by an NSF REU award.) Alexander received the *Theodore Bashkow award* in May 2000, for the computer science department senior who has excelled in independent projects.

Paul Goldstein (Spring 1996)

Andre Avzaradel (Spring 1996)

Tao Wu (Summer 1994). (Supported by NSF REU award; research resulted in published conference paper, 1996 Design Automation Conference.)

HIGH SCHOOL RESEARCH PROJECTS

Aiden Sheridan (December 2012 - present) Guiding a top Ossining High School (NY) sophomore on a 2 year research internship and project, working on asyn-

chronous and GALS networks-on-chip and robust delay-insensitive data encoding, for submission to the Intel Science Talent search competition in Fall-2014. Aiden won the **"Intel Excellence in Computer Science Award"** for his research poster on this research at the *14th Annual Westchester Science and Engineering Fair (WESEF)* in March 2014. He also won **1st Place in the Poster Competition** of the *2015 Westchester/Rockland Junior Science and Humanities Symposium (mathematics/physical science category)* in February 2015.

Shivam Pappu (Fall 2009) Collaborated on a research project with this high school senior, on the design of a high-speed asynchronous parallel prefix adder (Brent-Kung style), for submission to the Intel Science Talent search competition.

Bryan Bonnet (Summer 2009) Collaborated on a research project to model and simulate a new asynchronous digital conversion circuit (two-phase LEDR encoding to four-phase dual-rail encoding).

DEPARTMENTAL COMMITTEES

Academic Committee (1995 - 2002).

Course Scheduling (with Prof. Jonathan Gross; 1995 - 2000).

Faculty Recruiting Committee (Fall 1997 - 2004, 2005-06). I was host for many computer engineering candidates during this period, and took a lead on processing applications, and proposing invitations. Two of my hosted candidates were hired: Stephen Edwards (2001), Luca Carloni (2004).

IBM/Columbia Liaison Committee (Spring 2005-). I joined this committee, to develop and formalize increased contacts and interaction between Columbia and IBM.

PhD Committee (Fall 1993 - 1998).

PhD Admissions Sub-Committee (Fall 1993 - Spring 1997).

Chair, Strategic Planning Committee (CS Department) (Spring 2001-Spring 2002, Fall 2005-2006). *From 2005-2006,* as chair, I *organized and hosted a visit* to the CS department by **Bill Campbell, chair of Columbia Board of Trustees** (12/1/05). I organized the schedule for the visit day, as well as arranged for the set of faculty talks, and led the rehearsal of the faculty. *From 2001-2002,* I was chair of the new committee, setting future directions for the department, and drafting a Strategic Plan and Vision Statement, which was submitted to Dean Galil.

Visibility Committee (Fall 2004 - Spring 2005).

EXTERNAL SITE VISIT

Presenter: Gave talk for Computer Engineering area, invited external panelist (January 2003).

NSF DEPARTMENT INFRASTRUCTURE PROPOSAL

Contributor: Fall 2001 Proposal and revision round.

Area Captain: for written section of NSF department infrastructure proposal: *Scalable Multimedia Information Processing*, NSF CDA96 25374. Area: Scalable Systems for Mobile and Portable Computing. Total Award: $1,933,492 (9/1/96 - 8/31/01).

OTHER DEPARTMENTAL, FSEAS, and UNIVERSITY-WIDE ACTIVITIES

Columbia University Senate (2008-2010. I served as a Senator for a two-year term, and also was a member of the *Faculty Affairs Subcommittee*.

Women in Computer Science (WICS). Panelist and presenter to WICS group on how to pursue research (4/15/05).

CS Curriculum Changes. I proposed 2 new courses, *CSEE 3827 Fundamentals of Computer Systems,* and *CSEE 4823 Advanced Logic Design.* I prepared writeups on these new courses for the Academic Committee and the COI, and gave presentations at AC meetings and faculty meetings. Both courses have been approved (2003-2004).

Junior Faculty Recruiting. I have played the lead on junior recruiting in computer engineering, including the hosting of 3 candidates (Budiu, Carloni, Wang) in 2003-2004, and many more in past years (1993-2004 inclusive).

New Science Building: Computer Engineering Proposal. I was asked by Profs. Schulzrinne (CS) and Heinz (EE) to be in charge of a computer engineering proposal for the new science building. I wrote and revised the proposal, and submitted it to the Provost (2/28/04).

Computer Engineering BS and MS Program. I previously made the final revisions to the Computer Engineering MS proposal, and then helped push it through the University Senate in 02-03. The program was approved in January 2003, and participated in BS and MS advising in 2003-2004.

SEAS Ad Hoc Committee. Member of ad hoc committee for tenure case of SEAS faculty member (4/22/04, 1/24/06, 3/29/06, 1/19/10).

Engineering Council Visit. I participated in their CS department visits (4/14/05 and 4/15/04), as computer engineering representative.

Computer Engineering/EE Faculty-Student Dinner. Attended at the Faculty House (4/20/04, 4/26/06).

SEAS Senior Class Fund Committee: Gift Presentation. Participated as a faculty representative (10/15/03).

Presentation to Chief-of-Staff, U.S. House of Representatives Science Committee. I was asked by Ellen Smith, assistant VP of Public Affairs, to give a presentation on my recent research for Tim Clancy, the chief of staff of the US House Science Committee (2/23/01).

Invited Participant, Columbia Presidential Search Committee's meeting with SEAS faculty, 5/29/01.

SEAS Ad Hoc Committee Member. For tenure case of a EE faculty member (4/9/01).

Group Leader, CS Department Retreat. I was group leader of the strategic planning session of our department retreat (November 2000).

Joint Music/CS Position. CS Department liaison with Music Department, helped edit proposal submitted to Vice Provost Michael Crow (Spring 99).

NSF Infrastructure Program PI Meeting (August 8-9, 1999): senior department representative, Las Cruces, New Mexico; for department CISE infrastructure award.

Days on Campus luncheon (April 1999): for prospective undergraduate applicants.

Engineering Weeks: majors presentation (Spring 2000, 2001): for prospective undergraduate majors.

PhD TA/Instructor Scheduling (1994 - 95).

CS Departmental Colloquium (1993 - 94): organized the colloquium.

CS Self-Timed Seminar (1993 - present): co-ran the seminar.

Advisor, Computer Engineering: juniors/seniors (Fall 1993 - present).

Advisor, Columbia College: juniors (1993-94,1995-96), seniors (1994-95, Fall 96).

CS Qualifying Exams:

- wrote Computer Organization section (Fall 1993 - Fall 1996)
- wrote Digital Logic section (Fall 1995- 1996)

CS Comprehensive Exams: wrote Computer Architecture section (Fall 1997 - Spring 2004)