Steven Nowick awarded NSF grant to develop asynchronous on-chip interconnection networks

Steven Nowick

Meeting the country's future technological needs is one of the grand challenges of the next decade. It will require cost-effective and systematic approaches to building large-scale computing systems capable of massively parallel computation tasks. Such systems will involve hundreds or thousands of processors, or more, on a single computer chip housed in either large data centers or on desktop or hand-held consumer products.

Designing such systems will not be easy, and it currently entails severe cost overheads. The tremendous amounts of energy usage required means that thermal overheating is a problem as is poor delivered performance. The complexity in assembling large numbers of varied components onto a single chip is also a challenge. Exacerbating everything is the traditional use of a fixed-rate clock that centrally controls all components on a chip.

One promising alternative is to build *plug-and-play* computer systems that dispense entirely with a global clock and rely instead on asynchronous communications where individual components communicate with one another as needed. Structured digital on-chip interconnection networks, called *networks on chip* (NoC's), are already an organizing backbone of many recent commercial parallel computers and embedded systems, using synchronous approaches as well as recent forays into asynchronous approaches (IBM's TrueNorth neuromorphic chip, STMicroelectronics' STHORM embedded processor). While initial NoC solutions with asynchronous design have been promising and demonstrate an ease of assembly and scalability, they lack fundamental features needed to make them viable for industry.

To explore and significantly advance plug-and-play systems for industrial applications, the National Science Foundation established the grant "An Asynchronous Network-on-Chip Methodology for Cost-Effective and Fault-Tolerant Heterogeneous SoC (System-on-Chip) Architectures." This grant, for $420,000, will fund several several significant new research directions in the area of asynchronous on-chip networks and systems.

The grant's principal investigator is Steven Nowick, a computer scientist whose research in computer systems has included asynchronous networks on chip. "This grant will allow me to further research an area I've long been excited about. It will fund two graduate students, allowing us to make progress in asynchronous networks-on-chip by developing better ways to implement error detection and correction, multicast/broadcast capability, performance enhancement, and automated design flow," says Nowick. "Taken together, this new approach promises a significant advance forward in providing the capability to assemble cost-effective parallel computer systems."

Steven Nowick is a professor of Computer Science and Electrical Engineering (and by courtesy, Electrical Engineering) at Columbia University, and the co-founder and former chair of the Computer Engineering Program.
Nowick received his PhD in Computer Science from Stanford University in 1993, and his BA from Yale University.

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