Nalini Vasudevan

EDUCATION

- PhD (with Distinction), Computer Science, **Columbia University**. (2007 - 2011)
  Advisor: Prof. Stephen Edwards. GPA: 4.05 (on a scale of 4)

- MPhil, Computer Science, **Columbia University**. (2007 - 2010)
  GPA: 4.05 (on a scale of 4)

- Master of Science, Computer Science, **Columbia University**. (2006 - 2008)
  GPA: 4.05 (on a scale of 4)

- Bachelor of Engineering, Computer Science, **RV College of Engineering** , Visveswariah Technological University (VTU), India. (2001 - 2005)
  First Class with Distinction, Eight Semesters aggregate - 85 %. GPA: 4 (on a scale of 4)

WORK
EXPERIENCE

- Software Engineer, **Google**, Mountain View (Mar 2014 - Present)
  Search Infrastructure Group
  Designing, building and optimizing systems for better search quality and performance.

- Research Scientist, **Intel Labs**, Santa Clara (Feb 2011 - Mar 2014)
  Programming Systems Lab
  Designed and implemented aggressive loop level optimizations for high performance computing applications. Added new assembly level instructions to Intel's ISA.

- Graduate Research Assistant, **Columbia University**, New York (Jan 2007 - Jan 2011)
  Languages and Compilers Group
  Designed and implemented parallel models for computation.

- Research Co-op, **IBM T.J.Watson Research Center**, New York (Jan 2010 - Aug 2010)
  Programming Technologies Group
  Designed algorithms for scheduling and synchronization in the X10 concurrent model.

- Research Intern, Alcatel-Lucent **Bell Laboratories**, New Jersey (Jun 2009 - Aug 2009)
  Computing and Software Principles Group
  Designed and verified lock-free data structures for concurrent hash tables.

- Research Co-op, **IBM T.J.Watson Research Center**, New York (Jun 2008 - Aug 2008)
  Programming Technologies Group
  Designed synchronization algorithms in the X10 concurrent programming model.

- Research Intern, **Microsoft Research**, United Kingdom (Jun 2007 - Aug 2007)
  Programming Principles and Tools Group
  Designed and implemented a deterministic concurrent library in Haskell

- Software Engineer, **Yahoo R&D Center**, Bangalore (July 2005 - Feb 2006)
  Yahoo Direct Ads Group
  Developed a heuristic based trigger management system that maps yahoo users' events to triggers

- Research Intern, **Indian Institute of Science**, Bangalore (Jan 2005 - May 2005)
  Communication and Networking Lab
  Implemented localization techniques for ad-hoc sensor networks

AWARDS AND
HONORS

- **Google Peer Bonus** 2016
  For resolving a widespread issue quickly.

- **Google Peer Bonus**   2016

  Debugging a bug that affected multiple products across Google.

- **Google Peer Bonus**   2016

  For being extremely quick in offering a solution to a complex issue.

- **Google Spot Bonus**   2016

  For performance that went beyond the highest expectations

- **Google Peer Bonus**   2016

  For being extremely quick in offering a solution to a complex issue

- **Google Spot Bonus**   2015

  For performance that went beyond the highest expectations

- **Intel High 5 Award**   2013

  For extraordinary dedication to innovation

- **Intel Divisional Recognition Award**   2013

  For 'above and beyond' accomplishment

- **Intel High 5 Award**   2011

  For extraordinary dedication to innovation

- **PhD with Distinction**   2011

- **Google Anita Borg Scholar**   2010

  One of 25 scholars in the US to receive the award.

- **3rd Place, ACM Student Research Competition**   2010

  Held at the Conference on Programming Architectures and Compilation Techniques (PACT'10).

- **Google Grace Hopper Sponsorship**   2010

  All-paid expenses to attend Grace Hopper Celebration 2010 in Atlanta.

- **NSF PACT Travel Grant**   2010

  To present at PACT'10.

- **HiPC Scholarship**   2010

  One of the top few posters from US-based students at HiPC '10.

- **ACM SRC Award**   2010

  To take part in the student research competition at PACT'10.

- **HotPar Student Grant**   2010

  To present at HotPar'10 Workshop.

- **ACM SIGPLAN Travel Award**   2010

  To attend the PLDI'10 conference at Toronto, Canada.

- **TCPP Travel Award**   2010

  To present at the IPDPS PhD Forum in Atlanta.

- **Yahoo!/Columbia Gracehopper Scholarship**   2009

  All expenses paid scholarship to attend the Grace Hopper Celebration'09 at Tucson.

- **ACM SIGPLAN PAC Award**   2009

  ACM travel award to attend the PLDI'09 Conference at Dublin, Ireland.

- **Google PLDI'2009 Grant**   2009

  One of 3 students to receive the Google grant to attend PLDI'09 at Dublin, Ireland.

- **CRA-W Travel Grant**   2009

  Financial aid to attend the CRA-W Grad Cohort Program at San Mateo.

- **CRA/CDC Travel Scholarship**   2009
  Selected to attend the PLOSA'09 Workshop at Washington D.C.

- **IBM Thanks! Award**   2008
  Awarded during my internship at IBM Research in 2008.

- **TCPP Travel Award**   2008
  To present at the IPDPS Conference at Miami.

- **Artist2 Network of Excellence Grant**   2008
  Sponsored trip to the Artist2 Summer School in Grenoble, France.

- **Onassis Foundation Financial Aid**   2008
  Travel aid to attend the 2008 Lectures in Computer Science, Greece.

- **NSF-Grace Hopper Scholarship**   2007
  Selected to attend the Grace Hopper Conference at Orlando.

- **CRA-W Travel Support**   2007
  Financial aid to attend the CRA-W Grad Cohort Program at San Francisco.

- **Best Undergraduate Thesis of the year**   2005
  Titled 'Localization of Ad-Hoc Sensor Networks', RV College of Engineering (VTU).

- **Merit Seat**   2001 - 2005
  80% tuition waiver during all four years of undergraduate education. Given to top 10%.

- **Best Project Award**   2004
  Project On 'Speech Recognition using ANNs' presented at IOTA 2004, CS Tech Fest, Bangalore, India.

- **Qualified in Graduate Aptitude Test in Engineering** (GATE)   2004
  Obtained a percentile of 99.13. GATE is conducted by the seven IITs and IISc in India.

- **Runner-Up at Date with .Net**   2004
  A Spot Programming Contest organized by .NET Users Group, Bangalore, India.

- **Third place in Spot Programming Contest at IOTA-2004**   2004
  Inter-Collegiate Computer Science Fest, Bangalore, India.

- **First place at Impulse'04**   2004
  Inter-collegiate System Modeling Event, Bangalore, India

- **51st rank in the Common Engineering Entrance Test (CET)**   2001
  out of 100,000 candidates, Karnataka, India.

- **Commended by the Assoc. of Mathematics Teachers of India**   1998
  in association with the National Board of Higher Mathematics, India.

- **Most determined student of the year** award   1998
  Cluny Convent High School, Bangalore, India.

TEACHING

- **Faculty Member**, Columbia Video Network   2009 - 2010
  Taught the COMS 3101-V03 C Programming Language course offered to off-campus students

- **Program Coordinator/Instructor, Emerging Scholars Program**, Columbia University 2009 - 2010
  Organized weekly workshops to encourage freshmen to major in Computer Science

- **Instructor**, Columbia University   2009
  Taught the COMS 3101-3 C Programming Language course
  Designed my own class structure and slides, prepared assignments and graded them

- **Teaching Assistant**, Computer Science, Columbia University

– CSEE W4840 course on Embedded System Design	2009
– COMS W4115 course on Programming Languages and Translators	2008
– COMS 3157 course on Advanced Programming	2008
– COMS 1003 course on Introduction to Computer Programming in C	2006

- **Program Committee Member**

– Workshop on Interaction and Concurrency Experience (ICE 2011)	2011

- **Session Chair**

– IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2011)	2011

- **Reviewer** for the following books/journals/conferences,

◇ Conference on Parallel Architectures and Compilation Techniques (PACT 2012)	2012
◇ IEEE Conference on Parallel and Distributed Systems (ICPADS 2011)	2011
◇ Symposium on Principles and Practice of Parallel Programming (PPOPP)	2010
◇ Fundamenta Informaticae Journal	2010
◇ Springer Book on Correct-by-Construction Embedded Software Synthesis	2009
◇ ACM Conference on Languages, Compilers and Tools for Embedded Systems (LCTES)	2009
◇ ACM/IEEE Conference on Hardware/Software Codesign (CODES+ISSS)	2008

- **Memberships: IEEE, ACM, SIGPLAN, USENIX** — 2008-2011

- **Panelist, Grace Hopper Celebration 2010** — 2010
  A panel on *Beyond your technical skills: What makes a successful researcher?*

- **PhD Committee Member**, Department of Computer Science, Columbia University — 2008-2010
  The PhD committee revises policies of the CS PhD program

- **Mentor, Women in Computer Science (WICS)**, Columbia University — 2008-2010
  Provided assistance to female students in courses, research work and job search

- **Speaker, LINUXASIA 2006**, open source conference in Asia — 2006
  Demonstrated Gambas, an open source environment like Visual Basic.

- **Speaker, FOSS.IN 2005**, India's largest free and open source conference — 2005
  A hands-on session about extensions in Firefox

- **Organizer of IOTA 2003**, Technical Fest, India. — 2003
  Conducted events such as spot programming and debugging

1. Automatic Loop Vectorization Using Hardware Transactional Memory — 2014
   Sara S. Baghsorkhi, Albert Hartono, Youfeng Wu, Nalini Vasudevan, Cheng Wang

2. Instruction and Logic for Cache-Based Speculative Vectorization — 2013
   Nalini Vasudevan, Youfeng Wu, Cheng Wang, Sara Baghsorkhi, Albert Hartono

3. Methods and Systems to Vectorize Scalar Loops Having Loop-carried Dependences — 2013
   Jayashankar Bharadwaj, Nalini Vasudevan, Albert Hartono, Sara S. Baghsorkhi

4. Loop Vectorization Methods And Apparatus — 2012
   Nalini Vasudevan, Jayashankar Bharadwaj, Christopher Hughes, Milind Girkar, Mark Charney, Robert Valentine, Victor Lee, Daehyun Kim, Albert Hartono, Sara Baghsorkhi

5. Apparatus and Method For Selecting Elements of a Vector Computation   2012

Victor W. Lee, Jayashankar Bharadwaj, Daehyun Kim, Nalini Vasudevan, Tin-Fook Ngai, Albert Hartono, Sara Baghsorkhi

6. Instruction To Reduce Elements In a Vector Register With Strided Access Pattern.   2012

Albert Hartono, Jayashankar Bharadwaj, Nalini Vasudevan, Sara S. Baghsorkhi, Victor W. Lee, Daehyun Kim

7. Speculative Non-faulting Loads and Gathers   2012

Jayashankar Bharadwaj, Nalini Vasudevan, Victor W. Lee, Sara S. Baghsorkhi, Albert Hartono, Daehyun Kim

8. Apparatus for Propagating Conditionally Evaluated Values in SIMD/Vector Execution   2012

Jayashankar Bharadwaj, Nalini Vasudevan, Victor W. Lee, Daehyun Kim, Albert Hartono, Sara S. Baghsorkhi

9. Apparatus And Method For Detecting Identical Elements Within A Vector Register   2011

Victor W. Lee, Daehyun Kim, Tin-Fook Ngai, Jayashankar Bharadwaj, Albert Hartono, Sara S. Baghsorkhi, Nalini Vasudevan

10. Systems, Apparatuses and Methods For Setting an Output Mask in a Destination Writemask register from a source write mask register using an input writemask and immediate   2012

Victor W. Lee, Daehyun Kim, Tin-Fook Ngai, Jayashankar Bharadwaj, Albert Hartono, Sara Baghsorkhi, Nalini Vasudevan

11. Apparatus and method for vectorization with Speculation support   2011

Jayashankar Bharadwaj, Victor W. Lee, Kim Daehyun, Nalini Vasudevan, Tin-Fook Ngai, Albert Hartono, Sara S. Baghsorkhi

12. Apparatus And Method For Selecting Elements Of a Vector Computation   2011

Jayashankar Bharadwaj, Nalini Vasudevan, Victor W. Lee, Daehyun Kim, Albert Hartono, Sara S. Baghsorkhi

13. Fast Biased Locks   2010

Kedar Namjoshi, Nalini Vasudevan

PUBLICATIONS   **Book Chapters**

1. Compiling SHIM   2010

Stephen A. Edwards, Nalini Vasudevan

Synthesis of Embedded software - Frameworks and Methodologies for Correctness by Construction Software Design, Springer, 1st edition, 2010.

Journal Papers

2. Buffer Sharing in Rendezvous Programs   2010

Nalini Vasudevan, Stephen A. Edwards

IEEE Transactions on Computer Aided Design (TCAD 2010).

Conference Papers

3. Simple and Fast Biased Locks   2010

Nalini Vasudevan, Kedar Namjoshi, Stephen A. Edwards

Conference on Parallel Architectures and Compilation Techniques (PACT 2010), Vienna, Austria.

4. Compositional Deadlock Detection for Rendezvous Communication   2009

Baolin Shao, Nalini Vasudevan, Stephen A. Edwards

International Conference on Embedded Systems (EMSOFT 2009), Grenoble, France. Acceptance Rate

= 33/106 = 31%.

5. A Determinizing Compiler   2009
   Nalini Vasudevan, Stephen A. Edwards
   ACM SIGPLAN Conference on Programming Languages Design and Implementation (PLDI 2009) -
   Fun Ideas and Thoughts (FIT), Dublin, Ireland.

6. Buffer Sharing in CSP-like programs   2009
   Nalini Vasudevan, Stephen A. Edwards
   7th ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE
   2009), Cambridge, USA.

7. Compile-Time Analysis and Specialization of Clocks in Concurrent Programs   2009
   Nalini Vasudevan, Olivier Tardieu, Julian Dolby, Stephen A. Edwards
   International Conference on Compiler Construction (CC 2009), Lecture Notes in Computer Science,
   York, UK. Acceptance Rate: 141/532 = 26%.

8. Celling SHIM: Compiling Deterministic Concurrency to a Heterogeneous Multicore   2009
   Nalini Vasudevan, Stephen A. Edwards
   24th Annual ACM Symposium on Applied Computing (SAC 2009), Honolulu, Hawaii, USA. Accep-
   tance Rate: 316/1084 = 29%.

9. Static Deadlock Detection for the SHIM Concurrent Language   2008
   Nalini Vasudevan, Stephen A. Edwards
   6th ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE
   2008), Anaheim, USA.

10. A Deterministic Multi-Way Rendezvous Library for Haskell   2008
    Nalini Vasudevan, Satnam Singh, Stephen A. Edwards
    22nd IEEE International Parallel and Distributed Symposium (IPDPS 2008), Miami, Florida, USA.
    Acceptance Rate: 105/410 = 25.

11. Programming Shared Memory Multiprocessors with Deterministic Message-Passing Concurrency:
    Compiling SHIM to Pthreads   2008
    Stephen A. Edwards, Nalini Vasudevan, Olivier Tardieu
    Design Automation and Test in Europe (DATE 2008). Acceptance Rate: 198/839 = 23%.

12. Comparative Analysis of Neural Network Techniques Vs Statistical Methods in Capacity
    Planning   2007
    Nalini Vasudevan, Gowri C. Parthasarathy
    5th IEEE ACIS International Conference on Software Engineering Research, Management & Applica-
    tions (SERA 2007).

Workshop Papers

13. Determinate Deadlock-free X10 and its compilation   2010
    Nalini Vasudevan, Vijay Saraswat, Olivier Tardieu, Julian Dolby
    Workshop on Partitioned Global Address Space (PGAS 2010), New York, USA.

14. Deterministic Deadlock-free Concurrency   2010
    Nalini Vasudevan
    High Performance Computing - Student Research Symposium (HiPC 2010), Bangalore, India.

15. Determinism Should Ensure Deadlock Freedom   2010
    Nalini Vasudevan, Stephen A. Edwards
    2nd USENIX Workshop on Hot Topics in Parallelism (HotPar 2010), Berkeley, California.

16. Ensuring Deterministic Concurrency through Compilation 2010
    Nalini Vasudevan, Stephen A. Edwards
    24th IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPS 2010), Atlanta, April 2010.

17. Iterative Image Based Video Summarization by Node Segmentation 2006
    Nalini Vasudevan, Arjun Jain, Himanshu Agrawal
    Information Technology and Sustainable Development, Saudi Computer Society (SCS), Riyadh, Saudi Arabia, March 2006.

18. Linux Cluster Possibilities in 3-D Photo Quality Imaging and Animation 2005
    Arjun Jain, Himanshu Agrawal, Nalini Vasudevan
    World Academy of Science, Engineering and Technology (WASET), November 2005.

19. A Connectionist Framework For Feature Based Speech Recognition Using Artificial Neural Networks 2004
    Nalini Vasudevan, Anushruthi Rai, Arjun Jain
    18th CSI Student Convention, Computer Society of India, Bangalore, India, Nov 2004.

Technical Reports

20. Efficient, Deterministic, and Deadlock-free Concurrency 2011
    PhD Thesis, Technical Report CUCS.013.11, Columbia University, March 2011.

21. Static Deadlock Detection in SHIM with an Automata Type Checking System 2008
    Dave Aaron Smith, Nalini Vasudevan, Stephen A. Edwards
    Technical Report CUCS.053.08, Columbia University, Department of Computer Science, New York, USA, December 2008.

22. Analysis of Clocks in X10 Programs (Extended) 2008
    Nalini Vasudevan, Olivier Tardieu, Julian Dolby, Stephen A. Edwards
    Technical Report CUCS.052.08, Columbia University, Department of Computer Science, New York, USA, December 2008.

23. A JPEG Decoder in SHIM 2006
    Nalini Vasudevan, Stephen A. Edwards
    Technical Report CUCS.48.06, Columbia University, Department of Computer Science, New York, USA, December 2006.

TALKS   **Invited Talks**

1. Efficient, Deterministic and Deadlock-free Concurrency
    Intel Labs, Santa Clara, Aug 2010. 2010

2. Static Deadlock Detection in Concurrent Programming Languages
    At IBM Research, Watson Research Center, New York, May 2008. 2008

3. Gambas: Gambas Almost Means BASic:
    - At LINUX ASIA/2006, Open Source conference and exposition in Asia. 2006
    - At RV College of Engineering, India. 2005
    - At FOSS.IN/2004, India's largest Free and Open Source symposium. 2004

4. Add More to Firefox
    At FOSS.IN/2005, India's largest Free and Open Source symposium. 2006

Conference Presentations

5. Simple and Fast Biased Locks   2010
   International Conference on Programming Architectures and Compilation Techniques (PACT 2010),
   Vienna, Austria.

6. Buffer Sharing in CSP-like programs   2009
   7th ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE
   2009), Cambridge, USA.

7. A Determinizing Compiler   2009
   ACM SIGPLAN Conference on Programming Languages Design and Implementation (PLDI 2009) -
   Fun Ideas and Thoughts (FIT), Dublin, Ireland.

8. Compile-Time Analysis and Specialization of Clocks in Concurrent Programs   2009
   International Conference on Compiler Construction (CC 2009), York, UK.

9. Static Deadlock Detection for the SHIM Concurrent Language   2008
   6th ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE
   2008), Anaheim, USA.

10. A Deterministic Multi-Way Rendezvous Library for Haskell   2008
    22nd IEEE International Parallel and Distributed Symposium (IPDPS 2008), Miami, Florida, USA.

POSTERS

- D^2C: Deterministic, Deadlock-free Concurrency
  Internal Conference on Parallel Architectures and Compiler Techniques (PACT 2010), Vienna, Austria.
  2010

- Ensuring Deterministic Concurrency through Compilation
  IEEE International Parallel & Distributed Processing Symposium (IPDPS), Atlanta.   2010

- Preventing Races and Deadlocks in Concurrent Programs: The SHIM Approach

   – Programming Languages, Operating Systems and Architecture Workshop   2009
   – CRA-W Grad Cohort, San Mateo   2009