## **CSEE W3827**

## Fundamentals of Computer Systems

## Homework Assignment 3

Prof. Martha A. Kim Columbia University Due Feb 26, 2016 by 5:00 PM

- Write your name and UNI on each page of your solutions.
- Note your collaborators.
- For each machine use as few states as you can.
- Show your work (i.e., state transition diagram, logic expressions, and a schematic using any gates).
- Turn in to the CSEE 3827 dropbox in the TA room.
- 1. (20 pts.) Give a schematic for a Moore counter that counts in the following sequence: 0, 1, 3, 6, 10, 15, 0, 1, 3 etc. Call the outputs *c*<sub>3:0</sub>.
- 2. (20 pts.) Give a schematic for a Moore recognizer that recognizes an input sequence that has three or more consecutive 1s or three or more consecutive 0s. The recognizer has a single input, *x*, and a single output, *y*, that it sets and holds at 1 once either streak has been seen. The output is reset to 0 only on machine reset. Give a schematic for your design.
- 3. (20 pts.) Design a machine that implements a Mealy serial 2's complement negator. The machine takes in serial 4-bit values  $x_0$ ,  $x_1$ ,  $x_2$ ,  $x_3$  and produces serial four bit outputs  $y_0$ ,  $y_1$ ,  $y_2$ ,  $y_3$  such that  $y_{3:0} = -x_{3:0}$ . Assume that a new four bit value begins every four cycles after reset, and there is no need to detect overflow. Call the input bit *x* and the output bit *y* and provide a complete design (i.e., state encoding and expressions for combinational logic). No need to draw the schematic.
- 4. (20 pts.) Give a state transition diagram for a Mealy machine with a single input, *a*, and a single output, *b*. The input bitstream is a series of serial twobit values. For example the values *x*, *y*, and *z* would appear to the machine as a  $a = x_1, x_0, y_1, y_0, z_1, z_0$ . After each two-bit value, the machine should indicate when the most recent value was larger than the previous value by setting b = 1. For the first value arriving after reset, when there was no previous value, the machine should set b = 0.

5. (20 pts.) Reverse engineer the state transition diagram for the FSM below.



Note that this machine uses T flip flops, or "toggle" flip flops, whose behavior is as follows.

$$\begin{array}{ccc}
T & Q^+ \\
\hline
0 & Q \\
1 & \overline{Q}
\end{array}$$