

CSEE W3827
 Fundamentals of Computer Systems
 Homework Assignment 2

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UPDATE: Due Feb 11, 2016 by 5:00 PM.
Turn in to the CSEE 3827 dropbox in the TA room.
Do not turn in at lecture or via Piazza.

*Write your name **and UNI** on each page of your solutions.
 Show your work for each problem, and the final schematic.
 Use as few AND2, OR2, and INV gates as possible. No other gates are allowed. Indicate the gate count for each design.
 Problem #3 is the only exception to the above rule.
 Note your collaborators.*

1. (20 pts.) Implement a 2-bit comparator whose single output *less* is true if and only if $X(x_1, x_0) < Y(y_1, y_0)$.
2. (20 pts.) Redesign the comparator from the previous problem using the additional assumption that neither x_1 and y_1 nor x_0 and y_0 will be 1 at the same time.
3. (20 pts.) Design a shifter that takes an 8-bit input ($in_{7:0}$) and an operation code ($c_{1:0}$) and produces an 8-bit output ($out_{7:0}$). The shifter should perform the following three operations:
 - *no shift* ($c = 00$): do nothing
 - *shift right logical* ($c = 01$): shift the input one position to the right, filling with a zero
 - *shift right arithmetic* ($c = 10$): shift the input one position to the right, filling with the sign bit
 - *shift left logical* ($c = 11$): shift the input one position to the left, filling with a zero
4. (20 pts.) Implement a **TALLY** module that takes three bits of input ($x_{2:0}$) and produces two bits of output ($y_{1:0}$). The two bit output value should indicate the number of input bits that are true.
5. (20 pts.) Complete the missing (dotted) part of the circuit below. The whole thing should implement the majority function, producing a true value when more than half of the seven input bits are true.

