CSEE 3827: HOMEWORK 3   DUE: 3/7/11

Complete the following problems. Be sure to show your work for partial credit.

1. A JK flip-flop is a flip-flop with the following *characteristic* table:

J	K	Q_{next}	comment
0	0	Q	hold state
0	1	0	reset
1	0	1	set
1	1	$\overline{Q}$	toggle

A Mux-Not flip-flop (MN flip-flop) behaves as follows: if M=1, the flip-flop complements the current state. If M=0, the next state of the flip-flop is equal to the value of N.

   (a) Derive the characteristic table for the MN flip-flop.
   (b) Show how a JK flip-flop can be converted into an MN flip-flop by adding gates and inverters.

2. Derive the state diagram and characteristic table of the latch circuit below.
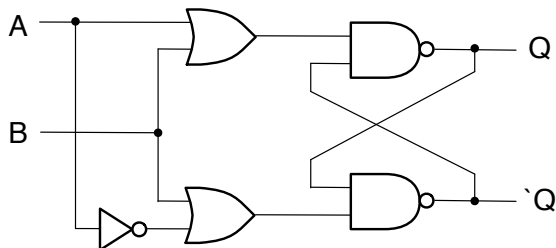
3. Construct two parity checkers, one Mealy machine, one Moore machine. Both machines should have the following interface.

   - Inputs
     - X: 1 bit input signal
     - CLK: 1 bit clock
     - RST: 1 bit active high reset
   - Outputs
     - P: 1 bit parity signal where P=0 when an odd number of 1s seen on X, and P=1 for an even number of 1s on X

4. In this problem you will design two machines to convert serial input into 4-bit parallel output. Both machines should be Moore machines and have the following interface:

   - Inputs
     - S: 1 bit serial input (e.g., if $S = S_0, S_1, S_2, S_3, S_4, S_5, S_6, S_7...$)
     - CLK: 1 bit clock
     - RST: 1 bit active high reset
   - Outputs
     - $P_{3:0}$: 4 bit parallel output data word (... then $P = S_{0:3}$, then $P = S_{4:7}$ and so on.)
     - V: 1 bit valid signal indicating when there is a 4 bit word available on P

   - First design and implement this converter using only D flip flops to hold the state.
   - Implement a second design using a shift register to store the serial input. You may need to store other state as well. This is fine and you may use whatever state elements you like.