CSEE 3827: Fundamentals of Computer Systems

Lecture 9

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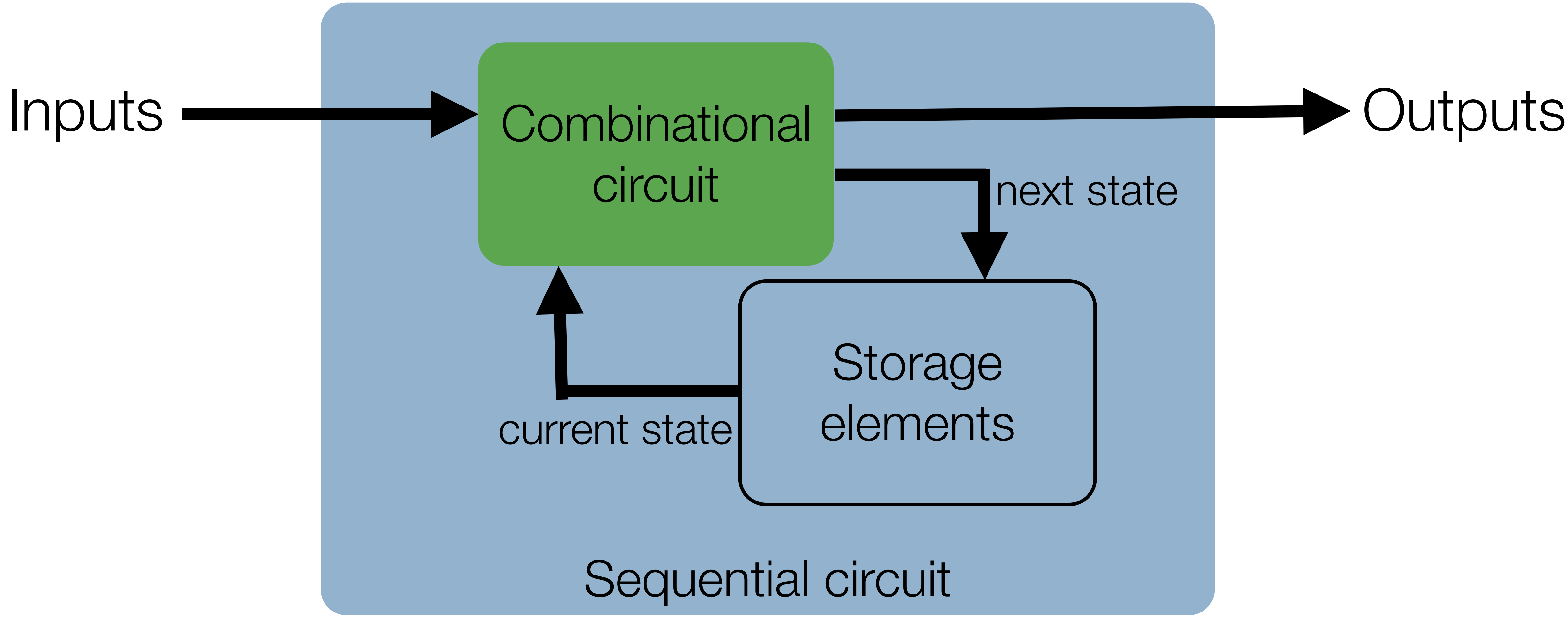
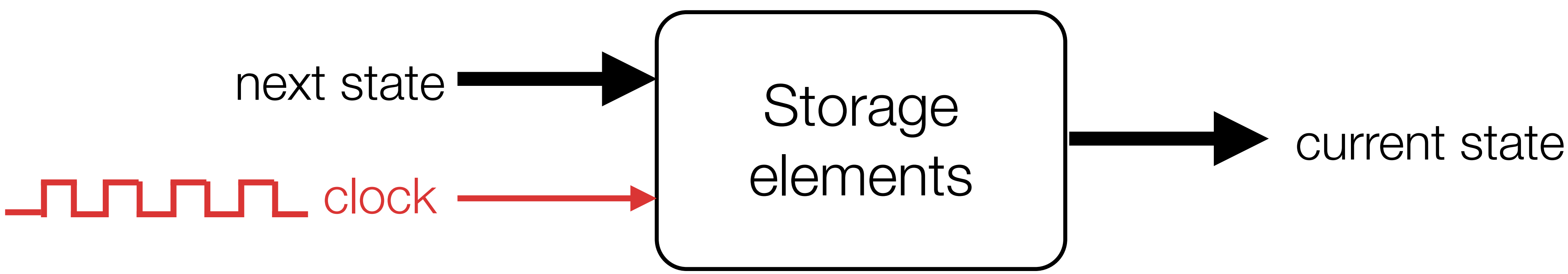
Combinational v. sequential logic



Asynchronous v. synchronous circuits

- **asynchronous sequential circuits**: behavior depends on input signals at *any instant of time*

- **synchronous sequential circuits**: behavior defined by signal values at *discrete times*

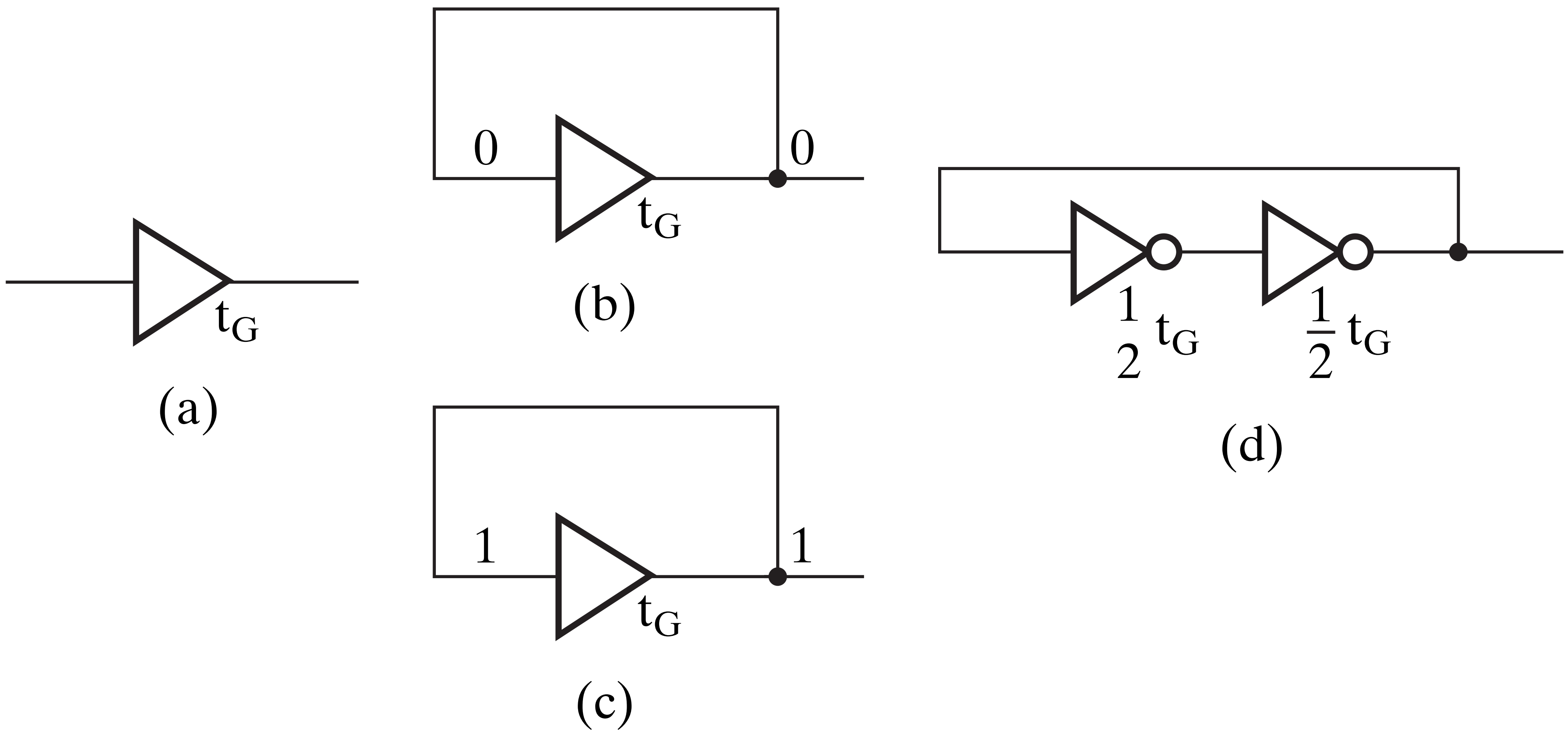


Latches (asynchronous storage elements)

Simple logic for information storage

5-2

Can build basic storage out of any gate that has delay (t_G)

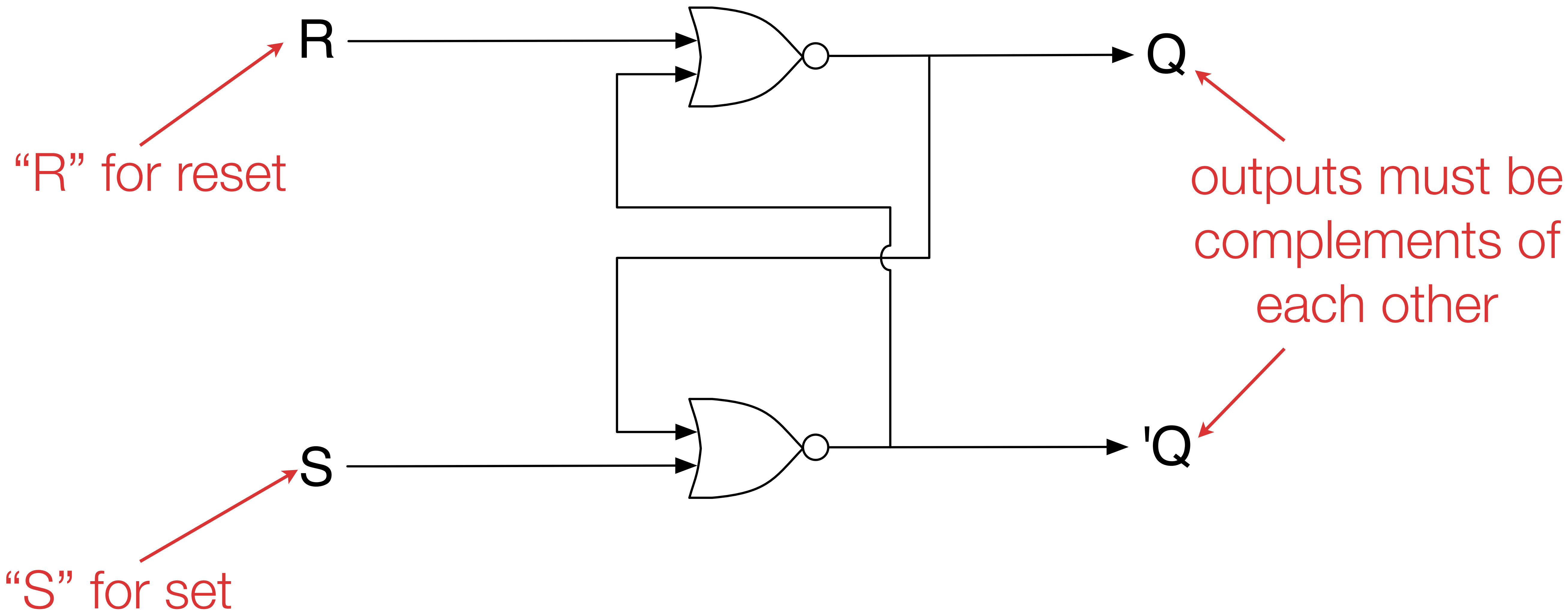


However, these storage circuits are not writable. . .

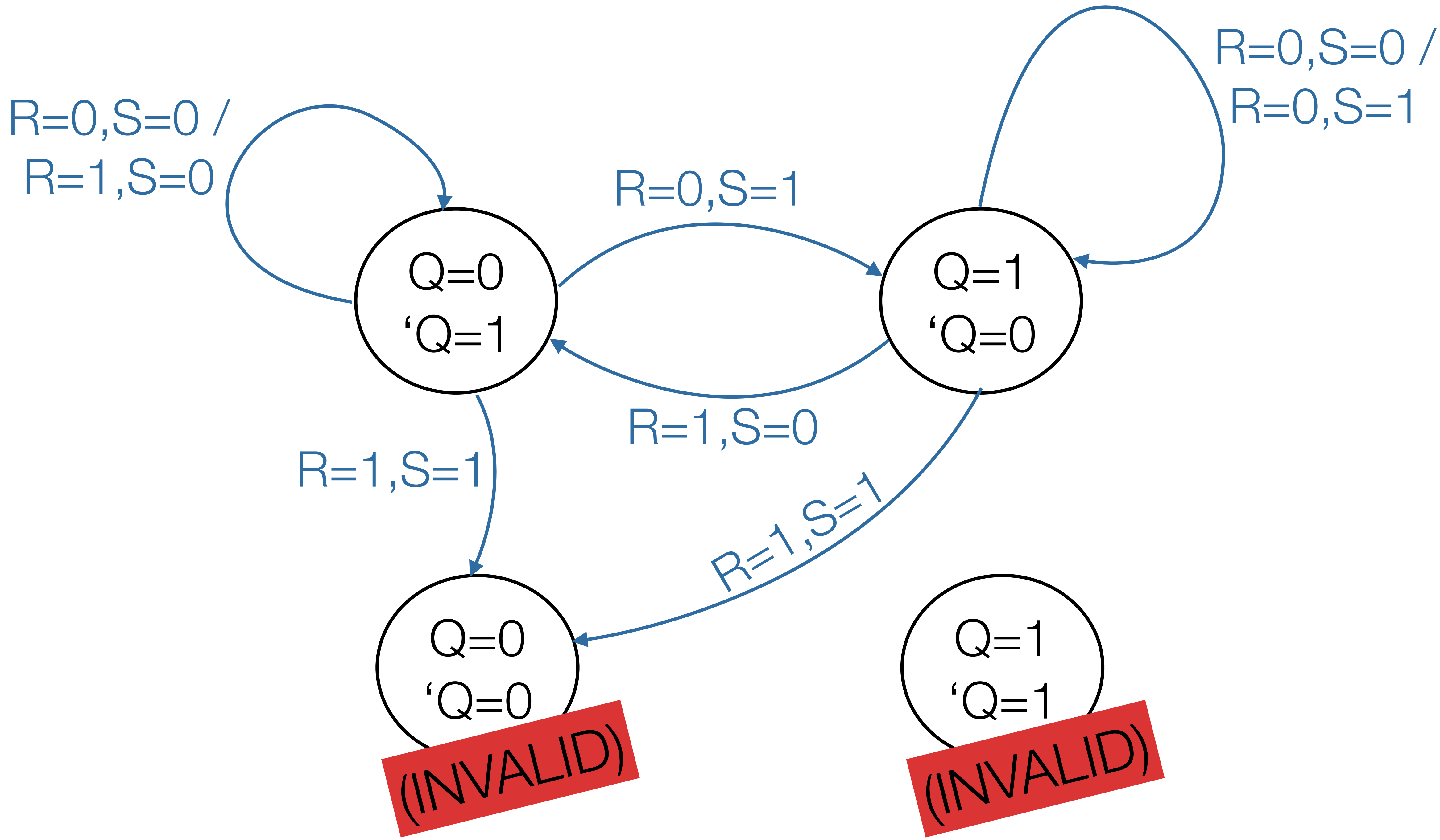
M. Morris Mano & Charles R. Kime
LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 4e

SR latch

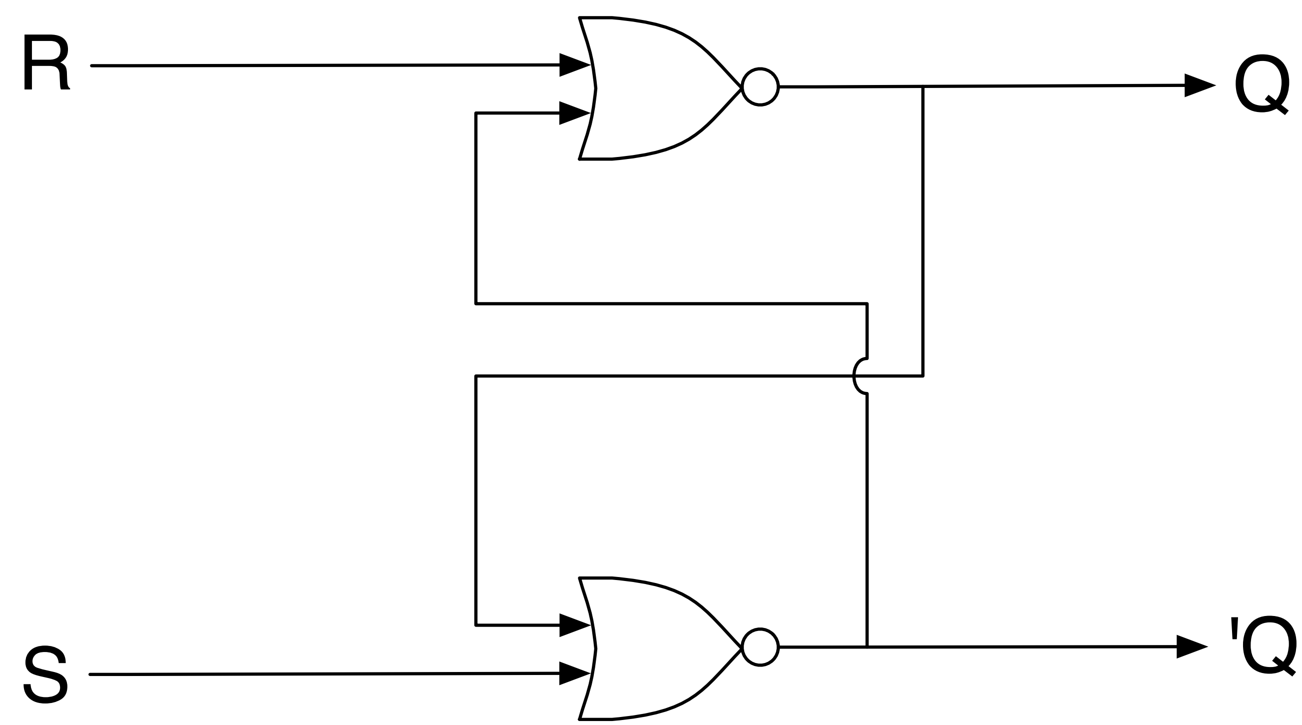
- Latch constructed of cross-coupled NOR gates



SR latch state diagram



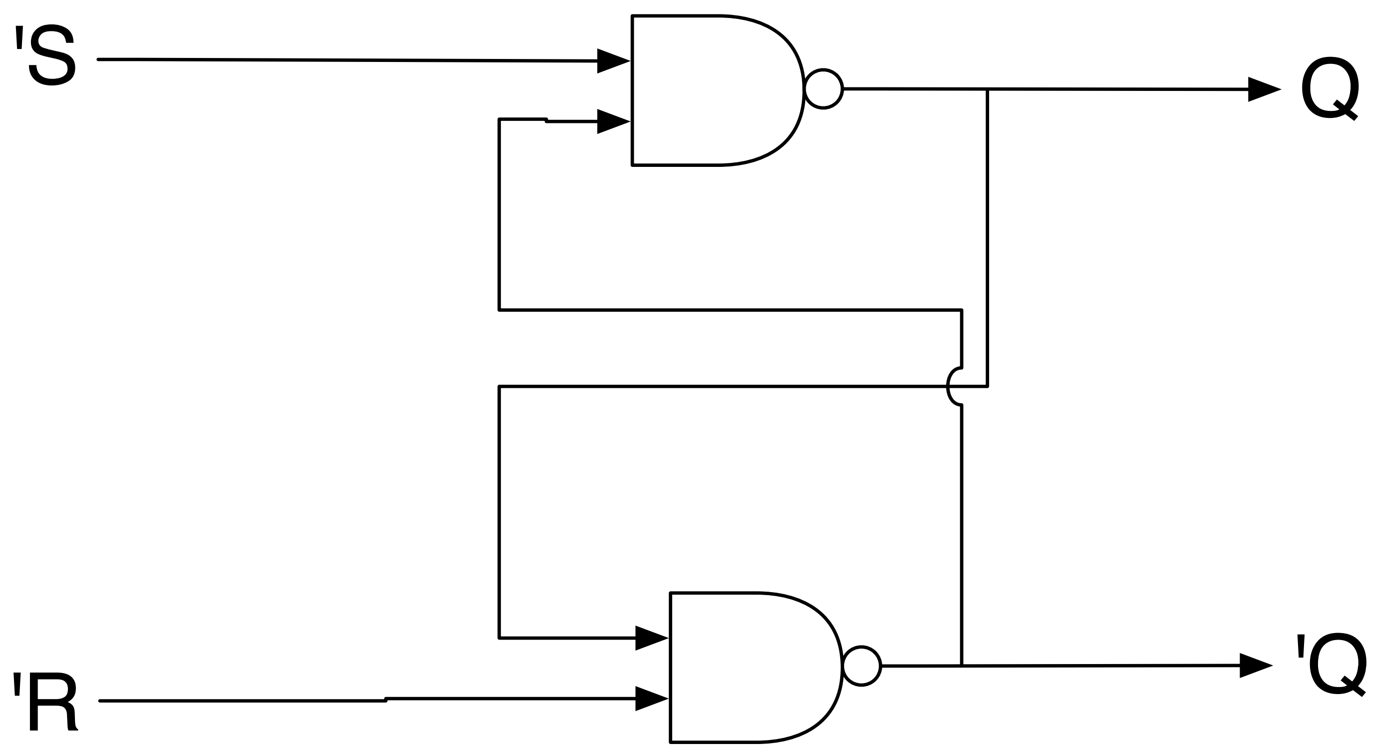
SR latch characteristic table



S	R	next state
0	0	no change
0	1	reset (Q=0)
1	0	set (Q=1)
1	1	invalid

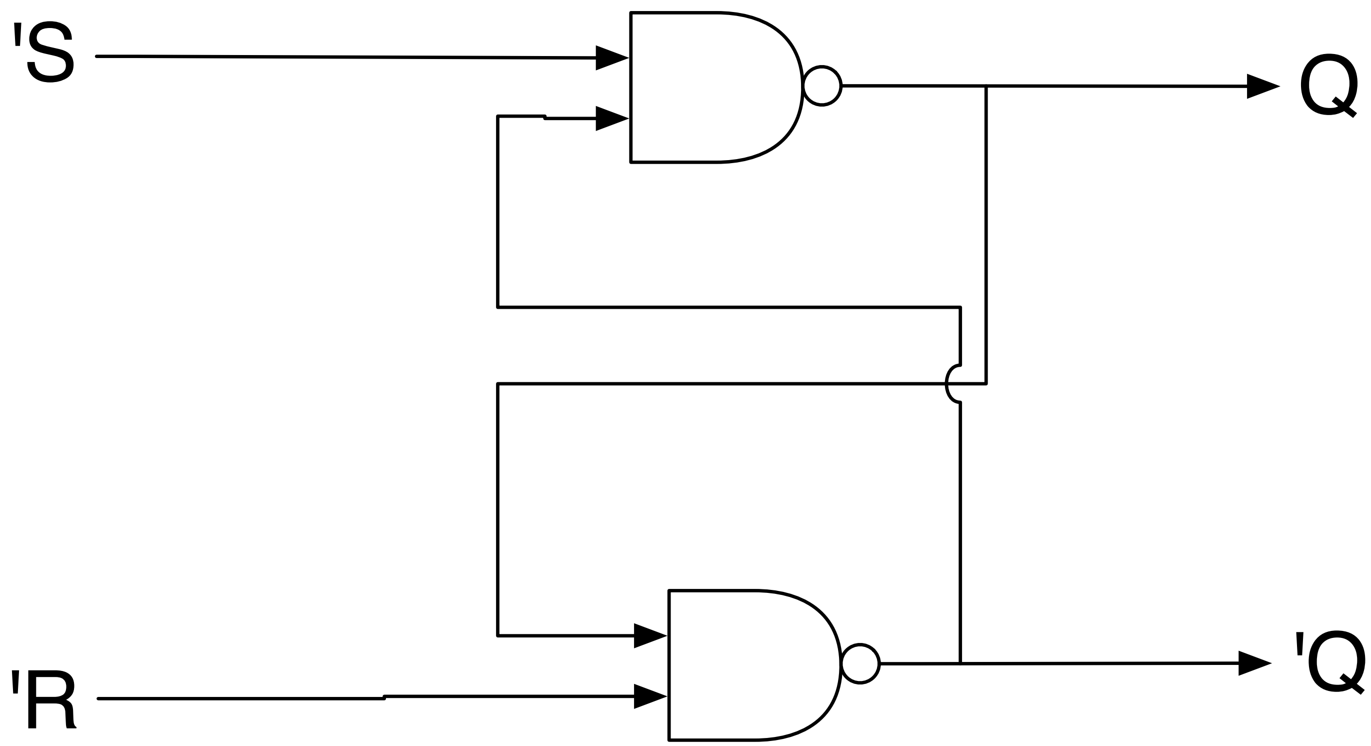
`S`R latch

- Latch constructed of cross-coupled NAND gates



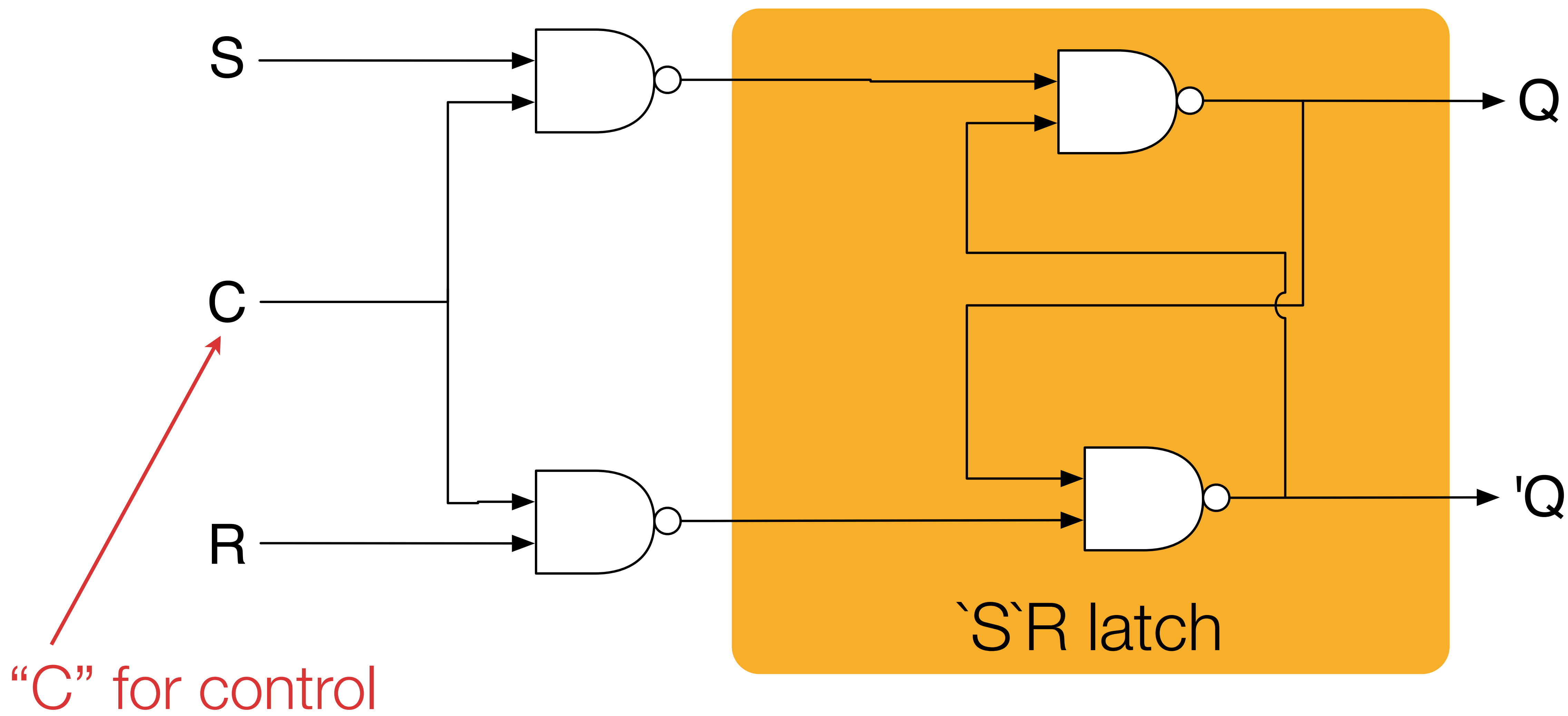
- This latch holds its state when both inputs are 1. `S = 0 makes Q = 1, `R = 0 makes Q = 0.

`S`R latch characteristic table

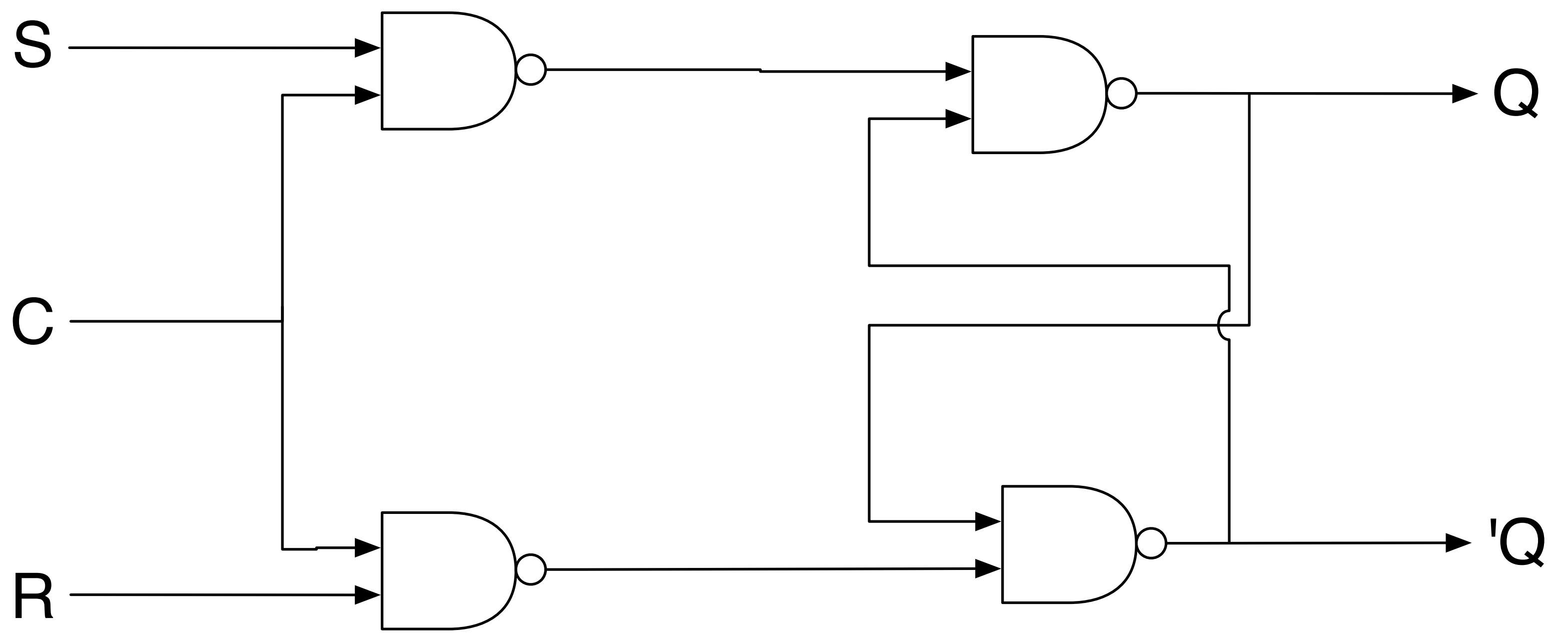


`S	`R	next state
0	0	invalid
0	1	set (Q=1)
1	0	reset (Q=0)
1	1	no change

SR latch with control input

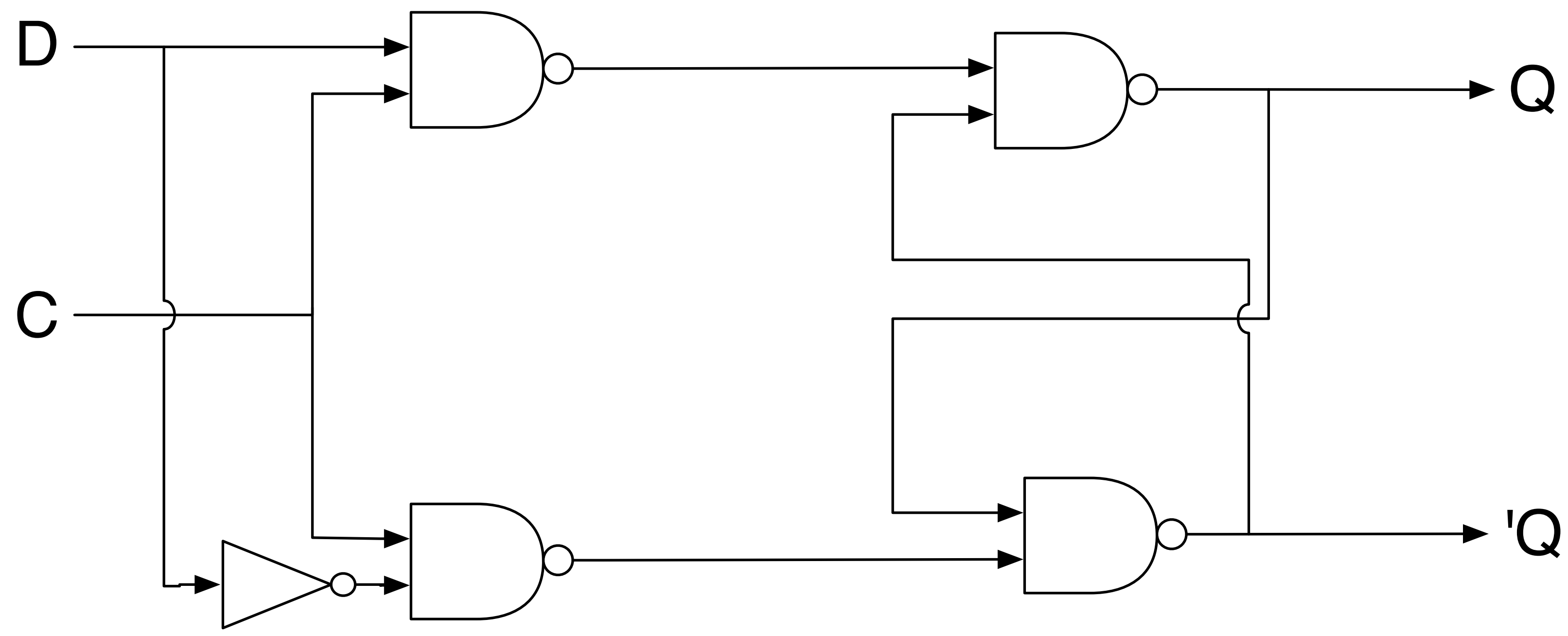


SR latch with control input characteristic table



C	S	R	`S	`R	next state
0	x	x	1	1	no change
1	0	0	1	1	no change
1	0	1	1	0	reset (Q=0)
1	1	0	0	1	set (Q=1)
1	1	1	0	0	invalid

D latch with control input characteristic table

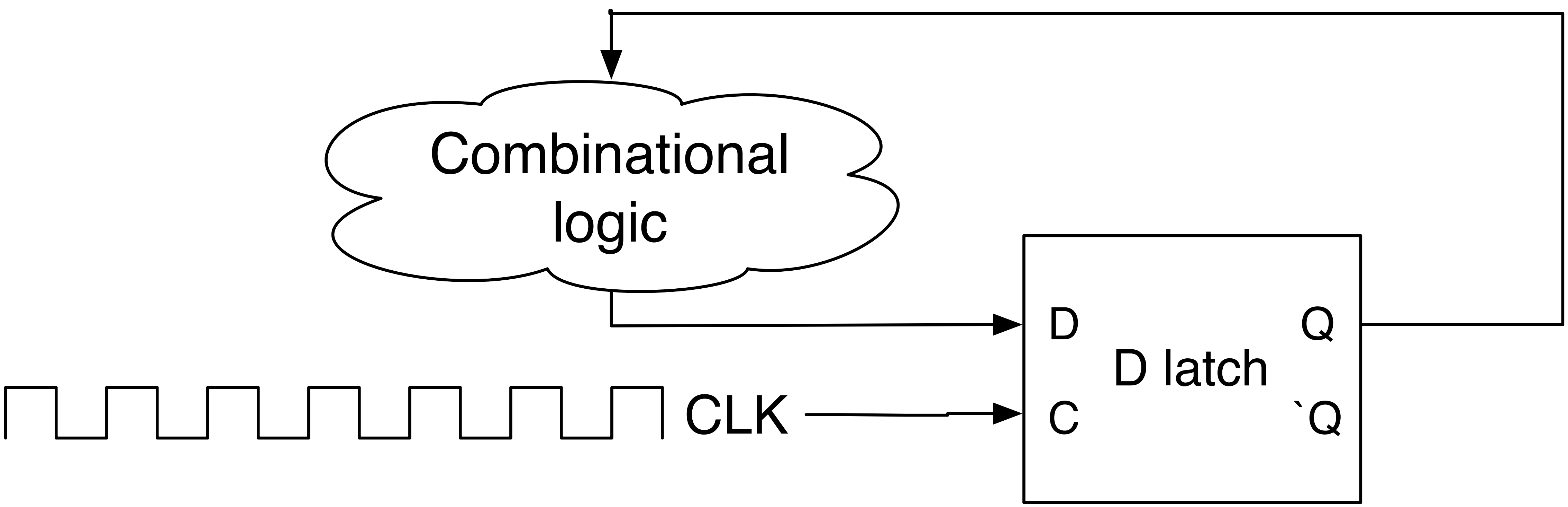


C	D	\`S	\`R	next state
0	x	1	1	no change
1	0	1	0	reset (Q=0)
1	1	0	1	set (Q=1)

Flip-flops (synchronous storage elements)

Why we need flip flops

- This circuit is not safely (predictably) synchronous



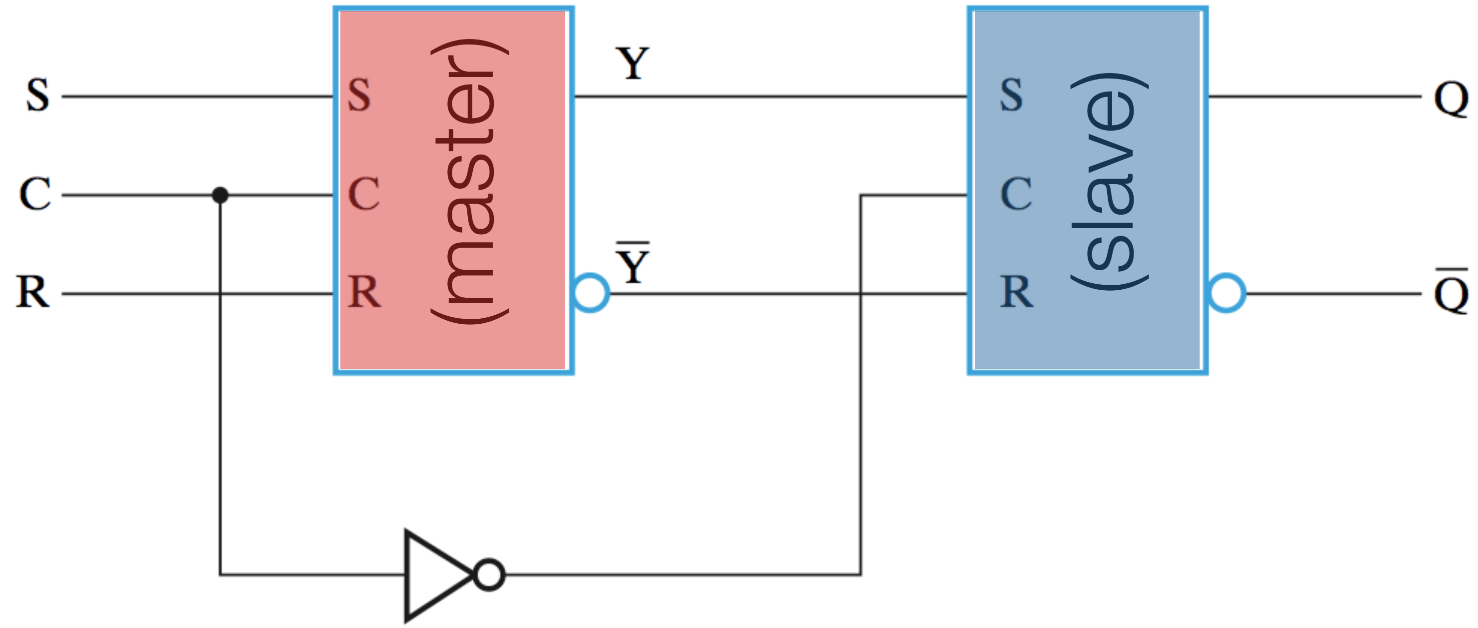
- The problem is transparency of latches: as soon as the input changes, at some time later the output will change

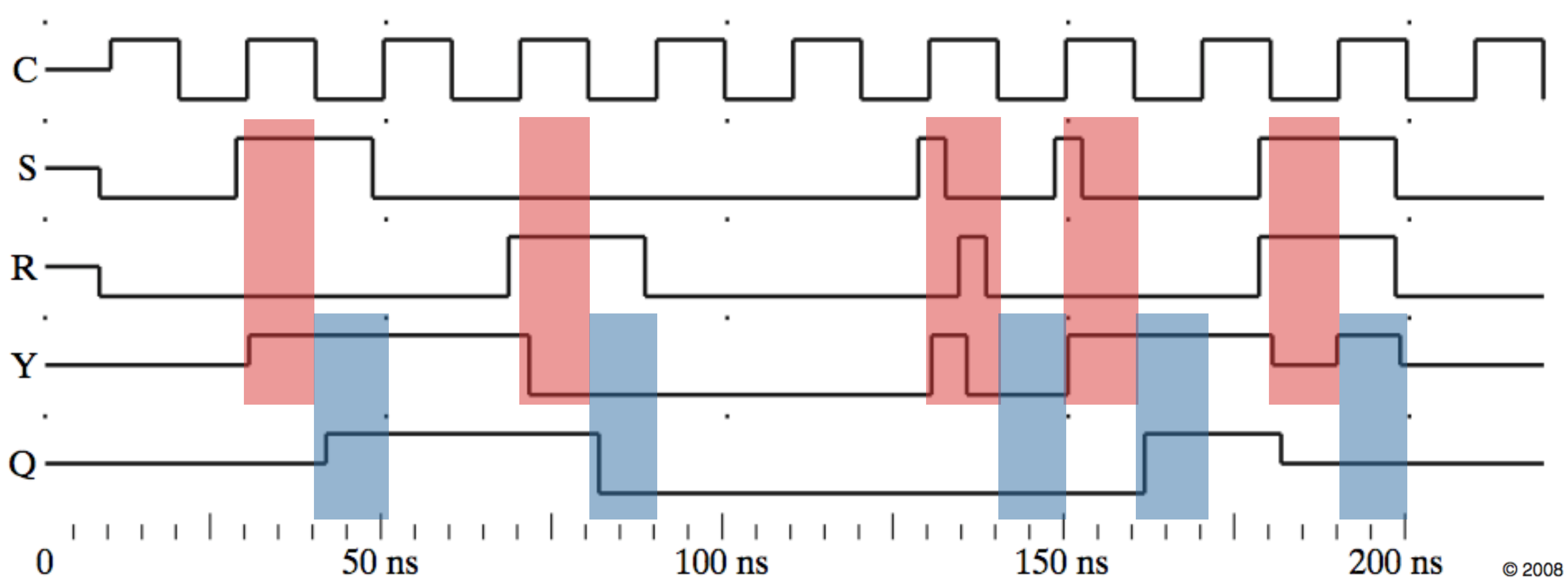
- Flip flops are designed so that outputs will **not** change within a single clock pulse

SR master-slave flip-flop

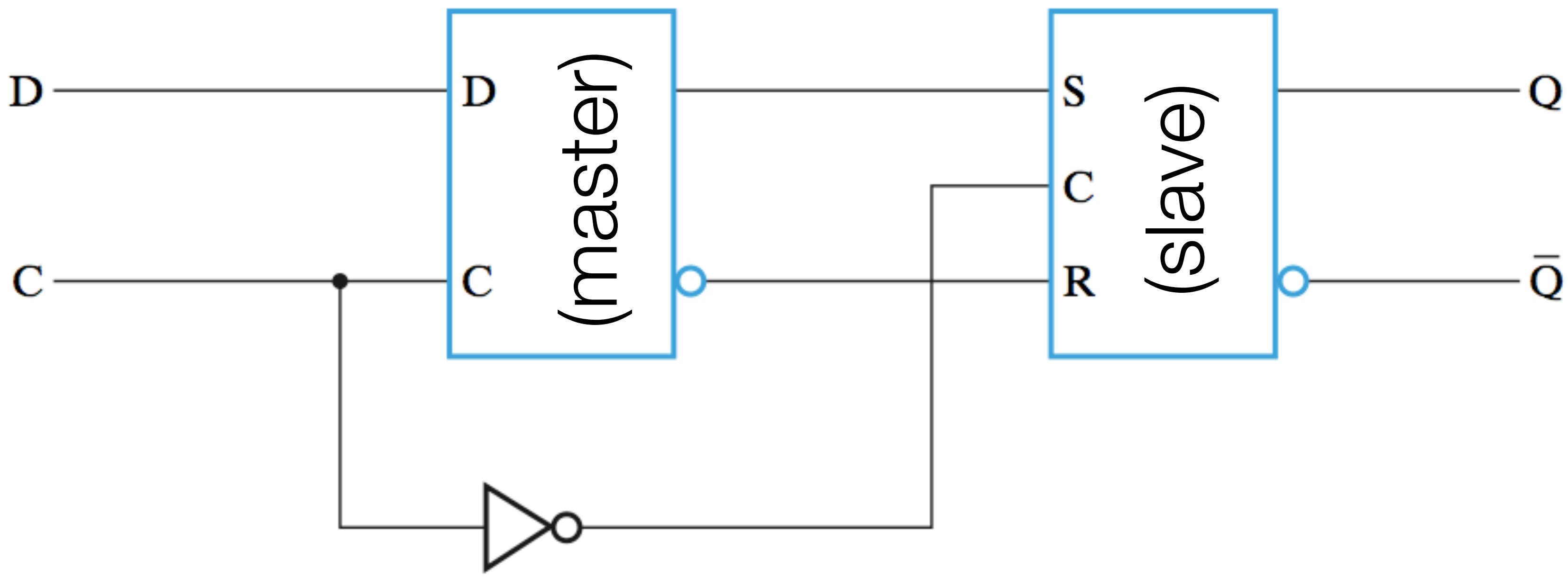
Internal state (Y) updated when CLK=1

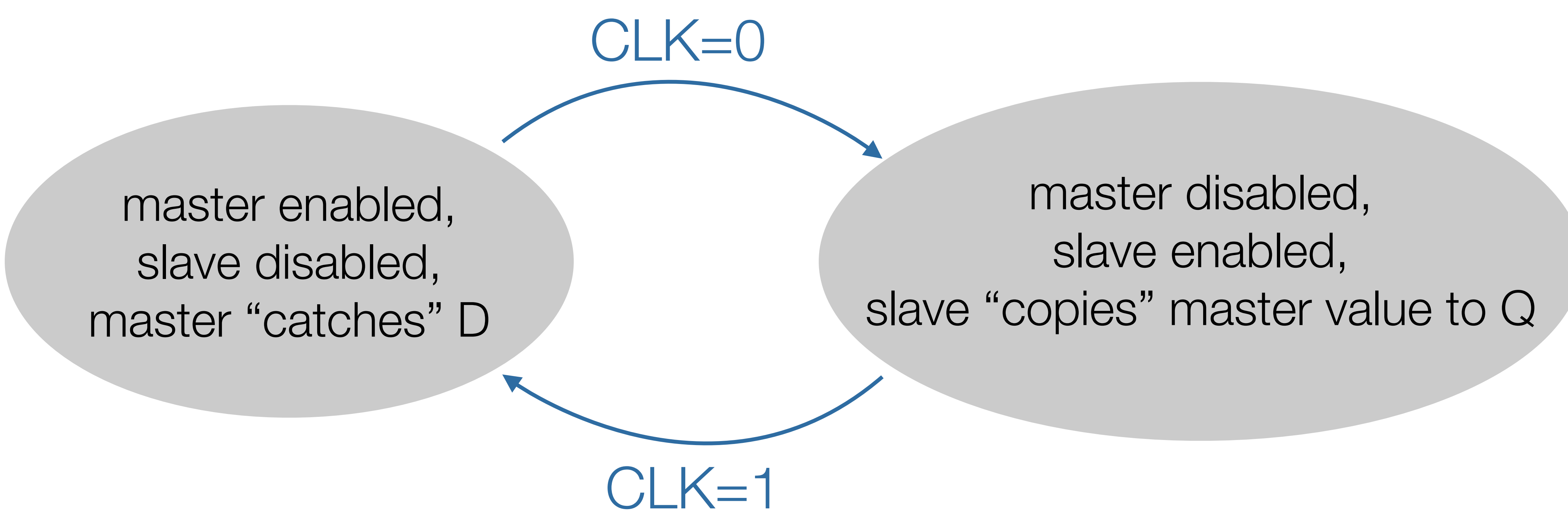
External state (Q) updated when CLK=0



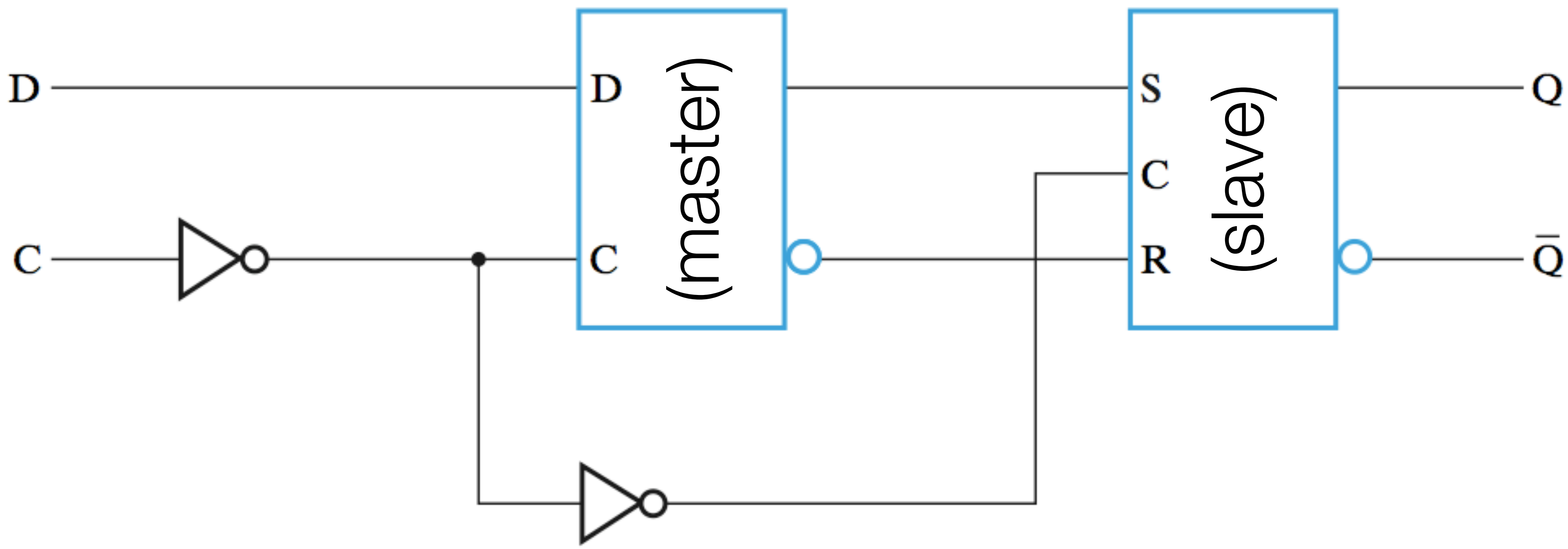


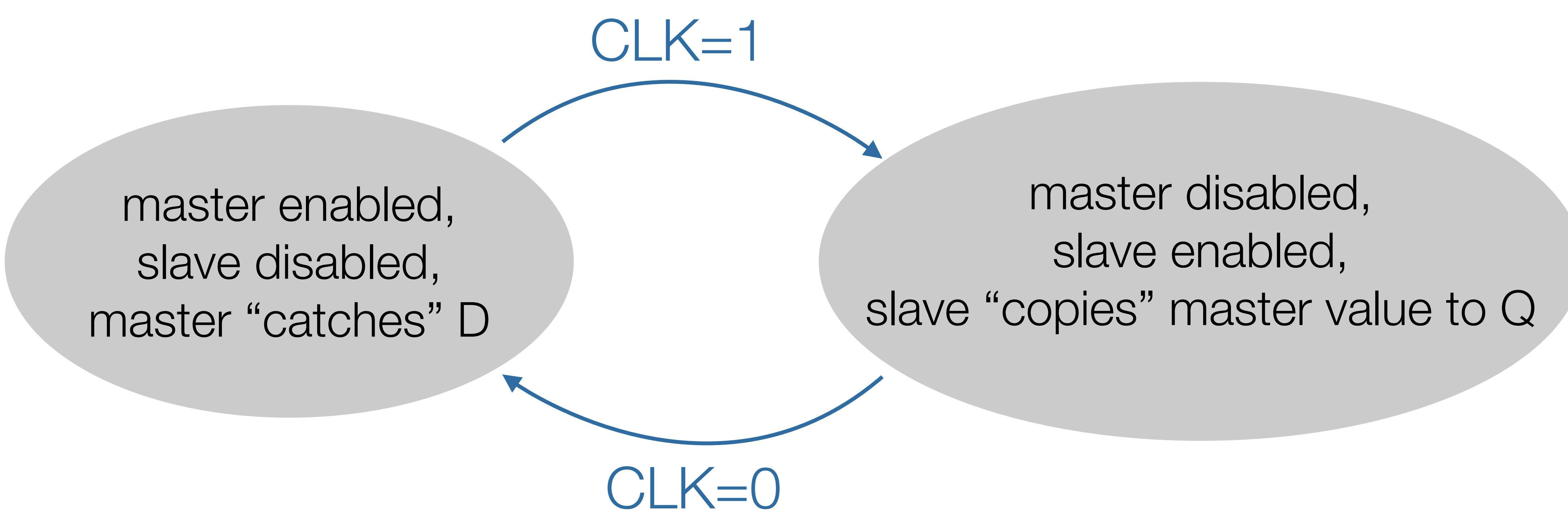
Negative-edge-triggered D flip-flop



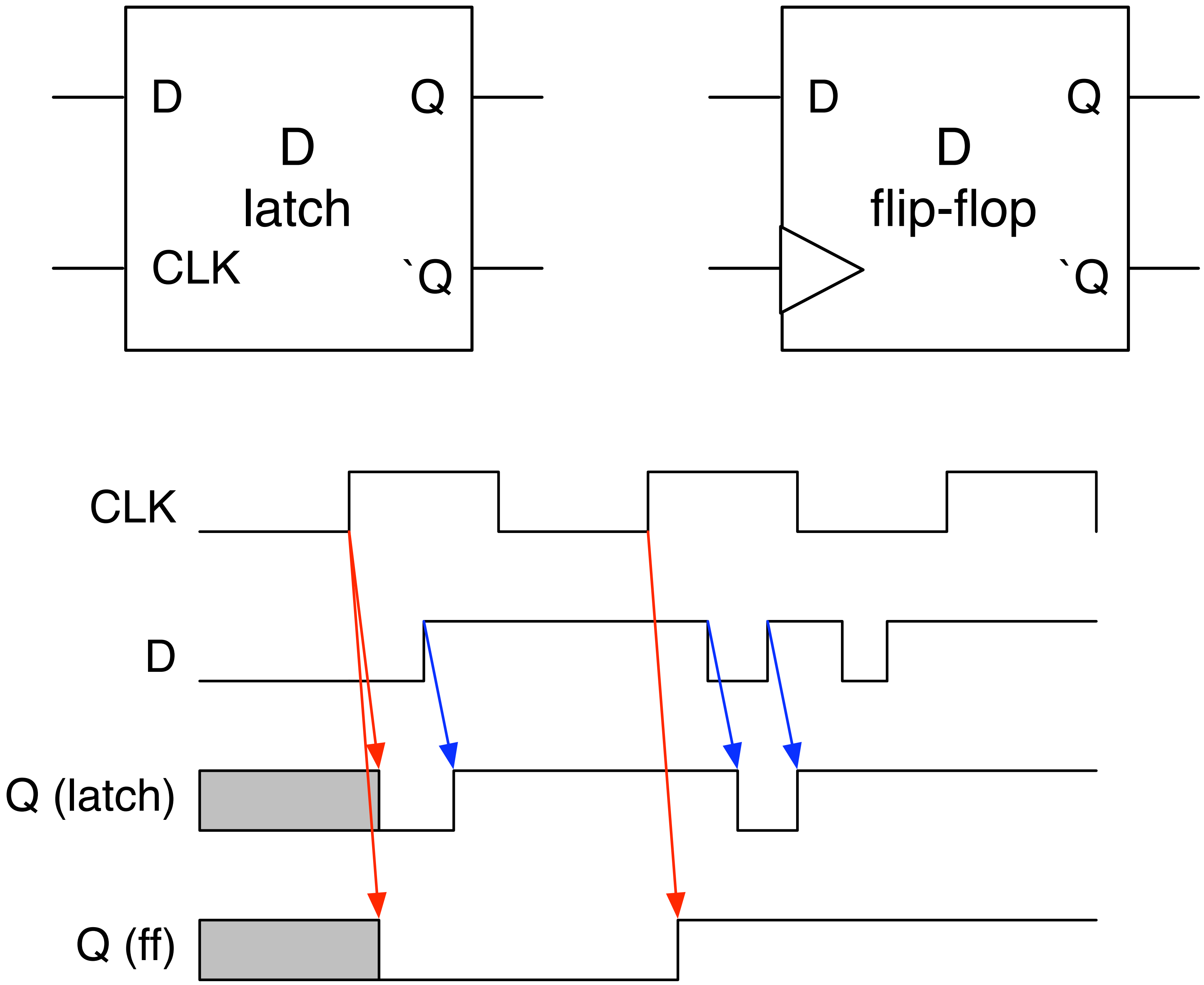


Positive-edge-triggered D flip-flop

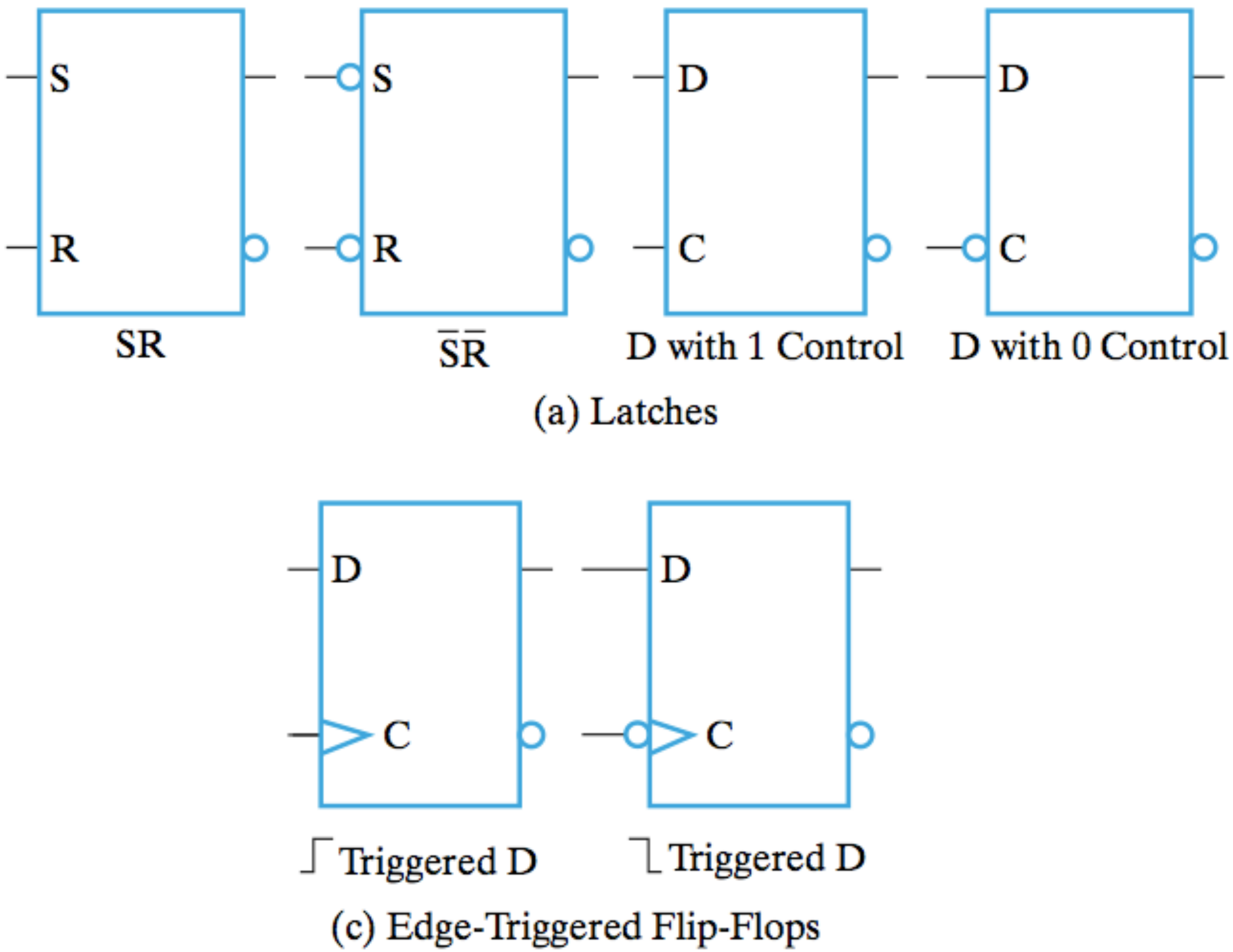




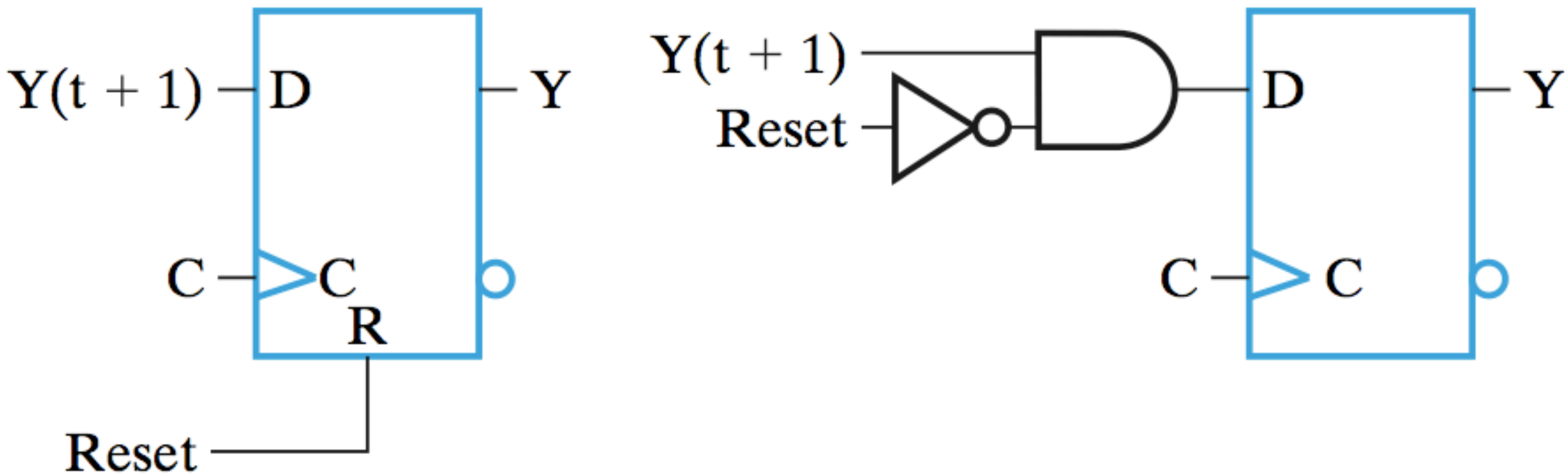
D latch v. D flip-flop



Some notes on notation



Adding reset signals



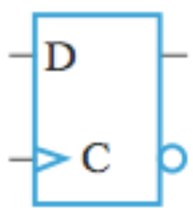
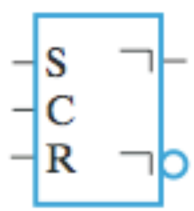
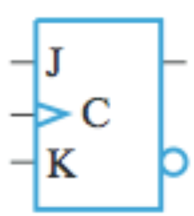
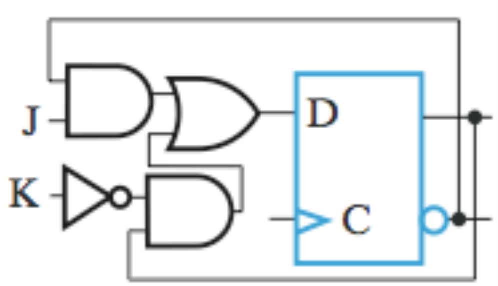
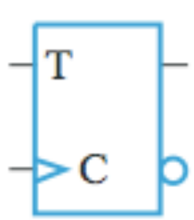
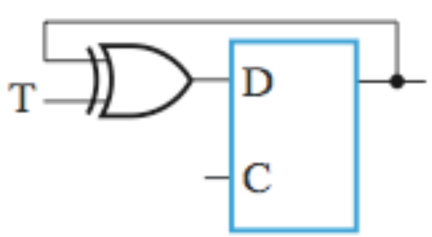
(a) Asynchronous Reset

(b) Synchronous Reset

(resets immediately)

(resets at clock edge only)

Two more flip-flops: JK and T flip-flops

Type	Symbol	Logic Diagrams	Characteristic Equation
D		See Figure 5-12	$Q(t+1) = D(t)$
SR		See Figure 5-9	$Q(t+1) = S(t) + \bar{R}(t)\,Q(t)$
JK			$Q(t+1) = J(t)\,\bar{Q}(t) + \bar{K}(t)\,Q(t)$
T			$Q(t+1) = T(t) \oplus Q(t)$

Characteristic Table

D:

D	Q(t+1)	Operation
0	0	Reset
1	1	Set

SR:

S	R	Q(t+1)	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

JK:

J	K	Q(t+1)	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}(t)$	Complement

T:

T	Q(t+1)	Operation
0	$Q(t)$	No change
1	$\bar{Q}(t)$	Complement

Excitation Table

D:

Q(t+1)	D	Operation
0	0	Reset
1	1	Set

SR:

Q(t)	Q(t+1)	S	R	Operation
0	0	0	X	No change
0	1	1	0	Set
1	0	0	1	Reset
1	1	X	0	No change

JK:

Q(t)	Q(t+1)	J	K	Operation
0	0	0	X	No change
0	1	1	X	Set
1	0	X	1	Reset
1	1	X	0	No Change

T:

Q(t+1)	T	Operation
$Q(t)$	0	No change
$\bar{Q}(t)$	1	Complement