CSEE 3827: Fundamentals of Computer Systems

Lecture 6

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Combinational circuits

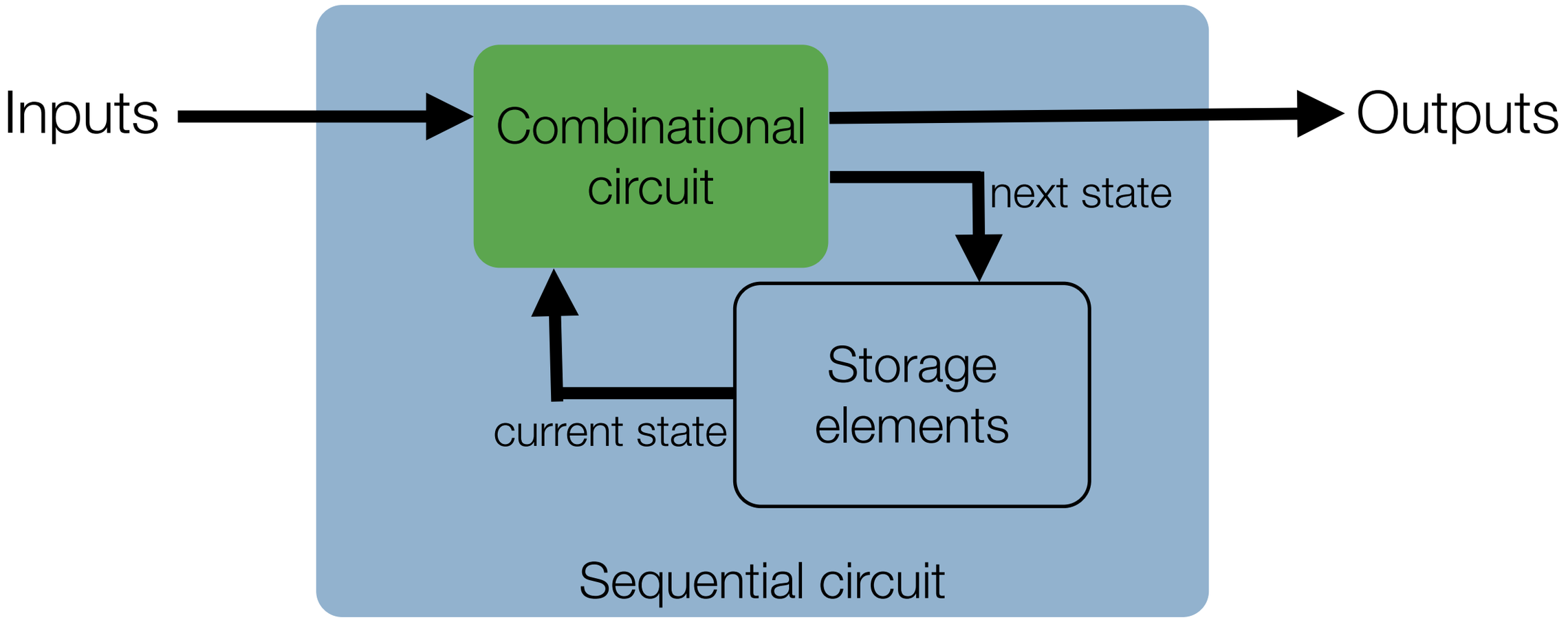
- Combinational circuits are stateless

- The outputs are functions only of the intputs

Sequential circuits

- Sequential circuits have state

- The outputs are functions of both the current inputs and the current state of the circuit



Design procedure

1.Specification

(define desired behavior)

2.Formulation

(derive a truth table or boolean equations that relate outputs to inputs)

3.Optimization

4.Technology Mapping

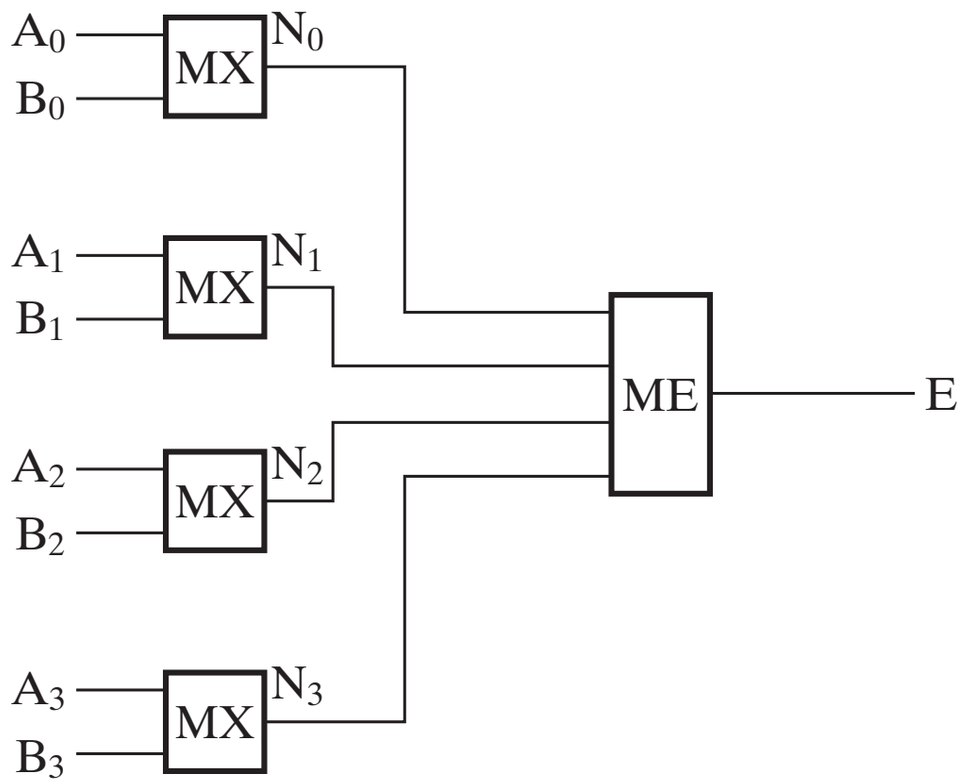
(transform circuit to use available gates (e.g., NANDs))

5.Verification

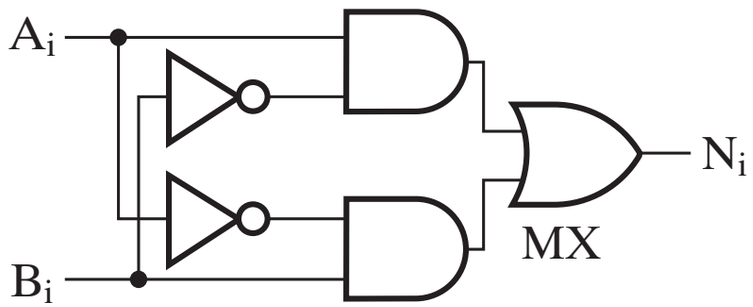
(verify that final design behaves correctly)

Hierarchical design

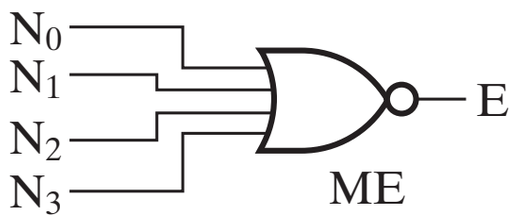
(4-bit equality comparator)



(a)



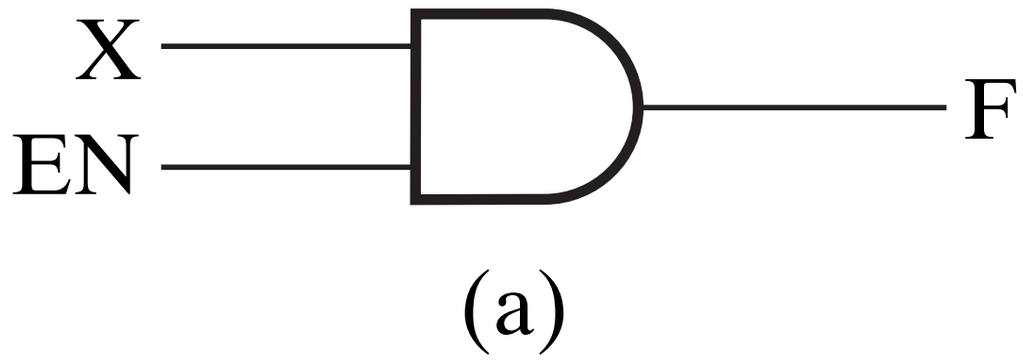
(b)



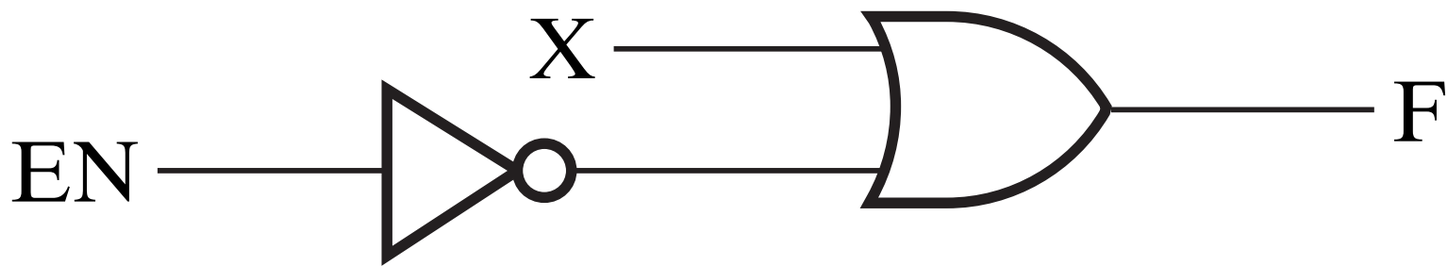
(c)

Enabling

Enabled circuits



(a)



(b)

Output is enabled only when input ‘ENABLE’ signal is asserted

Enabling example: Car control

- Inputs:
  - IG (ignition switch)
  - LS (light switch)
  - RS (radio switch)
  - WS (power window switch)
- Outputs
  - L (lights)
  - R (radio)
  - W (power windows)

What are the enabling relationships?

What is the truth table for this system?

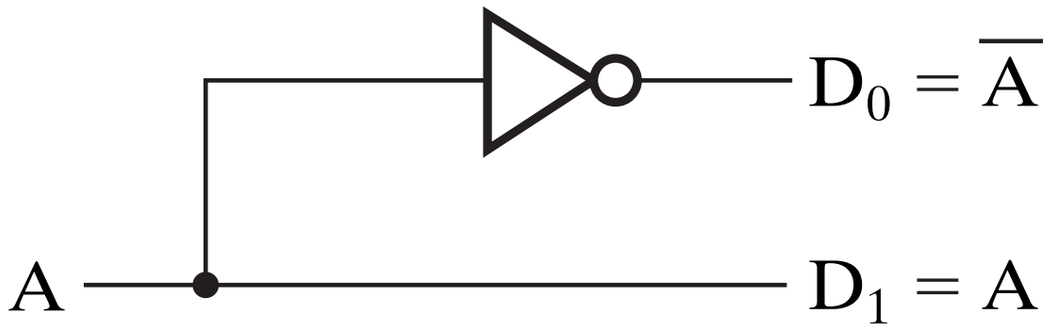
Decoding

Decoder (1:2)

Converts n-bit input to m-bit output, where n <= m <= 2^n

A	D_0	D_1
0	1	0
1	0	1

(a)



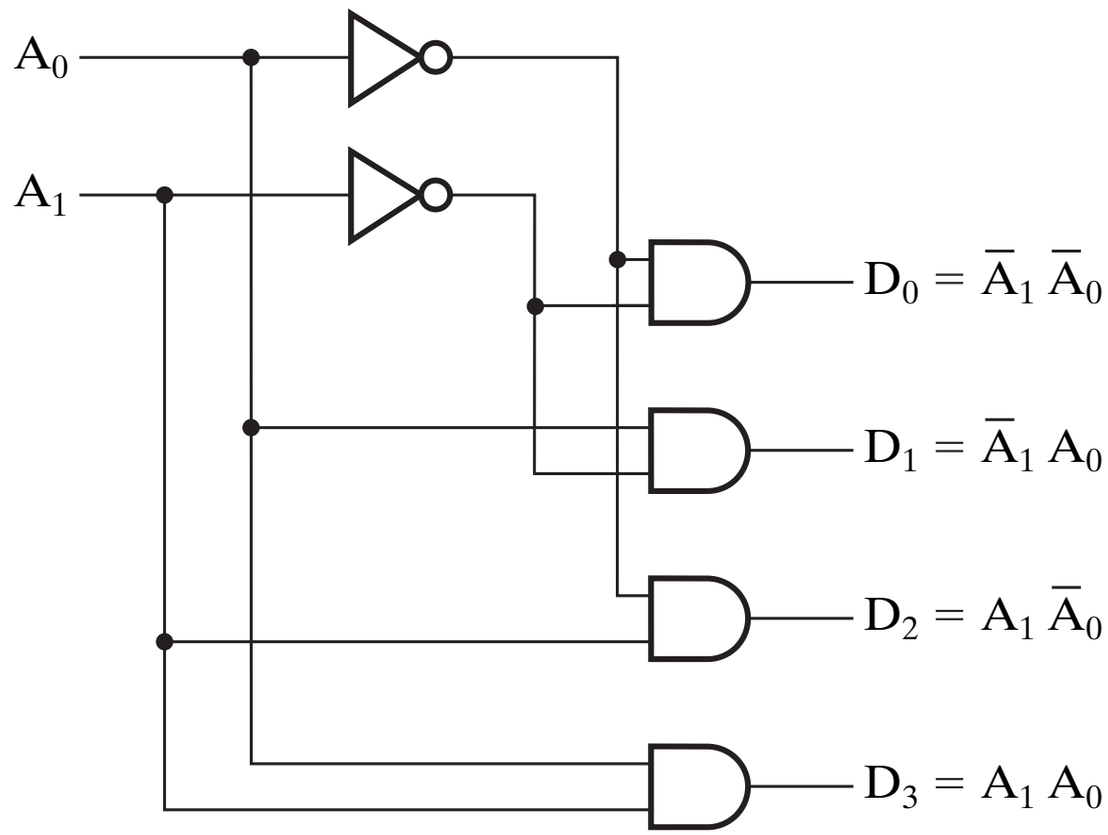
(b)

Decoder (2:4)

n

A_1	A_0	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

(a)

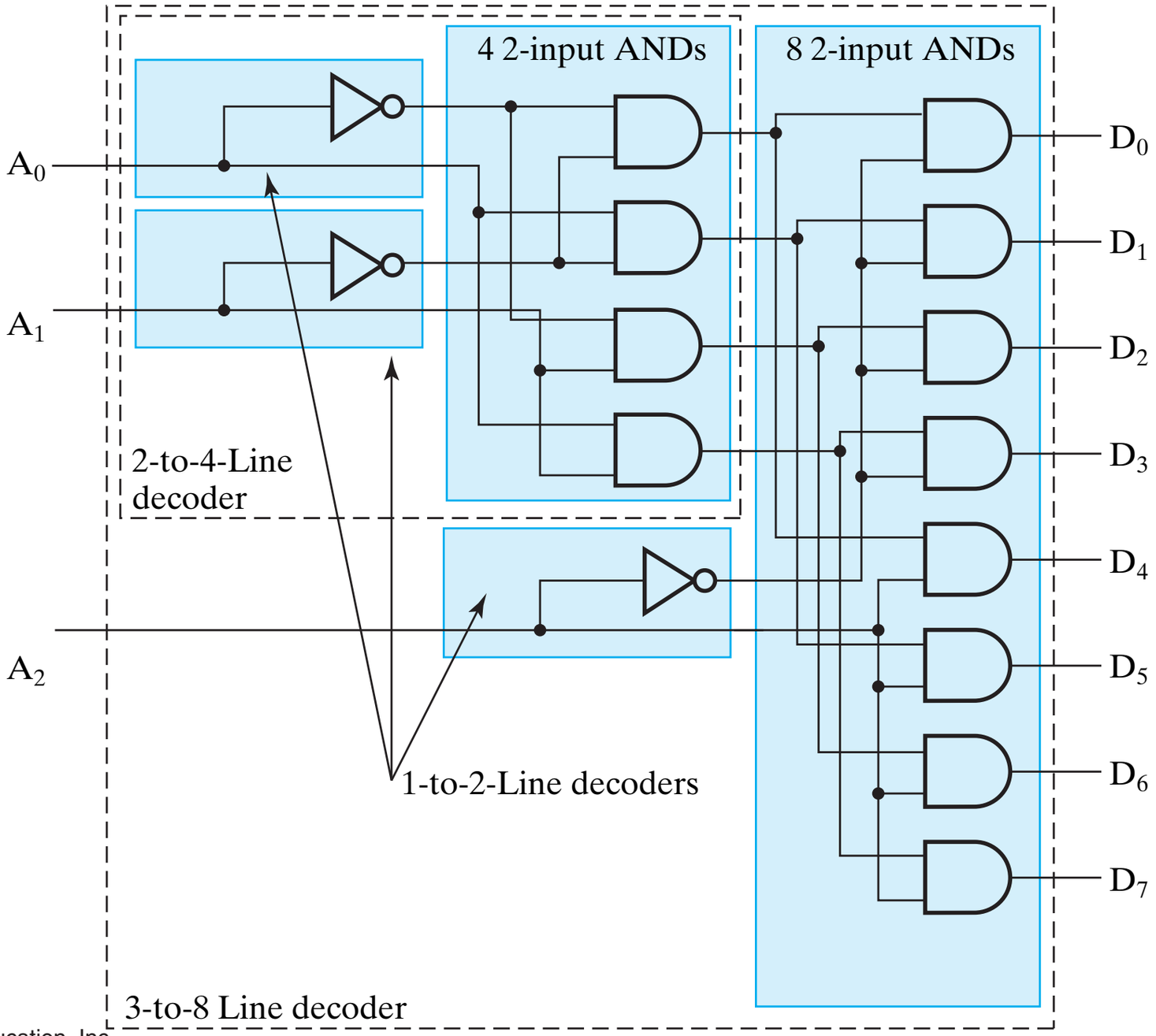


(b)

Decoder (3:8)

Hierarchical design: use small decoders to build bigger decoder

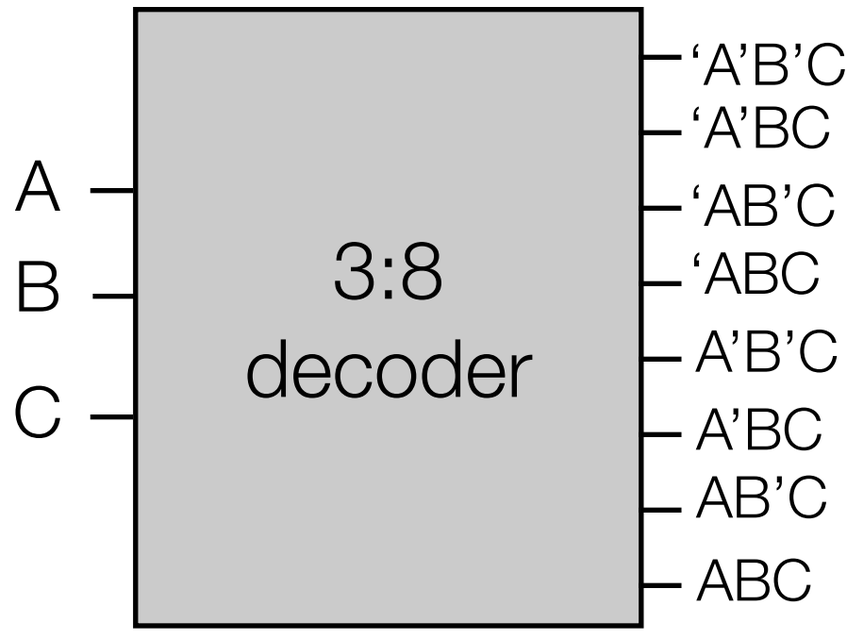
3-19



M. Morris Mano & Charles R. Kime
LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 4e

Decoder-based circuits

- If decoders produce minterms...



Encoding

Encoders

T 3-7

Inverse of a decoder: converts m-bit input to n-bit output, where $n <= m <= 2^n$

TABLE 3-7
Truth Table for Octal-to-Binary Encoder

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

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T 3-7

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0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Priority Encoder

T 3-8

TABLE 3-8
Truth Table of Priority Encoder

Inputs				Outputs		
D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

Code conversion

General code conversion

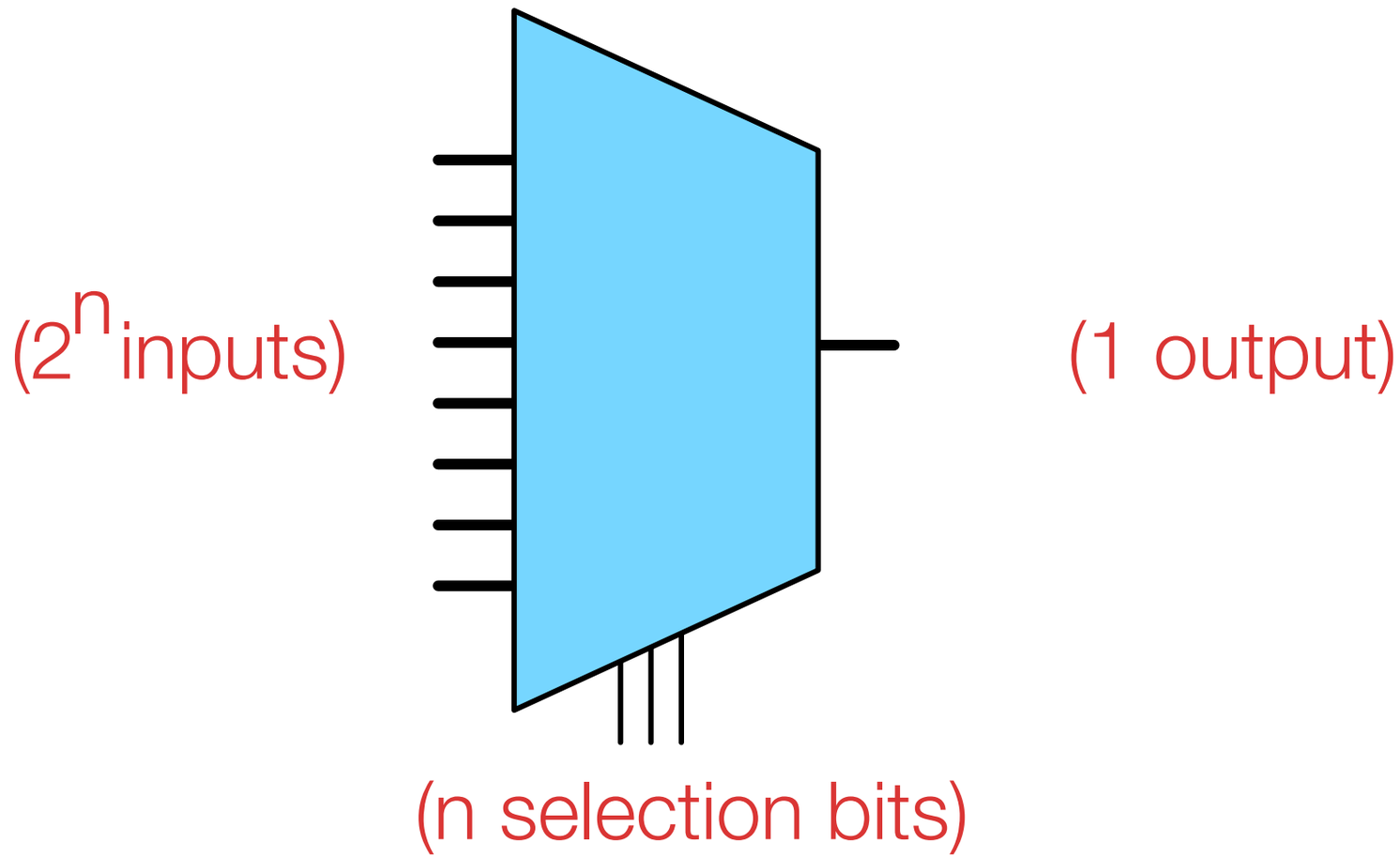
3-3

(a) Segment designation (b) Numeric designation for display

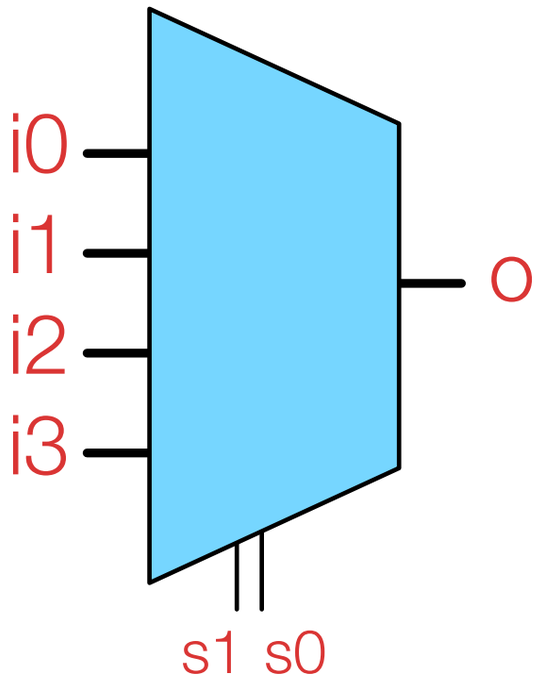
Multiplexers

Multiplexers

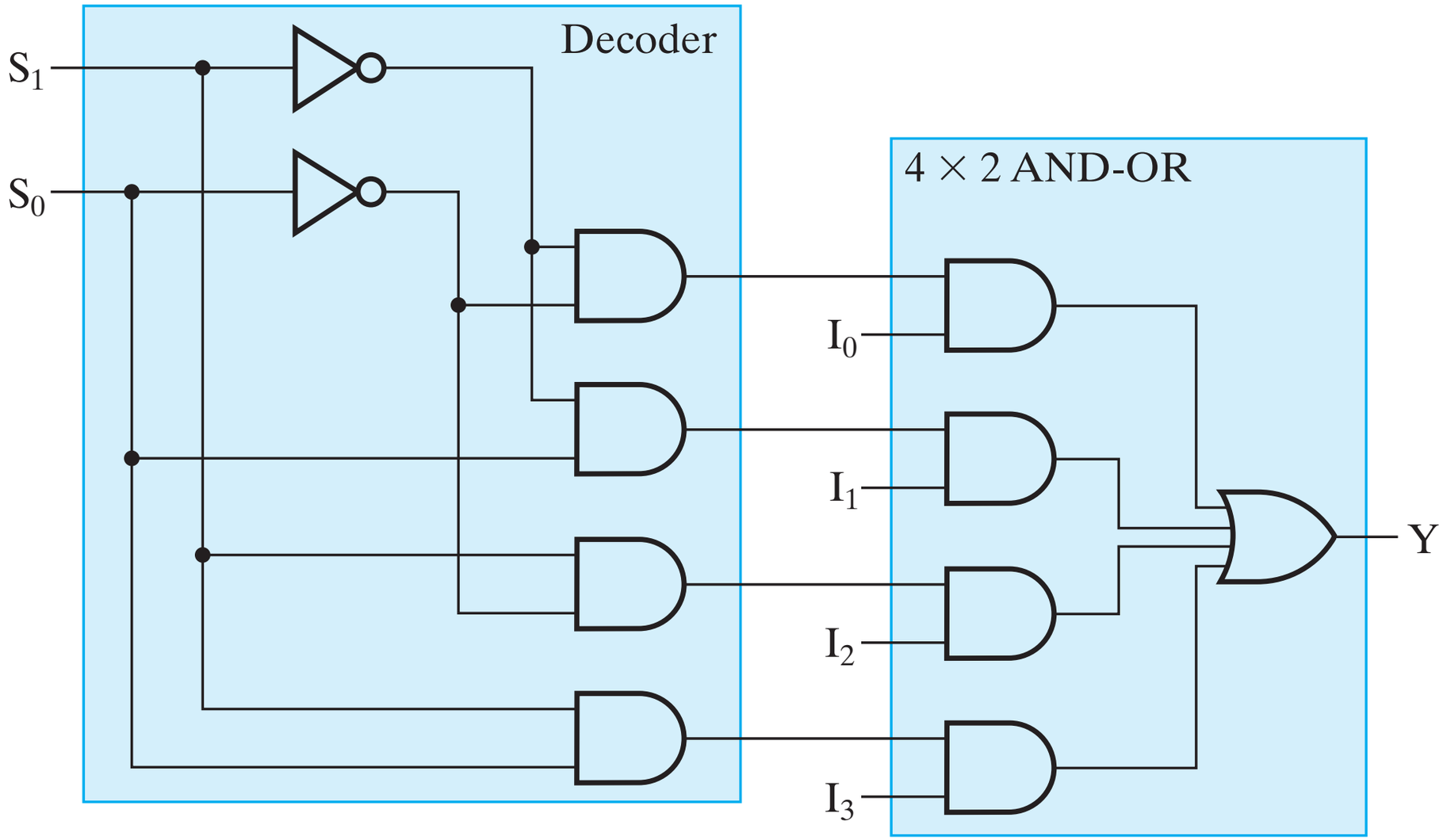
- Combinational circuit that selects binary information from one of many input lines and directs it to one output line



Truth table for a 4:1 mux



Internal mux organization



Multibit multiplexing