CSEE 3827: Fundamentals of Computer Systems

Lecture 10

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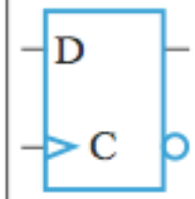
Flip-flop refresher

Flip-flop summary

D



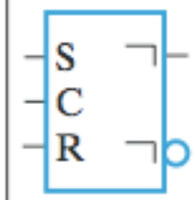
See Figure 5-12

D	Q(t+1)	Operation
0	0	Reset
1	1	Set

$Q(t+1) = D(t)$

Q(t+1)	D	Operation
0	0	Reset
1	1	Set

SR



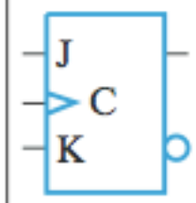
See Figure 5-9

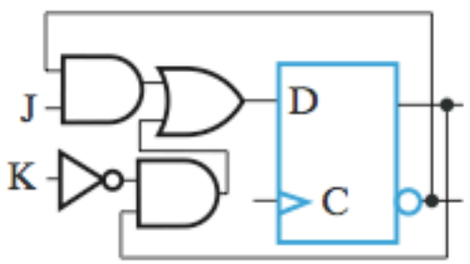
S	R	Q(t+1)	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

$Q(t+1) = S(t) + \bar{R}(t)\,Q(t)$

Q(t)	Q(t+1)	S	R	Operation
0	0	0	X	No change
0	1	1	0	Set
1	0	0	1	Reset
1	1	X	0	No change

JK



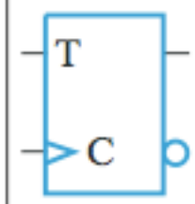


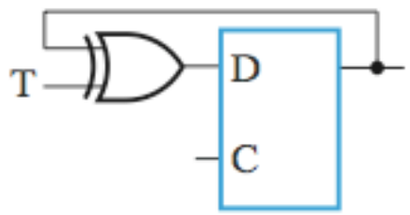
J	K	Q(t+1)	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}(t)$	Complement

$Q(t+1) = J(t)\,\bar{Q}(t) + \bar{K}(t)\,Q(t)$

Q(t)	Q(t+1)	J	K	Operation
0	0	0	X	No change
0	1	1	X	Set
1	0	X	1	Reset
1	1	X	0	No Change

T





T	Q(t+1)	Operation
0	$Q(t)$	No change
1	$\bar{Q}(t)$	Complement

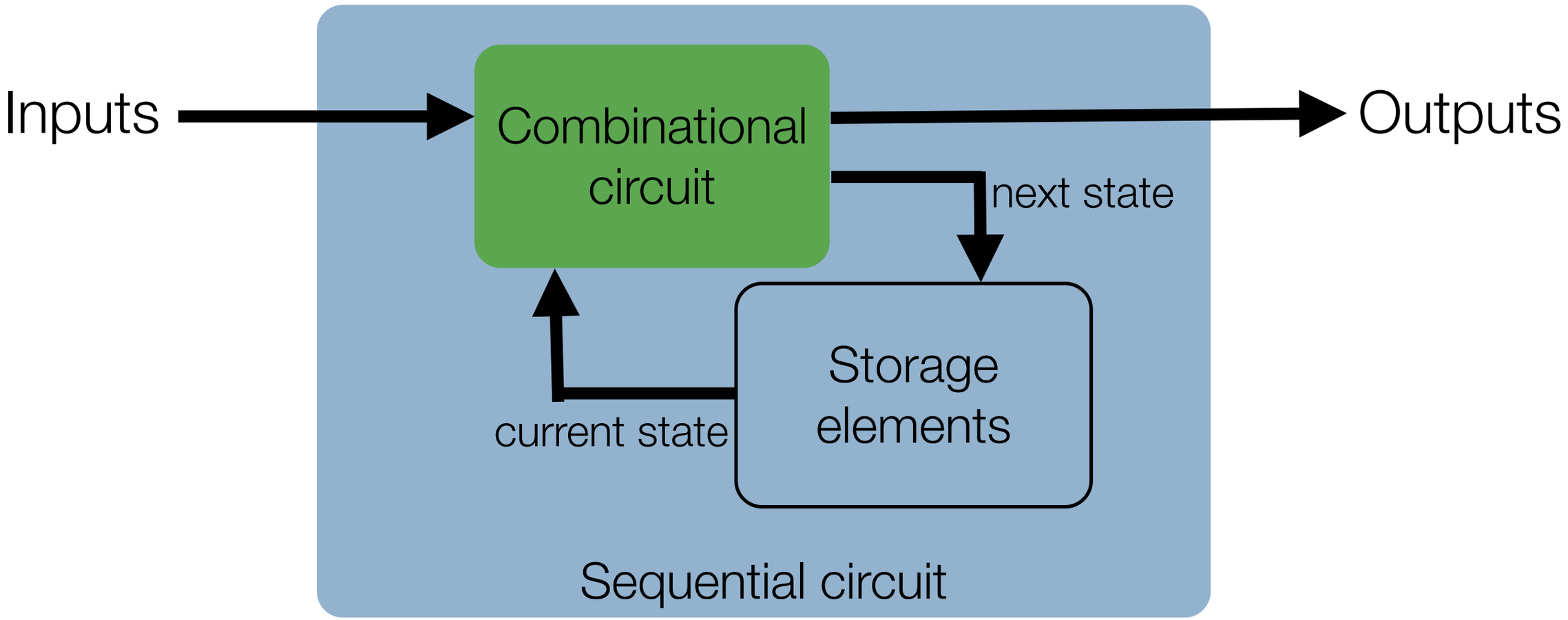
$Q(t+1) = T(t) \oplus Q(t)$

Q(t+1)	T	Operation
$Q(t)$	0	No change
$\bar{Q}(t)$	1	Complement

In class exercise: design a four-bit register

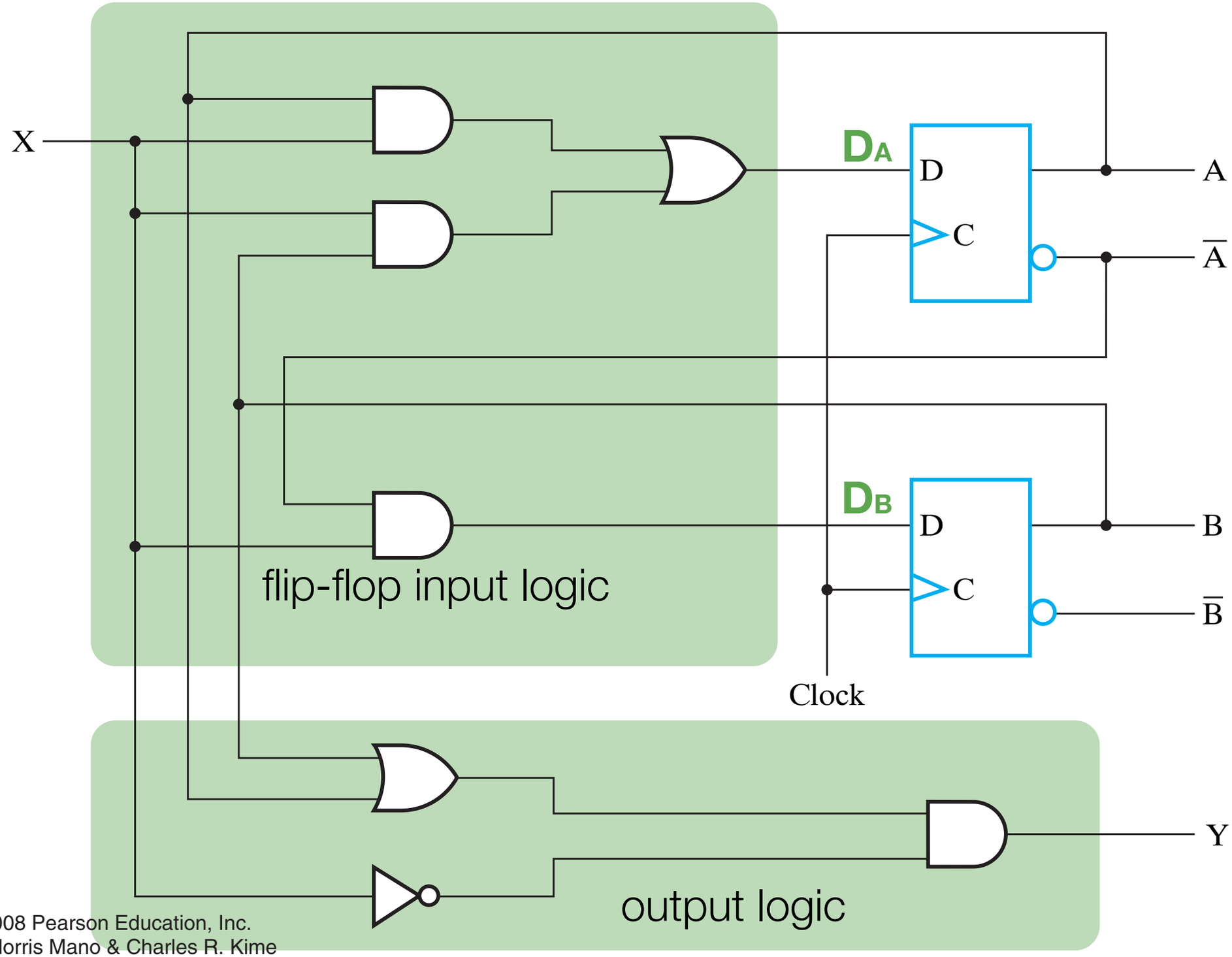
Finite state machines

Sequential circuit



Sequential circuit (schematic)

5-15



LOGIC AND COMPUTER DESIGN FUNDAMENTALS, 4e

Sequential circuit (1 dimensional state table)

T 5-1

TABLE 5-1
State Table for Circuit of Figure 5-15

Present State		Input	Next State		Output
A	B	X	A	B	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

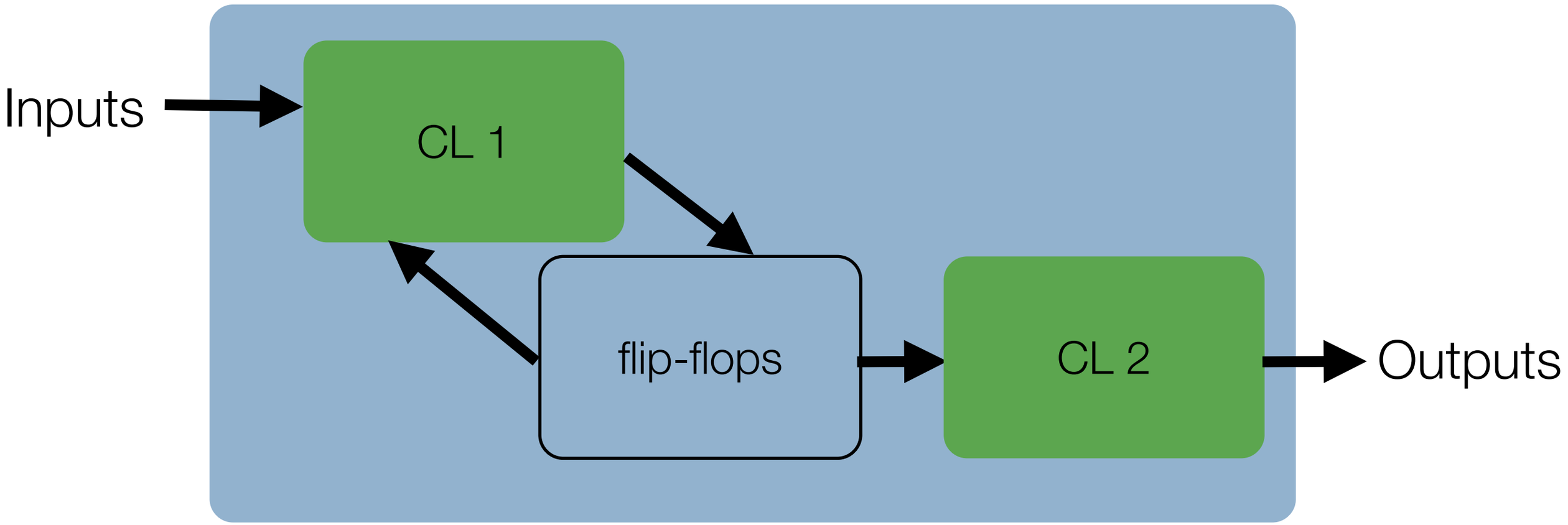
Sequential circuit (2 dimensional state table)

T 5-2

TABLE 5-2
Two-Dimensional State Table for the Circuit in Figure 5-15

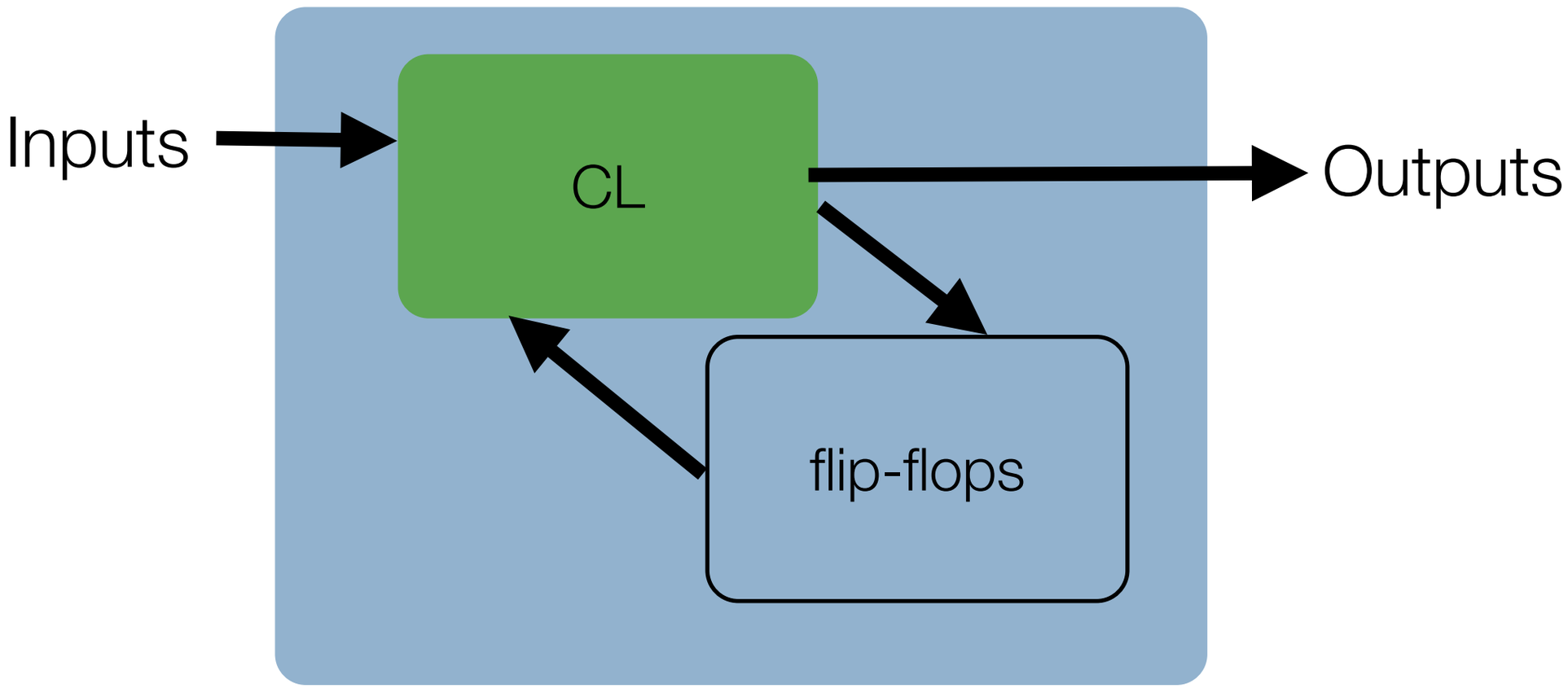
Present state		Next state				Output	
		X = 0		X= 0		X = 0	X = 1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

Moore circuit



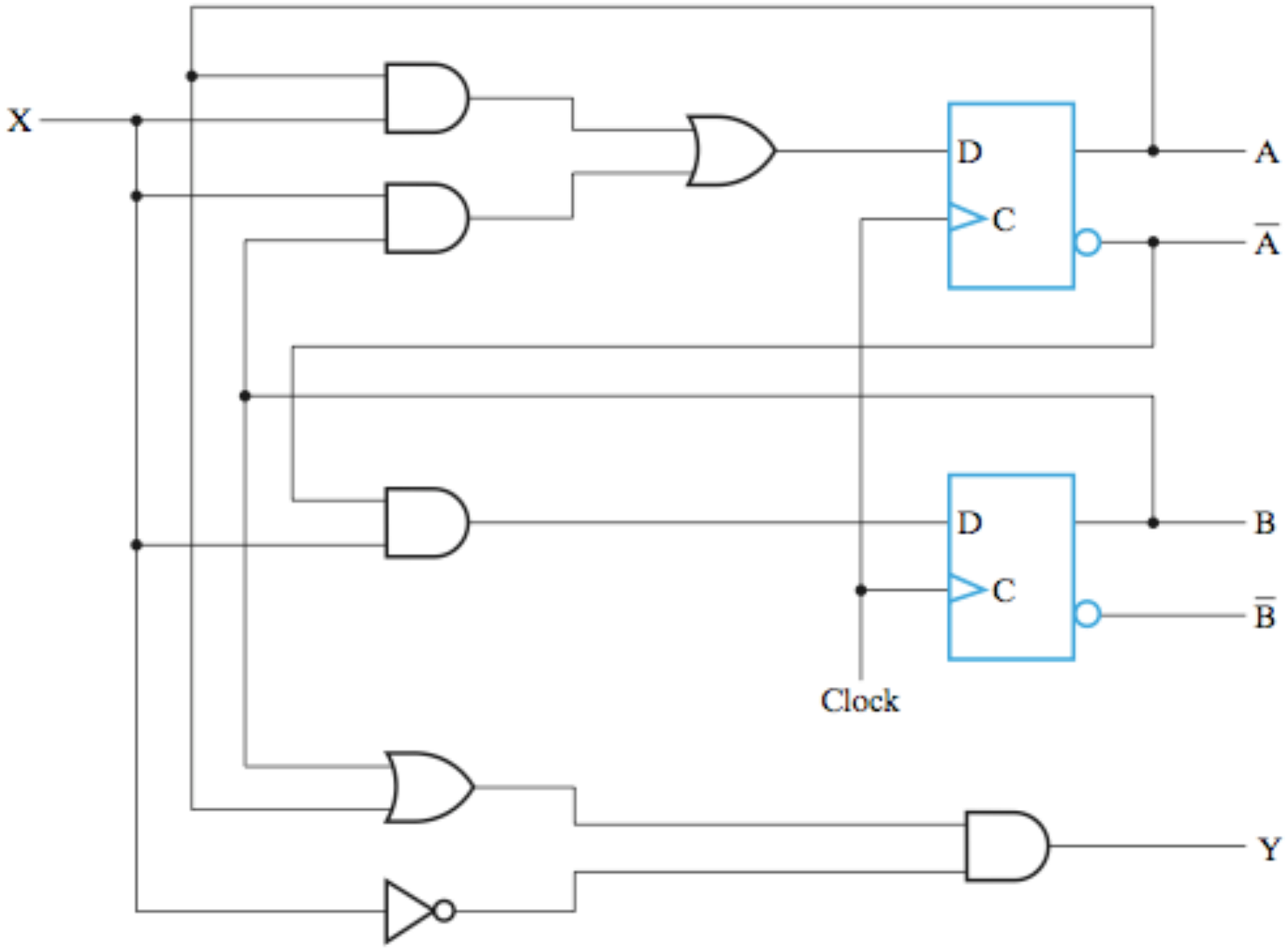
a *circuit in which the output depends only on the current state*

Mealy circuit

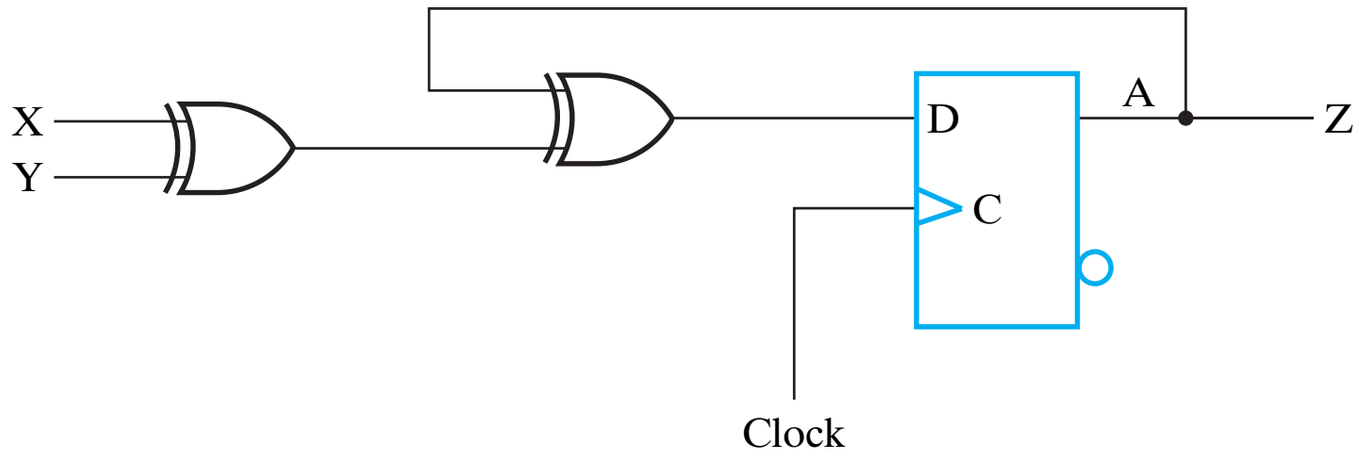


a circuit in which the outputs depend on the inputs as well as the current state

A Mealy or Moore circuit?



An example Moore circuit



(a)

Present state	Inputs		Next state	Output
A	X	Y	A	Z
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(b) State table

Alternate representation: state diagrams

State machine design procedure

1.Specification

2.Formulation

3.State assignment

4.Flip-flop input equation determination

5.Output equation determination

6.Optimization

7.Technology mapping

8.Verification

In class exercise: design a 3-bit counter

In class exercise: design a vending machine

- This vending machine will dispense a soda after the user has entered $.15
- Inputs: N, D (nickel, dime, quarter inserted)
- Output: R (release soda)