CSEE 3827: Problem Set 4 — Due: 3/9/09

Complete the following problems. Be sure to show your work for partial credit.

1. Gray codes have the useful property that consecutive numbers differ in only a single bit position. Design a 3-bit Gray code counter FSM with no inputs and three outputs. When reset, the output should be 000. On each clock edge, the output should advance to the next Gray code. After reaching 100, it should repeat with 000. Draw a schematic for this counter using T flip-flops.

Number	**Gray code**		
0	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	1	0
5	1	1	1
6	1	0	1
7	1	0	0

2. Suppose you are told that a Moore machine has five flip-flops, three inputs, and nine outputs. Assume that the states are encoded as compactly as possible (e.g., no one-hot encoding) and that transitions are all explicitly labelled with an actual input value (e.g., no transitions with "x" labels). Answer the following questions:

   (a) What are the minimum and maximum numbers of states in the state diagram?

   (b) What are the minimum and maximum numbers of transition arrows starting at a particular state?

   (c) What are the minimum and maximum numbers of transition arrows that can end in a particular state?

   (d) What are the minimum and maximum numbers of different binary patterns that can be displayed on the outputs?

3. Design a combination lock as shown in the drawing below. Assume the internally known combination $C_3C_2C_1C_0$ as shown. The state of the lock is indicated by the output *locked*. Once unlocked (*locked* = 0) the lock should remain unlocked until the *lock* input is true. Once locked, the lock will remain locked until it has seen the initition sequence "000" followed by the correct combination $C_3 = 0, C_2 = 1, C_1 = 1, C_0 = 0$ on the input. Design the internal logic of this lock (using D flip-flops) and draw the circuit that implements it.