CSEE W3827
Fundamentals of Computer Systems
Homework Assignment 5

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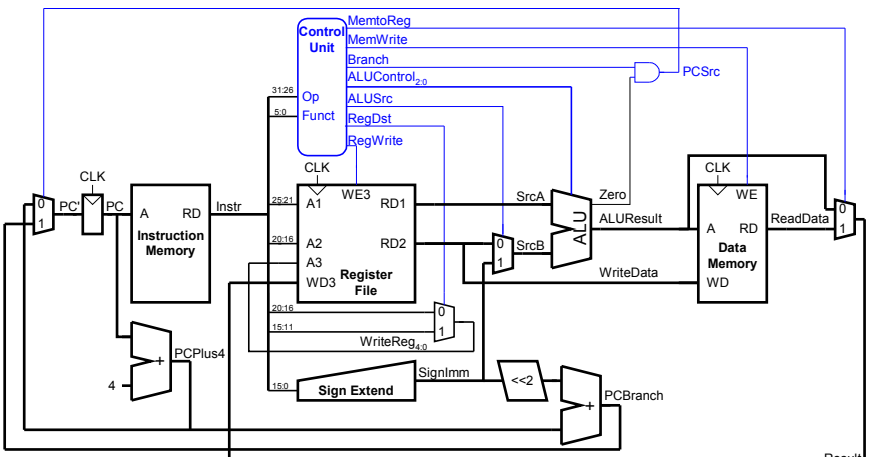
Due November 24, 2015 at 10:10 AM

Write your name **and UNI** on your solutions

Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

1. (30 pts.) Indicate the value on the wires listed on the next page when executing the given instruction. Indicate don't care values with an X. Otherwise use as specific a descriptor as possible. For example the value in memory at address A could be indicated with "Mem[A]".



	`sw $t3, 8($v0)`	`sub $s4, $t3, $a0`
MemtoReg		
MemWrite		
Branch		
$ALUControl_{2:0}$		
ALUSrc		
RegDst		
RegWrite		
PCSrc		
ALUResult		
SignImm		

2. Assuming the single cycle datapath with the components and critical path described on the slides (mips-uarch.pdf, slide 17) as a baseline, analyze the impact of the following changes.

   (a) (10 pts.) If data memory were made 50% slower, how much slower would the processor become? (Give a percent.)

   (b) (10 pts.) If the ALU and adders were all made twice as fast, how much faster would the processor be? (Give a percent.)

   (c) (15 pts.) If you could halve the size of the MIPS register file, causing a 50ps decrease in register file read time and a 30% increase in the number of instructions (due to the loads and stores needed move data between memory and this smaller set of instructions), should you make the change? Provide quantitative support for your answer.

3. (35 pts.) A “stuck at” fault is a fabrication error where a wire is stuck at some constant value no matter what. Below, design a small MIPS function called `regwriteone` to detect whether the `RegDst` control wire is stuck at 1. Your function should take no arguments and return 1 if `RegDst` is stuck at 1 and 0 otherwise.

   Note: The functon should respect calling conventions, and use only instructions supported by our single cycle processor (`lw, sw, beq, addi, add, slt, and, or, addu, subu,` plus `jr` to return from the function.