1. (10 points) Show how to implement the 7-segment decoder shown in class using a 4:16 decoder and OR gates (of any size) [UPDATE: You may use inverters if you wish, but it is not mandatory.]
2. (15 points) Show how to implement $F = \overline{A}B + BD + \overline{A}B\overline{D} + \overline{B}CD$ using a 4:1 mux whose select bits are $A$ (most significant) and $B$. 
3. (15 points) Design a circuit that takes a 4-bit number and increments it by one. It should operate cyclically, so when the input is 15, the output should be 0.
4. (20 points) Give a schematic that compares three 8-bit values $A$, $B$, and $C$. Your circuit should output 1 if $A > B > C$, 0 otherwise. [UPDATE: Assume the 8-bit values are 2’s complement. You may also assume that the values on $A$, $B$, and $C$ will not cause overflow (i.e., no need for your implementation to handle overflow cases).]
5. (20 points) Design a histogram circuit that accepts eight 2-bit values and produces 4 4-bit values indicating how many times each of the four possible input values (00, 01, 10 and 11) appeared on the eight inputs. Provide a schematic for your design.
6. (20 points) Using full adders, design a circuit that accepts a seven-bit input and outputs the number of input bits that are 1 as a 3-bit binary number.