CSEE W3827

Fundamentals of Computer Systems

Homework Assignment 5

Prof. Martha A. Kim

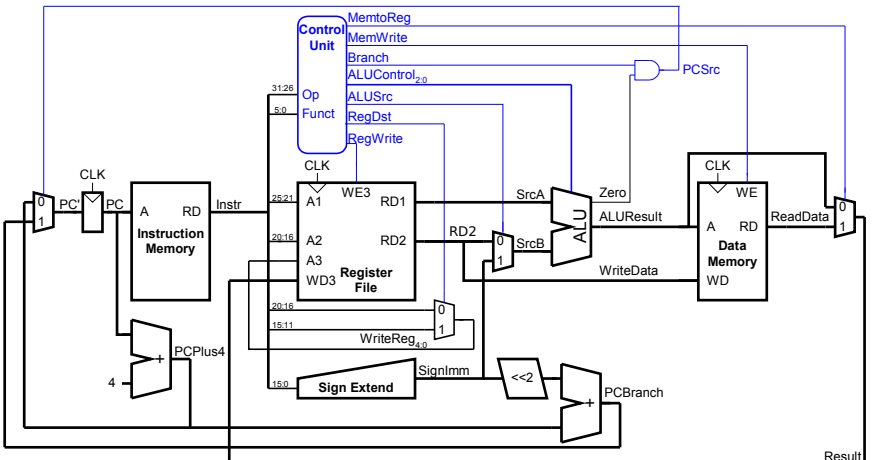
Columbia University

Due November 13, 2014 at 10:10 AM

Write your name **and UNI** on your solutions

Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

1. (30 pts.) List the wire names in the datapath below for which the **value is ignored** when executing the given instruction.



(a) `add $t0, $t0, $t1`

(b) `lw $t0, 4($a0)`

2. Assuming the following dynamic instruction frequency for a program running on the single-cycle MIPS processor...

`add`	15%
`addi`	25%
`beq`	10%
`lw`	30%
`sw`	20%

(a) (5 pts.) ... in what fraction of all cycles is the data memory used (either read or written)?

(b) (5 pts.) ... in what fraction of cycles is the sign extend circuit needed?

3. Assuming the single cycle datapath with the components and critical path described on the slides (mips-uarch.pdf, slide 17) as a baseline, analyze the impact of the following changes.

   (a) (10 pts.) If the ALU were made 5x faster, how much faster would the processor become? (Give a percent.)

   (b) (20 pts.) If you could double the size of the MIPS register file, causing a 100ps increase in register file read time and a 15% reduction in the number of instructions (thanks to fewer loads and stores), should you make this change? Provide quantitative support for your answer.

4. (30 pts.) A “stuck at” fault is a fabrication error where a wire is stuck at some constant value no matter what. Below, design a small MIPS function called `stuckatzero` to detect whether the `Branch` control wire is stuck at 0. Your function should take no arguments and return 1 if `Branch` is stuck at 0 and 0 if the wire is behaving properly.

   Note: The functon should respect calling conventions, and use only instructions supported by our single cycle processor (`lw, sw, beq, addi, add, slt, and, or, addu, subu,` and `slt`) plus `jr` to return from the function.