CSEE W3827

Fundamentals of Computer Systems

Homework Assignment 3

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Due October 7, 2014 at 10:10 AM

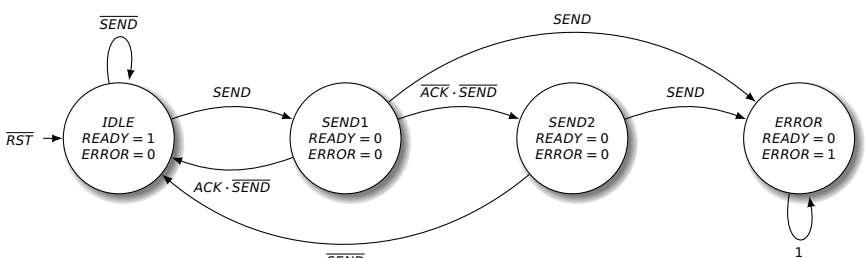
Write your name **and UNI** on your solutions

Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

1. (10 points) With a schematic, show how a positive edge triggered D flip-flop can be augmented to implement a positive edge triggered T (“toggle”) flip-flop.

   A T flip-flop has one input, T, and when T=1, the contents of the flip-flop will toggle from 0 to 1 or 1 to 0. When T=0 there is no change in the flip-flop state.

2. (35 points) Examine the state transition diagram below for a simple network send interface FSM. Upon receipt of the *SEND* input, the interface will attempt to send data for two cycles or until it receives back an *ACK*, whichever comes first. After each successful or attempted send it returns to an idle state where it awaits the next *SEND*. If a *SEND* arrives while the interface is already sending, the machine enters an error state from which the only exit is $\overline{RST}$.



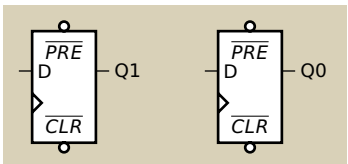
(a) (15 points) Using the state encoding given below, give expressions for this machine's output logic (*READY* and *ERROR*) and next state logic ($D1$, $D0$).

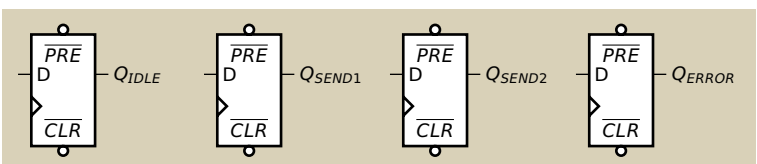
State	$Q1$	$Q0$
IDLE	0	0
*SEND*1	0	1
*SEND*2	1	0
ERROR	1	1

(b) (15 points) Using the state encoding given below, give expressions for this machine's output logic (*READY* and *ERROR*) and next state logic (D_{IDLE}, D_{SEND1}, D_{SEND2}, D_{ERROR}).

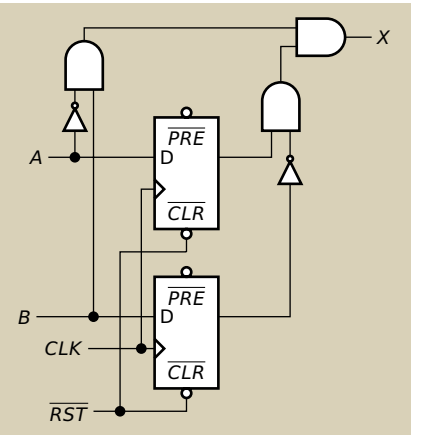
State	Q_{IDLE}	Q_{SEND1}	Q_{SEND2}	Q_{ERROR}
IDLE	1	0	0	0
*SEND*1	0	1	0	0
*SEND*2	0	0	1	0
ERROR	0	0	0	1

(c) (5 points) On the diagrams below, show how to wire up the $\overline{RST}$ signal for each of the two machines above.





3. (35 points) Examine the sequential circuit below.

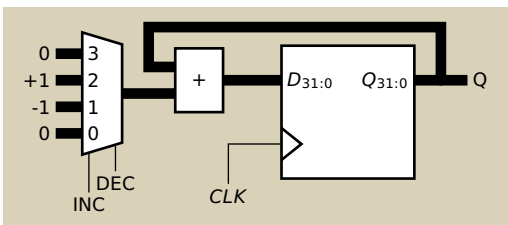


(a) (5 points) Is this a Mealy or a Moore machine?

(b) (20 points) Draw the state transition diagram for this machine.

(c) (10 points) Describe, in English, what this machine is doing.

4. (20 points) If the the up/down counter shown below is constructed using D flip-flops with a 2ns setup time, 2 ns hold time, a minimum propagation delay of 1ns, and a maximum propagation delay of 3ns, answer the following questions about the 32-bit adder used in the design.



(a) What is the smallest safe propagation delay through the adder?

(b) Assuming a 10ns clock period, what is the longest safe propagation delay through the adder?