MIDTERM REVIEW
10/10/13

- ☐ DFF timing & triggering
- ☐ 4-bit counter (FSM, Register, shifter)
- ☐ countdown circuit.
- ☐ Mealy FSM design

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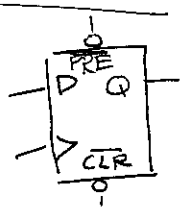
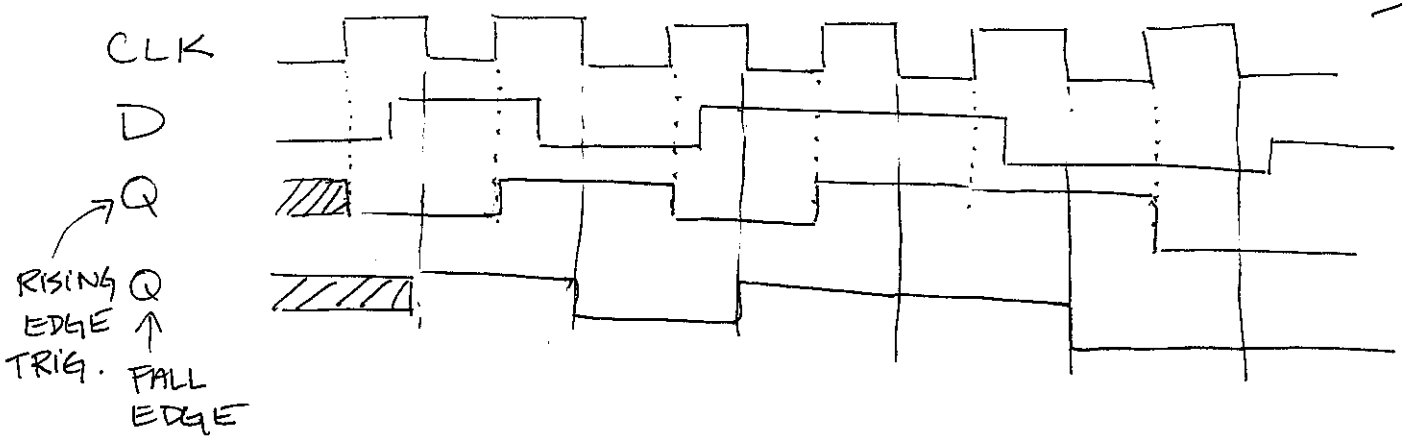
(0) DFF TIMING





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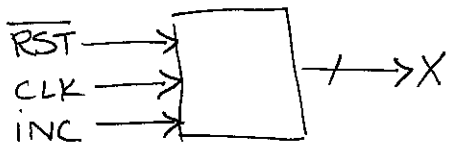
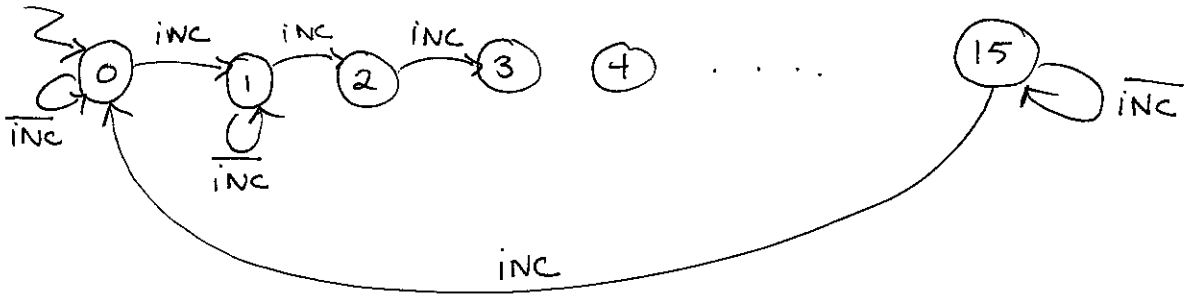
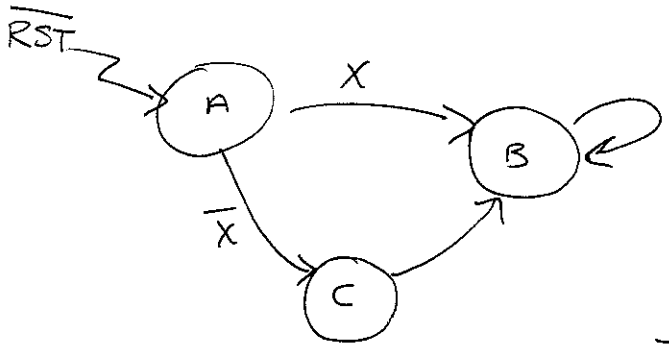
(1) 4-bit counter.



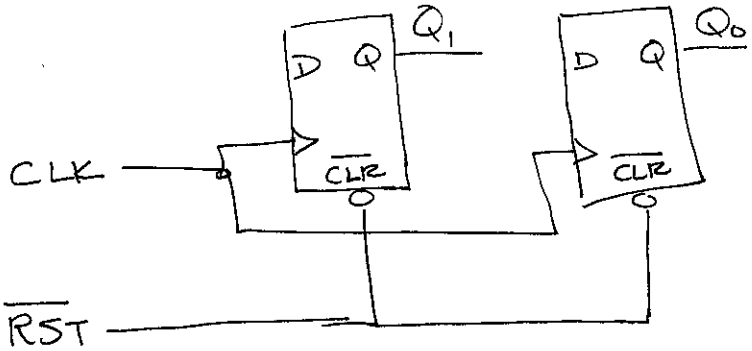
(1A)

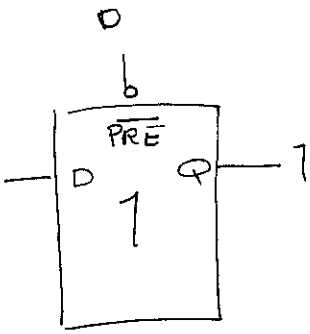


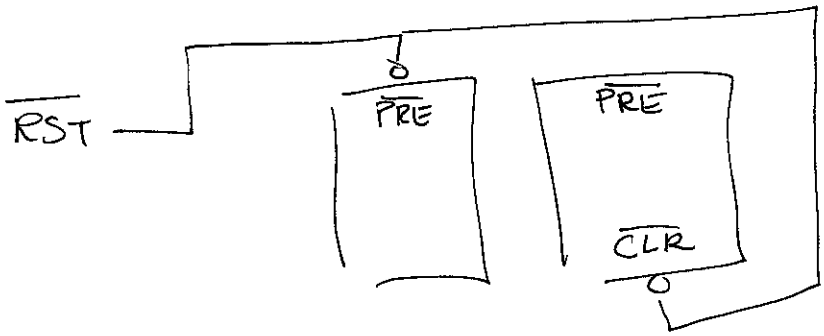
state	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
⋮			⋮	



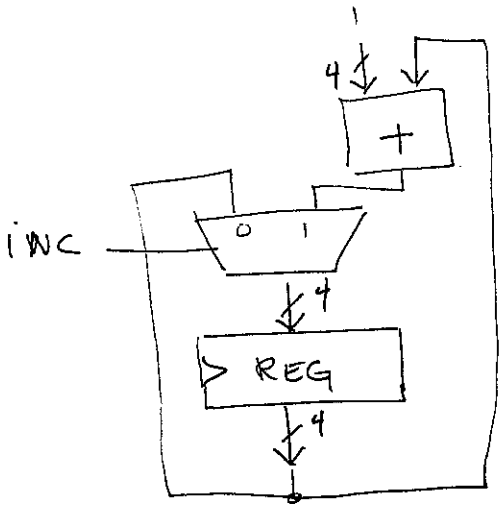
	Q_1	Q_0	Q_1	Q_0
A	0	0	1	0
B	0	1		
C	1	0		

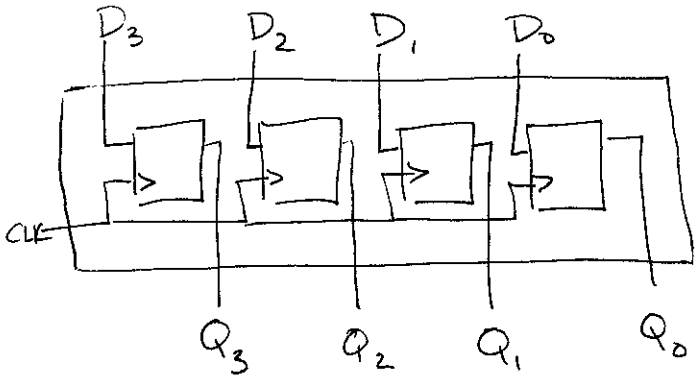




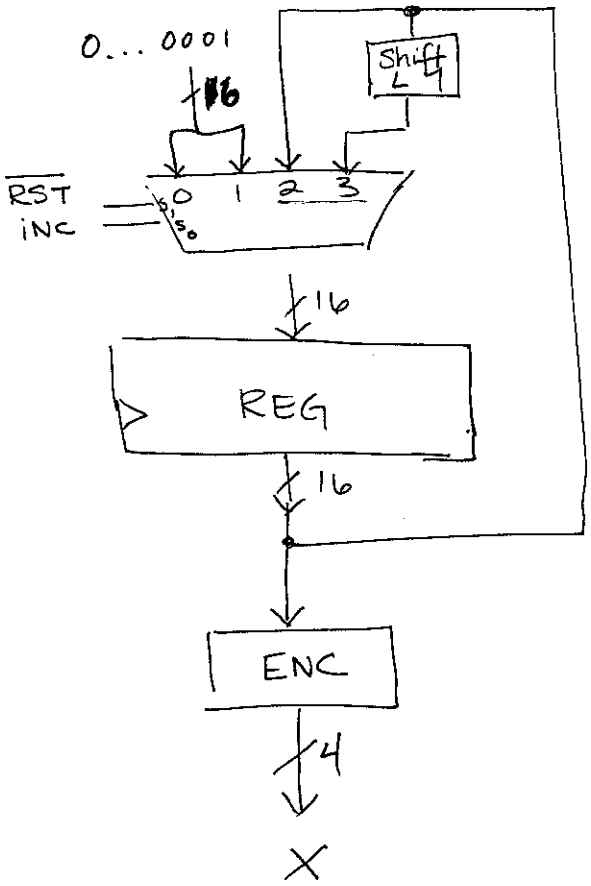


(B)


4
+
INC
0 1
4
REG
4

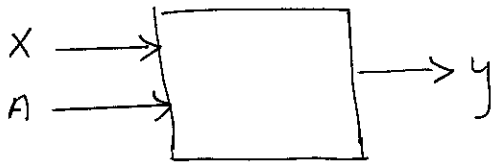

D3
D2
D1
D0
CLK
Q3
Q2
Q1
Q0

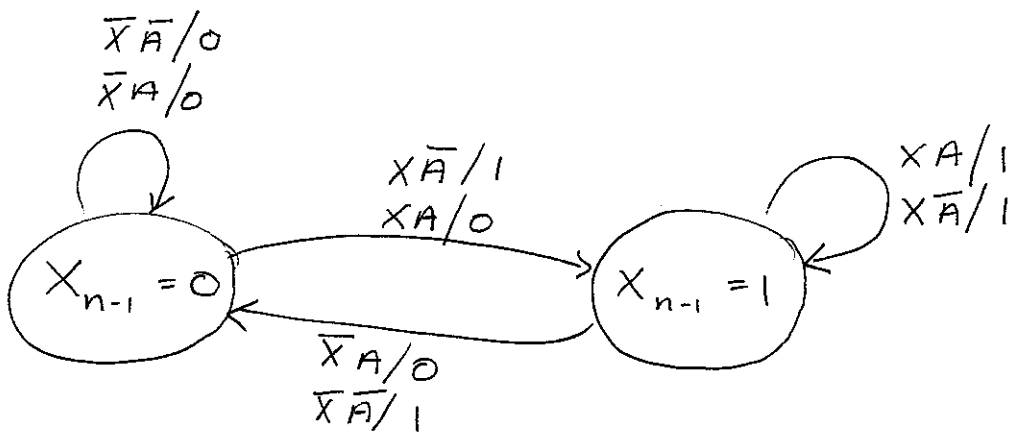
(C)


0...0001
16
Shift L 4
RST
INC
0 1 2 3
16
REG
16
ENC
4
X

(2) MEALY EXAMPLE

$$y_n = \begin{cases} A = 1: & X_n \cdot X_{n-1} \\ A = 0: & X_n + X_{n-1} \end{cases}$$





	Q
$X_{n-1} = 0$	0
$X_{n-1} = 1$	1

CURR	INPUT		NEXT	OUTPUT
Q	X	A	Q^+	y

ALT APPROACH