CSEE W3827

Fundamentals of Computer Systems

Homework Assignment 5

Prof. Martha A. Kim

Columbia University

Due December 5, 2013 at 10:10 AM

Write your name **and UNI** on your solutions

Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

1. (20 pts.) Imagine that the MIPS ISA were modified to disallow non-zero offsets in address calculations. All loads or stores of the form

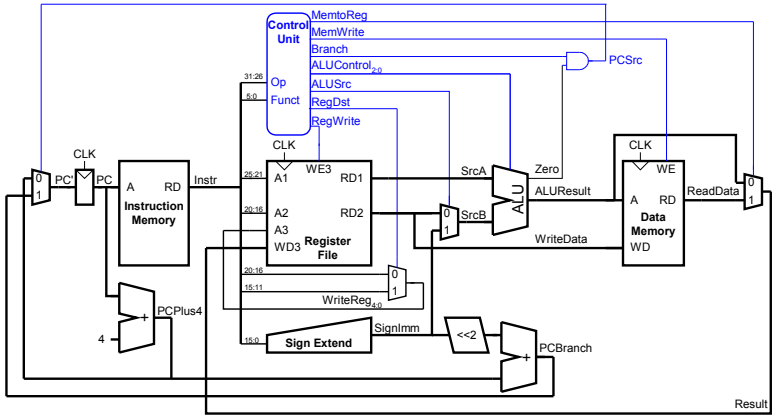
```
lw $x, a($y)
```

would need to become a two-instruction sequence such as:

```
addi $y, $y, a
lw $x, $y
```

(a) Show the modifications to the datapath and control to support this change. You should start from the implementation shown below and be sure not to change the behavior of any instructions *other than* the `lw` and `sw`.

(b) Assuming that SPECINT2000 consists of 25% loads and 10% stores, of which 40% and 50% respectively have non-zero offsets, what is percent change in SPECINT2000 execution time? You may assume no change in clock period as a result of your changes.



Inst.	OP	RegWrite	RegDst	ALUSrc	Branch	MemWrite	MemToReg	ALUOp
R-type	000000	1	1	0	0	0	0	1-
lw	100011	1	0	1	0	0	1	00
sw	101011	0	-	1	0	1	-	00
beq	000100	0	-	0	1	0	-	01

2. (15 points) Assuming the following control signals are (individually) stuck at 0, meaning they always have the value 0. For each, give an example of an instruction that would malfunction as a result.

   (a) *MemToReg*

   (b) $ALUOp_{1:0}$

   (c) *PCSrc*

3. (20 points) The table below describes the performance of two processors, A and B, and two compilers, C and D, on a standard benchmark program. Which is the best compiler-machine combination? Provide quantitative support for your choice.

		Compiler C		Compiler D	
	GHz	**Instructions**	**Avg. CPI**	**Instructions**	**Avg. CPI**
Processor A	3.4	7000	1.2	5000	1.5
Processor B	2.6	1500	2.2	1000	4.0

4. (20 points) Assuming the single-cycle processor examined in class, and the two sets of latencies shown below (processors A and B), indicate the critical path for each instruction listed below. All latencies provided are in units of picoseconds.

	I-Mem	Adder	Mux	ALU	Regfile	D-Mem	Control
Processor A	400	100	30	120	200	350	100
Processor B	500	150	100	180	220	1000	65

(a) An and instruction on processor A.

(b) A beq instruction on processor A.

(c) A sw instruction on processor B.

(d) A lw instruction on processor B.

5. (25 points) Consider the following MIPS program:

```
    addi $s0, $0, 0          # i = 0
    add $s1, $0, $0          # sum = 0
    addi $t0, $0, 10         # $t0 - 10
loop:
    slt $t1, $s0, $t0        # if (i < 10), $t1 == 1, else $t1 = 0
    beq $t1, $0, done        # if (i >= 10), branch to done
    add $s1, $s1, $s0        # sum += i
    addi $s0, $s0, 1         # i++
    j loop
done:
```

(a) How many cycles does it take to execute the following program on the multicycle MIPS processor?

(b) What is the CPI of this program?