CSEE W3827
Fundamentals of Computer Systems
Homework Assignment 2

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Due October 1, 2013 at 10:10 AM

Write your name **and UNI** on your solutions

Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

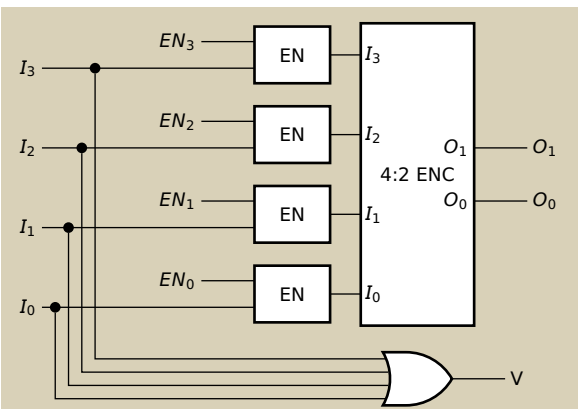
1. (10 pts.) Show how to build a 2:1 MUX using just a 3:8 DEC and an OR4 gate.

2. (10 pts.) Show how to build an AND2 using a single 2:1 MUX.

3. (20 pts.) Build an INTERLACER module that takes two 4-bit data inputs ($A_3 \ldots A_0$ and $B_3 \ldots B_0$) and a select input (S). This module should produce a single 8-bit data output ($C_7 \ldots C_0$) that interleaves the bits of A and B as follows:

   - If $S = 0$, $C_7 \ldots C_0 = A_3 B_3 \ldots A_0 B_0$
   - If $S = 1$, $C_7 \ldots C_0 = B_3 A_3 \ldots B_0 A_0$

4. (20 pts.) Complete the priority encoder below by giving expressions for EN_3, EN_2, EN_1 and EN_0.



5. (40 pts.) For this problem you will build and compare four different circuits to implement *F* using the components listed.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Component	Area	Crit. Path
2:1 MUX	7	4.5
4:1 MUX	24	8.0
8:1 MUX	57	11.5
INV	1	1.0
AND2	2	2.0
AND3	3	2.5
AND4	4	3.0
OR2	2	1.5
OR3	3	2.0
OR4	4	2.5

(a) Draw a schematic for F using only an 8:1 MUX and 1 INV.

(b) Draw a schematic for *F* using only an 4:1 MUX, 2 INV, and 1 AND2.

(c) Draw a schematic for F using only: 1 2:1 MUX, 3 INV, 1 AND3, 2 AND2, and 2 OR2.

(d) Draw a schematic for F using only: 4 INV, 1 AND4, 1 AND3, 1 AND2, 1 OR3.

(e) Compare the area and delay of the designs from parts (a) - (d) by populating the table below:

Design	Area	Crit. Path
(a)		
(b)		
(c)		
(d)		