# Joseph Zuckerman

Computer Science PhD Student

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## Education

**Columbia University** — *New York, New York*

PhD in Computer Science, NSF Graduate Research Fellow, SEAS Presidential Distinguished Fellow — *August 2019 - December 2024*

**Columbia University** — *New York, New York*

M.S. in Computer Science (4.0 GPA) — *August 2019 - April 2021*

**Harvard University** — *Cambridge, Massachusetts*

S.B. in Electrical Engineering, Magna Cum Laude with Highest Honors in Field (3.93 GPA), Phi Beta Kappa — *August 2015 - May 2019*

## Experience

**Columbia System Level Design Group** — *New York, New York*

Graduate Research Assistant (Advised by Prof. Luca Carloni) — *August 2019 - Present*

- Lead development for ESP, an open-source platform for heterogeneous system-on-chip design. Working on ESP has required knowledge in various areas of hardware (cache coherence, processor architecture, accelerator design, on-chip networks, bus protocols) and software (device drivers, operating systems, APIs), as well as familiarity with a variety of EDA tools for simulation, HLS, and FPGA synthesis. I collaborate with 10+ instutions that use ESP for their own research.
- Contributed significantly to the design, verification, and test of two 12nm, multi-core, many-accelerator SoCs
- Implemented cache hierarchy for heterogeneous SoCs in SystemVerilog and applied reinforcement learning for optimized runtime selection of accelerator cache coherence modes

**NVIDIA** — *Santa Clara, California*

ASIC Design Intern — *June - August 2019*

- Designed an interrupt aggregator for the memory subsystem of a mobile GPU SoC
- Migrated and instanced memory qualification engine in next generation chip
- Set up synthesis flows and implemented fixes for several timing violations

**Harvard Architecture, Circuits, and Compilers Group** — *Cambrige, Massachuestts*

Undergraduate Researcher (Advised by Profs. David Brooks and Gu-Yeon Wei) — *January 2018 - May 2019*

- Designed a hardware accelerator for Gibbs sampling for the Latent Dirichlet Allocation text classification application
- Adapted a Deep Neural Network Accelerator for VLSI class project

**NVIDIA** — *Austin, Texas*

Hardware Verification Intern — *June - August 2018*

- Enhanced an existing Verilog/C++ behavioral model for use in place of RTL in the development of a UVM testbench
- Wrote a detailed verification plan for these features and created a Verilog testbench to implement the plan

**NASA Jet Propulsion Laboratory** — *Pasadena, California*

Electrical Engineering Research Intern — *June - August 2017*

- Researched low-power power-supply circuits for use in a micro-mercury atomic clock
- Designed 60V and 1000V DC sources and a 400V, 1MHz RF source

**NoiseAware** — *Dallas, Texas*

Embedded Systems Engineering Intern — *June - August 2016*

- Wrote and debugged firmware for a non-invasive, smart noise monitor for short-term vacation rentals
- Developed a prototype for a new version of device and rewrote firmware for compatibility
- Added support for over-the-air firmware updates, simultaneous incoming requests, and high-latency internet service

## Talks

[1] **J. Zuckerman**, D. Giri, P. Mantovani, M. Cassel Dos Santos, K. Chiu, G. Di Guglielmo, G. Eichler, J. Kwon, L. Piccolboni, B. Seoyum, G. Tombesi, and L.P. Carloni
**System-Level Computer Architecture Research with Open ESP**
*First Workshop on Open-Source Computer Architecture Research (OSCAR), 2022.*

## Publications

[1] T. Jia, P. Mantovani, M. Cassel Dos Santos, D. Giri, **J. Zuckerman**, E.J. Loscalzo, M. Cochet, K. Swaminathan, G. Tombesi, J.J. Zhang, N. Chandramoorthy, J.D. Wellman, L.P. Carloni, K. Shepard, D. Brooks, G.Y. Wei, and P. Bose
**A 12nm Agile-Designed SoC for Swarm-Based Perception with Heterogeneous IP Blocks, a Reconfigurable Memory Hierarchy, and an 800MHz Multi-Plane NoC**
*IEEE European Solid State Circuits Conference (ESSCIRC), 2022.*

[2] **J. Zuckerman**, P. Mantovani, D. Giri, and L.P. Carloni
**Enabling Heterogeneous, Multicore SoC Research with RISC-V and ESP**
*Sixth Workshop on Computer Architecture Research with RISC-V (CARRV), 2022.*

[3] **J. Zuckerman**, D. Giri, J. Kwon, P. Mantovani, L.P. Carloni
**Cohmeleon: Learning-based Orchestration of Accelerator Coherence in Heterogeneous SoCs**
*IEEE/ACM International Symposium on Microarchitecture (MICRO-54), 2021.*

[4] P. Mantovani, D. Giri, G. Di Guglielmo, L. Piccolboni, **J. Zuckerman**, E. G. Cota, M. Petracca, C. Pilato, and L. P. Carloni
**Agile SoC Development with Open ESP**
*(invited) International Conference on Computer Aided Design (ICCAD), 2020.*

## Tutorials

[1] L. P. Carloni, G. Di Guglielmo, D. Giri, P. Mantovani, **J.Zuckerman**
**ESP: the Open-Source Research Platform for Agile SoC Design and Programming**
*International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2021.*

## Teaching

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| **CSEE 6868: Embedded Scalable Platforms**- Teaching Assistant | *Columbia University* | Spring 2022 |
| **CSEE 4868: System-on-Chip Platforms**- Teaching Assistant | *Columbia University* | Fall 2020, Fall 2021 |
| **CS141: Computing Hardware**- Teaching Fellow | *Harvard University* | Fall 2017, Spring 2019 |
| **CS50: Intro to Computer Science**- Course Assistant | *Harvard University* | Fall 2016 |

## Honors & Awards

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| **Andrew P. Kosoresow Memorial Award for Excellence in Teaching and Service** | *Columbia University* | 2022 |
| **Graduate Research Fellowship Winner** | *National Science Foundation* | 2021 |
| **Presidential Distinguished Fellowship** | *Columbia University* | 2019 |
| **Phi Beta Kappa Inductee** | *Harvard University* | 2019 |
| **Dean's Award for Outstanding Engineering Thesis: Honorable Mention** | *Harvard University* | 2019 |
| **Derek Bok Award for Distinction in Teaching** (for CS141) | *Harvard University* | 2017, 2019 |
| **John Harvard Scholar** (top 5% of class) | *Harvard University* | 2017 |

## Technical Skills

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| **Languages** | Assembly, Bash, C, C++, Java, Python, LaTeX, OCaml, SystemC, SystemVerilog, Verilog, VHDL |
| **Tools** | Cadence Incisive and Stratus HLS, Git, Mentor Modelsim, Wolfram Mathematica, Xilinx Vivado |

## Relevant Coursework

Artificial Intelligence, Compilers, Computer Architecture, Data Structures and Algorithms, Digital Design, Formal Verification, Hardware Security, Machine Learning, Microelectronic Devices and Circuits, Natural Language Processing, Operating Systems, Programming Languages, Signals and Systems, Quantum Computing, System-on-Chip Platforms, Systems Programming, VLSI