# Joseph Zuckerman

Computer Science PhD Candidate

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## Education

**Columbia University** — *New York, New York*

PhD in Computer Science, NSF Graduate Research Fellow, SEAS Presidential Distinguished Fellow — *August 2019 - May 2025*

**Columbia University** — *New York, New York*

M.S. in Computer Science (4.0 GPA) — *August 2019 - April 2021*

**Harvard University** — *Cambridge, Massachusetts*

S.B. in Electrical Engineering, Magna Cum Laude with Highest Honors in Field (3.93 GPA), Phi Beta Kappa — *August 2015 - May 2019*

## Experience

**IBM Research** — *Yorktown Heights, New York*

Student Researcher — *August 2022 - Present*

- System-level architecture and RTL development for a product-targeted SoC
- Produced the RTL and worked closely with a physical design team for a demonstration SoC in an advanced technology

**Columbia System Level Design Group** — *New York, New York*

Graduate Research Assistant (Advised by Prof. Luca Carloni) — *August 2019 - Present*

- Lead development for ESP, an open-source platform for heterogeneous system-on-chip design. This requires knowledge in various areas of hardware (cache coherence, processor and accelerator design, on-chip networks, bus protocols) and software (device drivers, operating systems, APIs); familiarity with a variety of EDA tools for simulation, HLS, FPGA synthesis; and a basic understanding of ASIC design. I oversee various development efforts for ESP, maintain its open-source release on GitHub, and collaborate with 10+ institutions that use ESP for their own research.
- Contributed significantly to the design, verification, and test of two 12nm, multi-core, many-accelerator SoCs
- Implemented cache hierarchy for heterogeneous SoCs in SystemVerilog and applied reinforcement learning for optimized runtime selection of accelerator cache coherence modes

**NVIDIA** — *Santa Clara, California*

ASIC Design Intern — *June - August 2019*

- Designed an interrupt aggregator for the memory subsystem of a mobile GPU SoC
- Migrated and instanced memory qualification engine in next generation chip
- Set up synthesis flows and implemented fixes for several timing violations

**Harvard Architecture, Circuits, and Compilers Group** — *Cambrige, Massachuestts*

Undergraduate Researcher (Advised by Profs. David Brooks and Gu-Yeon Wei) — *January 2018 - May 2019*

- Designed a hardware accelerator for Gibbs sampling for the Latent Dirichlet Allocation text classification application
- Adapted a Deep Neural Network Accelerator for VLSI class project

**NVIDIA** — *Austin, Texas*

Hardware Verification Intern — *June - August 2018*

- Enhanced an existing Verilog/C++ behavioral model for use in place of RTL in the development of a UVM testbench
- Wrote a detailed verification plan for these features and created a Verilog testbench to implement the plan

**NASA Jet Propulsion Laboratory** — *Pasadena, California*

Electrical Engineering Research Intern — *June - August 2017*

- Researched low-power power-supply circuits for use in a micro-mercury atomic clock

**NoiseAware** — *Dallas, Texas*

Embedded Systems Engineering Intern — *June - August 2016*

- Wrote and debugged firmware for a non-invasive, smart noise monitor for short-term vacation rentals
- Developed a prototype for a new version of device and rewrote firmware for compatibility
- Added support for over-the-air firmware updates, simultaneous incoming requests, and high-latency internet service

## Technical Skills

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|---|---|
| **Hardware** | SystemC, SystemVerilog, Verilog, VHDL |
| **Software** | C, Python |
| **EDA Tools** | Cadence Xcelium and Stratus HLS, Mentor Modelsim and Catapult HLS, Xilinx Vivado |
| **Other** | Bash, Git, LaTeX, Make, Wolfram Mathematica |

## Honors & Awards

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| **Andrew P. Kosoresow Memorial Award for Excellence in Teaching and Service** | *Columbia University* | 2022 |
| **Graduate Research Fellowship Winner** | *National Science Foundation* | 2021 |
| **Presidential Distinguished Fellowship** | *Columbia University* | 2019 |
| **Phi Beta Kappa Inductee** | *Harvard University* | 2019 |
| **Dean's Award for Outstanding Engineering Thesis: Honorable Mention** | *Harvard University* | 2019 |
| **Derek Bok Award for Distinction in Teaching** (for CS141) | *Harvard University* | 2017, 2019 |
| **John Harvard Scholar** (top 5% of class) | *Harvard University* | 2017 |

## Teaching

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| **CSEE 6868: Embedded Scalable Platforms**- Teaching Assistant | *Columbia University* | Spring 2022, 2023, 2024, 2025 |
| **COMS 6901: Projects in Computer Science**- Project Mentor | *Columbia University* | Fall 2022 - Fall 2024 |
| **CSEE 4868: System-on-Chip Platforms**- Teaching Assistant | *Columbia University* | Fall 2020, 2021 |
| **CS141: Computing Hardware**- Teaching Fellow | *Harvard University* | Fall 2017, Spring 2019 |
| **CS50: Intro to Computer Science**- Course Assistant | *Harvard University* | Fall 2016 |

## Publications

[1] M. Cochet, K. Swaminathan, E. J. Loscalzo, **J. Zuckerman**, M. Cassel dos Santos, D. Giri, A. Buyuktosunoglu, T. Jia, D. Brooks, G.-Y. Wei, K. Shepard, L. P. Carloni, P. Bose
**BlitzCoin: A Decentralized Hardware Solution for Power Management of Highly-Heterogeneous SoCs**
*IEEE Micro Special Issue on Top Picks From the 2024 Computer Architecture Conferences, Vol. 45, No. 3, July/August 2025.*

[2] G. Eichler, **J. Zuckerman**, L.P. Carloni
**An Energy-Efficient Kalman Filter Architecture with Tunable Accuracy for Brain-Computer Interfaces**
*The Proceedings of the Design Automation Conference (DAC), 2025.*

[3] G. Eichler, **J. Zuckerman**, L.P. Carloni
**KalmMind: A Configurable Kalman Filter Design Framework for Embedded Brain-Computer Interfaces**
*The Proceedings of the Conference on Design, Automation, and Test in Europe (DATE), 2025.*

[4] V. Suresh, B. Mishra, Z. Zhu, Y. Jing, N. Jin, C. Block, P. Mantovani, D. Giri, **J. Zuckerman**, L.P. Carloni, S. Adve
**Mozart: Taming Taxes and Composing Accelerators with Shared-Memory**
*International Conference on Parallel Architectures and Compilation Techniques (PACT), 2024.*

[5] **J. Zuckerman**, J.-D. Wellman, A. Vanamali, M. Shankar, G. Tombesi. K. Swaminathan, K. Lee, M. Kapur, R. Philhower, P. Bose, L.P. Carloni
**Towards Generalized On-Chip Communication for Programmable Accelerators in Heterogeneous Architectures**
*Workshop on Domain-Specific System Architecture (DOSSA), 2024.*

[6] M. Cochet, K. Swaminathan, E. J. Loscalzo, **J. Zuckerman**, M. Cassel dos Santos, D. Giri, A. Buyuktosunoglu, T. Jia, D. Brooks, G.-Y. Wei, K. Shepard, L. P. Carloni, P. Bose
**BlitzCoin: Fully Decentralized Hardware Power Management for Accelerator-Rich SoCs**
*International Symposium on Computer Architecture (ISCA), 2024.*

[7] E. Loscalzo, M. Cochet, **J. Zuckerman**, S. Zaliasl, M. Lekas, S. Cahill, T. Jia, K. Swaminathan, M. Cassel dos Santos, D. Giri, H. Sadeghi, J. Meyer, N. Sturcken, D. Brooks, G.-Y. Wei, L. Carloni, P. Bose, K. Shepard
**A 400-ns-Settling-Time Hybrid Dynamic Voltage Frequency Scaling Architecture and Its Application in a 22-Core Network-on-Chip SoC in 12-nm FinFET Technology**
*Symposium on VLSI Technology and Circuits (VLSI), 2024.*

[8] M. Cassel Dos Santos*, T. Jia*, **J. Zuckerman***, M. Cochet*, D. Giri, E.J. Loscalzo, K. Swaminathan, T. Thambe, J. J. Zhang, A. Buyuktosunoglu, K.L. Chiu, G. Di Guglielmo, P. Mantovani, L. Piccolboni, G. Tombesi, D. Trilla, J.D. Wellman, E.Y. Yang, A. Amarnath, Y. Jing, B. Mishra, V. Suresh, S. Adve, P. Bose, D. Brooks, L.P. Carloni, K.L. Shepard, and G.Y. Wei
**A 12nm Linux-SMP-Capable RISC-V SoC with 14 Accelerator Types, Distributed Hardware Power Management and Flexible NoC-Based Data Orchestration**
*International Solid State Circuits Conference (ISSCC), 2024.* ***Equally Credited Authors**

[9] G. Tombesi, **J. Zuckerman**, P. Mantovani, D. Giri, M. Cassel dos Santos, T. Jia, D. Brooks, G.Y. Wei, L.P. Carloni
**SoCProbe: Compositional Post-Silicon Validation of Heterogeneous NoC-Based SoCs**
*International Symposium on Networks-on-Chip (NOCS 2023)* ***[Best Paper Award]****. Published in IEEE Design and Test.*

[10] F. Gao, T.J. Chang, A. Li, M. Orenes-Vera, D. Giri, P. Jackson, A. Ning, G. Tziantzioulis, **J. Zuckerman**, J. Tu, K. Xu, G. Chirkov, G. Tombesi J. Balkind, M. Martonosi, L.P. Carloni, D. Wentzlaff
**DECADES: A 67mm2, 1.46TOPS, 55 Giga Cache-Coherent 64-bit RISC-V Instructions per second, Heterogeneous Many-core SoC with 109 Tiles including Accelerators, Intelligent Storage, and eFPGA in 12nm FinFET**
*Custom Integrated Circuits Conference (CICC), 2023.*

[11] T. Tambe, J. Zhang, C. Hooper, T. Jia, P. N. Whatmough, **J. Zuckerman**, M. Cassel dos Santos, D. Giri, E.J. Loscalzo, K. Shepard, L.P. Carloni, A. Rush, D. Brooks, and G.Y. Wei
**A 12nm 18.1TFLOPs/W Sparse Transformer Processor with Entropy-Based Early Exit, Mixed-Precision Predication and Fine-Grained Power Management**
*International Solid-State Circuits Conference (ISSCC), 2023.*

[12] M. Cassel Dos Santos, T. Jia, M. Cochet, K. Swaminathan, **J. Zuckerman**, P. Mantovani, D. Giri, J.J. Zhang, E.J. Loscalzo, G. Tombesi, K. Tien, N. Chandramoorthy, J.D. Wellman, D. Brooks, G.Y. Wei, K. Shepard, L.P. Carloni, and P. Bose
**A Scalable Methodology for Agile Chip Development with Open-Source Hardware Components**
*(invited) International Conference on Computer-Aided Design (ICCAD), 2022.*

[13] T. Jia, P. Mantovani, M. Cassel Dos Santos, D. Giri, **J. Zuckerman**, E.J. Loscalzo, M. Cochet, K. Swaminathan, G. Tombesi, J.J. Zhang, N. Chandramoorthy, J.D. Wellman, K. Tien, L.P. Carloni, K. Shepard, D. Brooks, G.Y. Wei, and P. Bose
**A 12nm Agile-Designed SoC for Swarm-Based Perception with Heterogeneous IP Blocks, a Reconfigurable Memory Hierarchy, and an 800MHz Multi-Plane NoC**
*IEEE European Solid State Circuits Conference (ESSCIRC), 2022.*

[14] **J. Zuckerman**, P. Mantovani, D. Giri, and L.P. Carloni
**Enabling Heterogeneous, Multicore SoC Research with RISC-V and ESP**
*Sixth Workshop on Computer Architecture Research with RISC-V (CARRV), 2022.*

[15] **J. Zuckerman**, D. Giri, J. Kwon, P. Mantovani, L.P. Carloni
**Cohmeleon: Learning-based Orchestration of Accelerator Coherence in Heterogeneous SoCs**
*IEEE/ACM International Symposium on Microarchitecture (MICRO-54), 2021.*

[16] P. Mantovani, D. Giri, G. Di Guglielmo, L. Piccolboni, **J. Zuckerman**, E. G. Cota, M. Petracca, C. Pilato, and L. P. Carloni
**Agile SoC Development with Open ESP**
*(invited) International Conference on Computer Aided Design (ICCAD), 2020.*

## Talks

[1] **J. Zuckerman**
**Democratizing System-on-Chip Research with Open ESP**
*UIUC Coordinated Science Laboratory Student Conference (Invited talk), February 2024.*

[2] **J. Zuckerman**
**Reconfigurable Data Orchestration for Scalable Silicon Systems**
*PhD Thesis Proposal, February 2024.*

[3] K. Y. Jiang, **J. Zuckerman**, L.P. Carloni
**Pipelining an Open-Source Last-Level Cache**
*Second Workshop on Open-Source Computer Architecture Research (OSCAR), June 2023.*

[4] **J. Zuckerman**
**Reconfigurability in Modern Computing Architectures**
*PhD Candidacy Exam, October 2022.*

[5] **J. Zuckerman**
**Agile Design, Optimization, and Test of Domain-Specific Systems-on-Chip**
*7th Workshop on the Future of Computer Architectures, IBM Research, October 2022.*

[6] **J. Zuckerman**, D. Giri, P. Mantovani, M. Cassel Dos Santos, K. Chiu, G. Di Guglielmo, G. Eichler, J. Kwon, L. Piccolboni, B. Seoyum, G. Tombesi, and L.P. Carloni
**System-Level Computer Architecture Research with Open ESP**
*First Workshop on Open-Source Computer Architecture Research (OSCAR), June 2022.*

## Relevant Coursework

Artificial Intelligence, Compilers, Computer Architecture, Data Structures and Algorithms, Digital Design, Formal Verification, Hardware Security, Machine Learning, Microelectronic Devices and Circuits, Natural Language Processing, Operating Systems, Programming Languages, Signals and Systems, Quantum Computing, System-on-Chip Platforms, Systems Programming, VLSI

## Tutorials

[1] L.P. Carloni, K.-L. Chiu, B. Seyoum, **J.Zuckerman**
**The ESP Approach to Agile Chip Design**
*International Symposium on Computer Architecture (ISCA), 2024.*

[2] L.P. Carloni, B. Seyoum, G. Tombesi, **J.Zuckerman**
**Design, Programming, and Partial Reconfiguration of Heterogeneous SoCs with ESP**
*Design, Automation and Test in Europe Conference (DATE), 2023.*

[3] L.P. Carloni, M. Cassel dos Santos, K.L. Chiu, G. Eichler, B. Seyoum, G. Tombesi, **J.Zuckerman**
**Design of Heterogeneous SoCs for ASIC and FPGA Targets with ESP**
*International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2023.*

[4] L. P. Carloni, R. Klein, S. Nemawarkar, S. Praveen, **J.Zuckerman**
**Hardware/Software Co-design with High-Level Synthesis**
*Design Automation Conference (DAC-59), 2022.*

[5] L. P. Carloni, G. Di Guglielmo, D. Giri, P. Mantovani, **J.Zuckerman**
**ESP: The Open-Source Research Platform for Agile SoC Design and Programming**
*International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2021.*