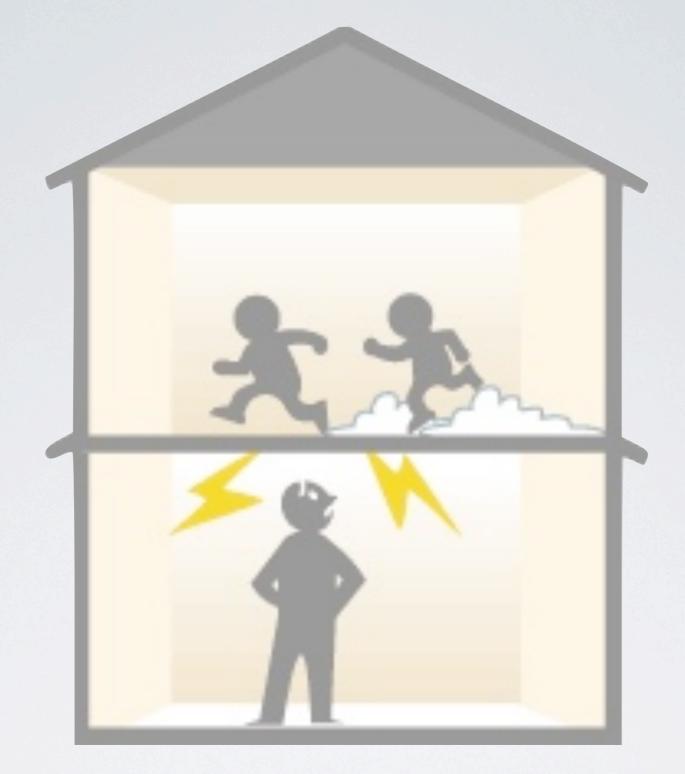
### Side-channel Vulnerability Factor: A Metric for Measuring Information Leakage

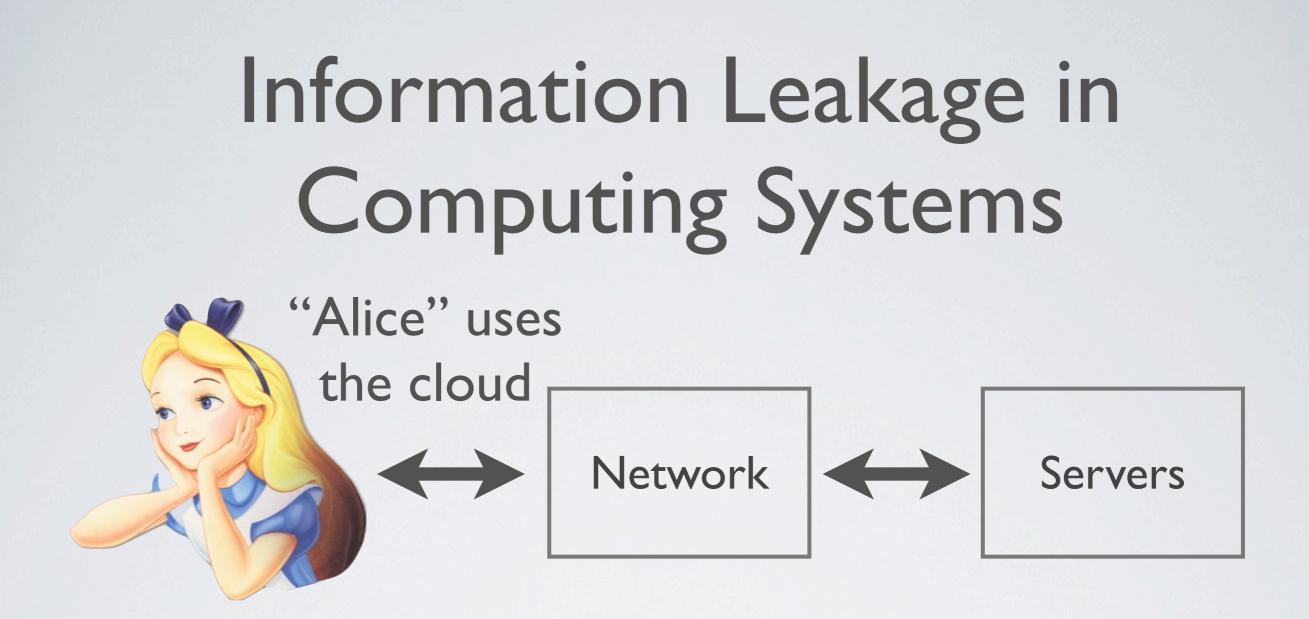
John Demme, Robert Martin, Adam Waksman, and Simha Sethumadhavan

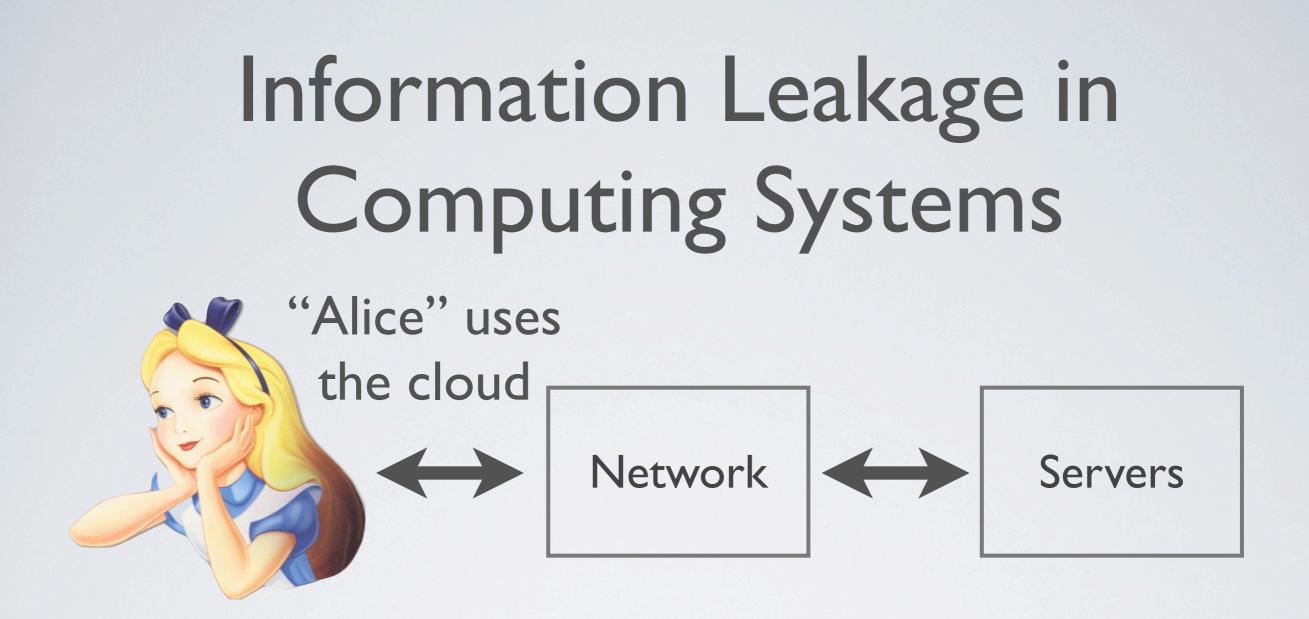
Computer Architecture and Security Technologies Lab Columbia University

# Information Leakage

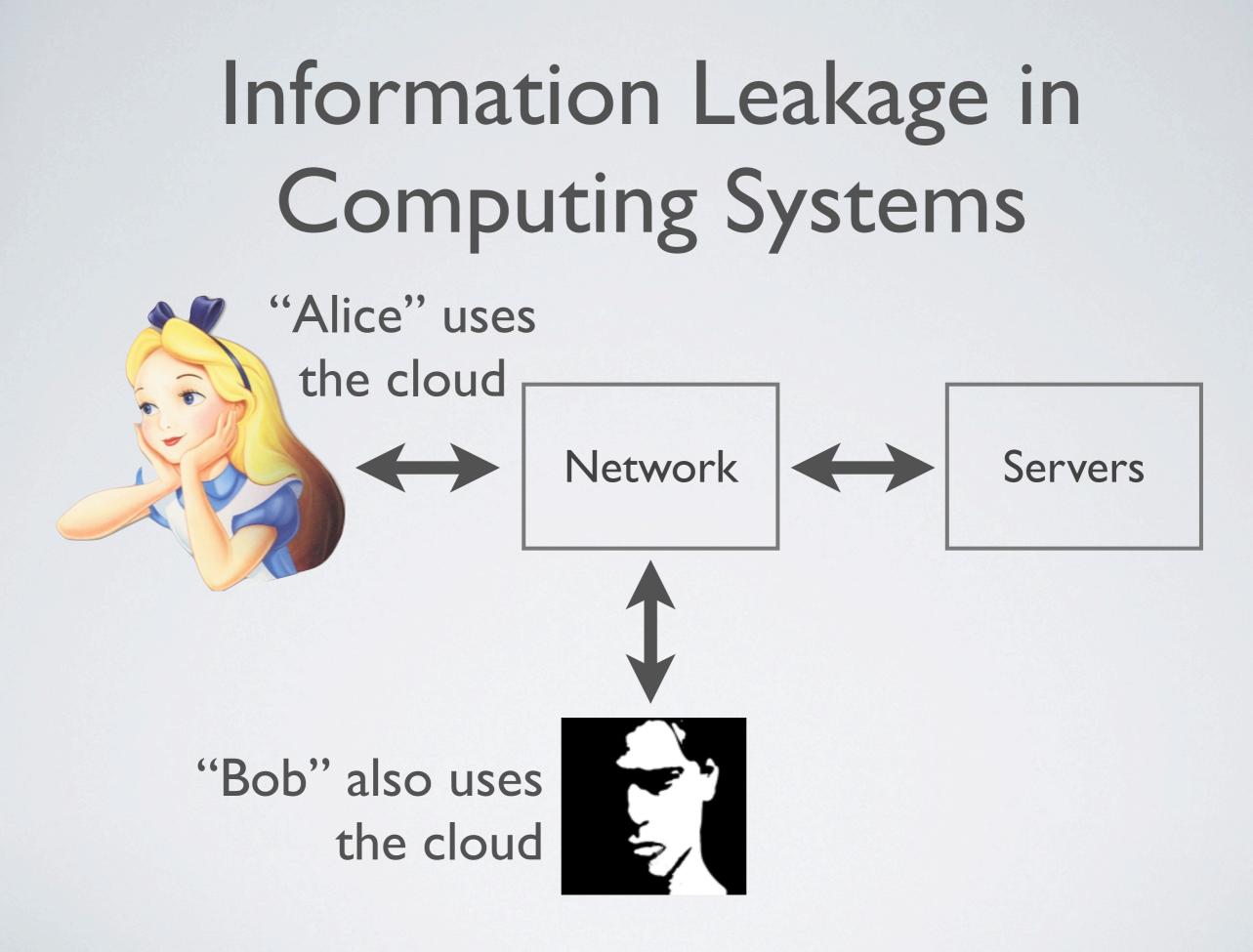


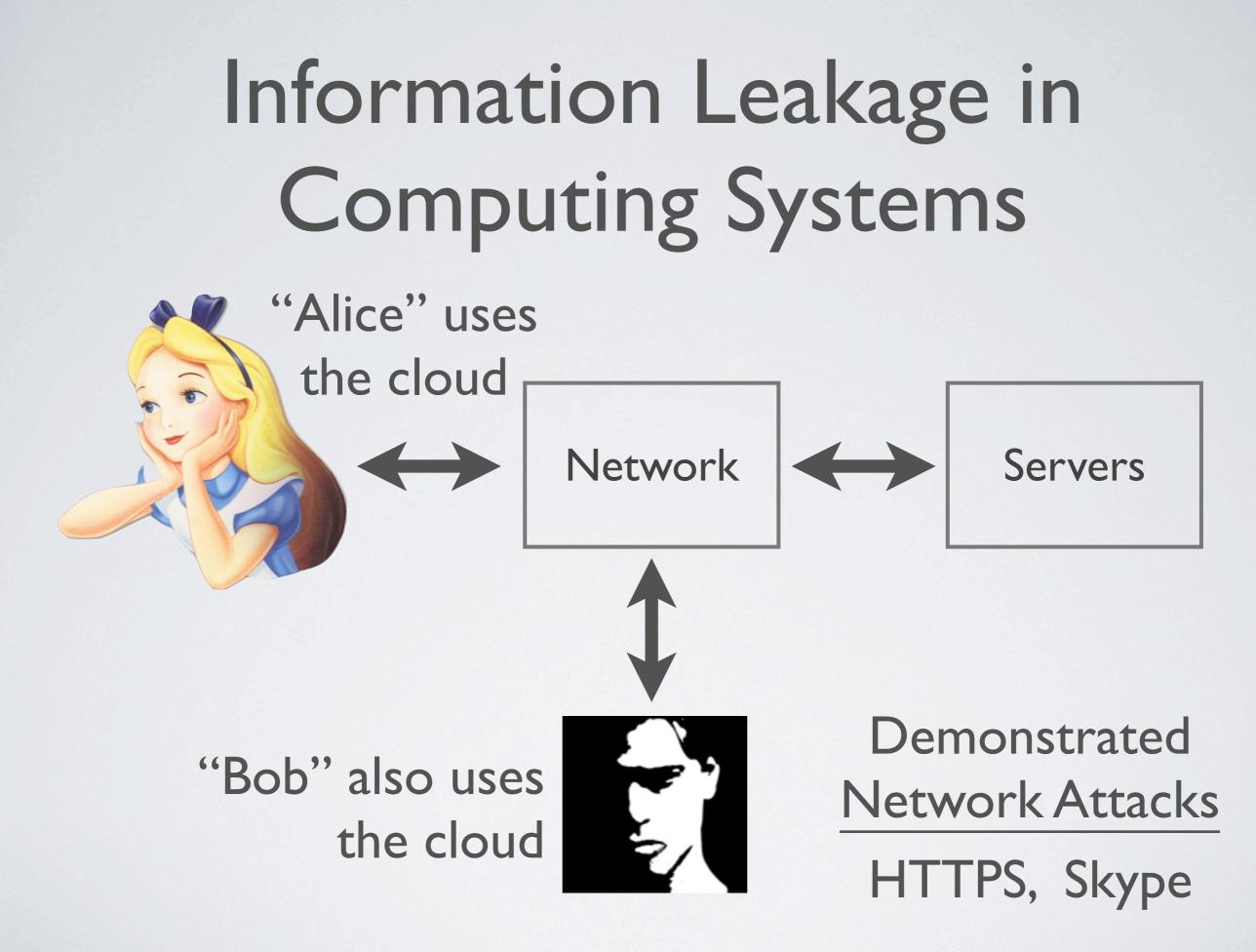
# Information Leakage

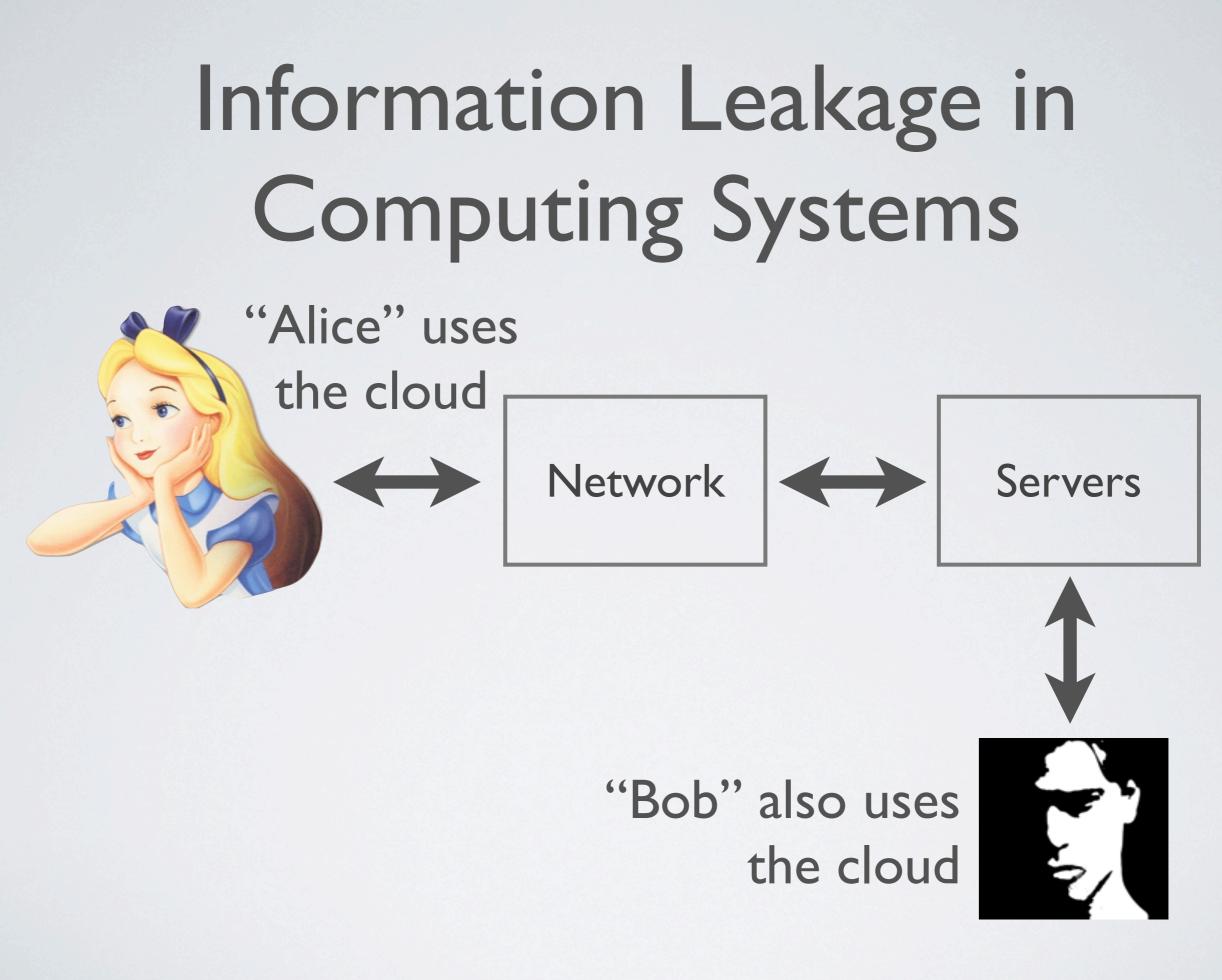


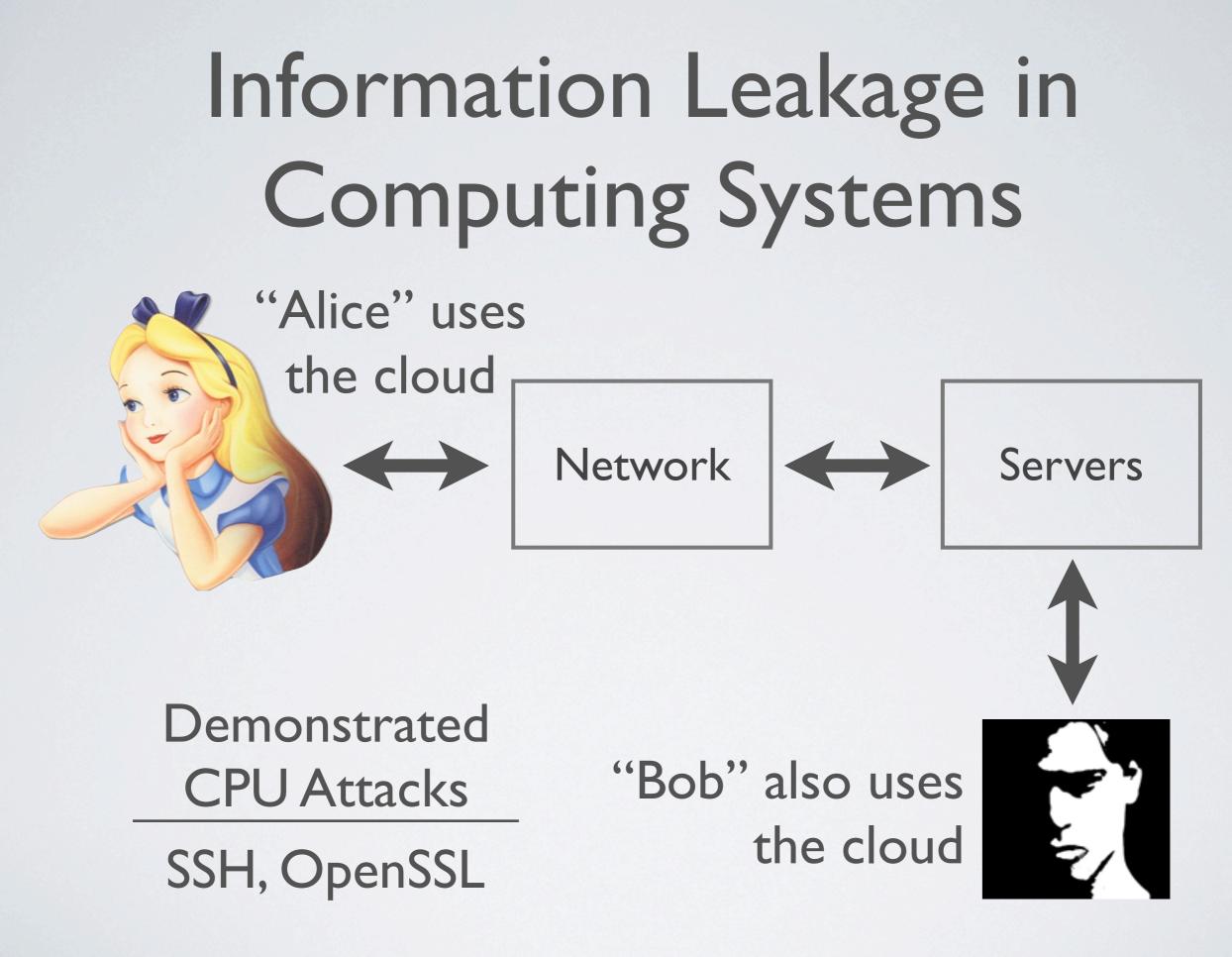


# Information leakage can create side channels









# **Big Problem**

### Side channels are unquantified.

### Therefore, they are dangerous.

## Contributions: a Quantitative Approach

## Contributions: a Quantitative Approach

Given systems S1, S2:

Security (S<sub>1</sub>) > Security(S<sub>2</sub>) ?

## Contributions: a Quantitative Approach

Given systems S1, S2:

Security (S<sub>1</sub>) > Security(S<sub>2</sub>) ?

Allows performance-security tradeoffs

## Outline

Side-channels101

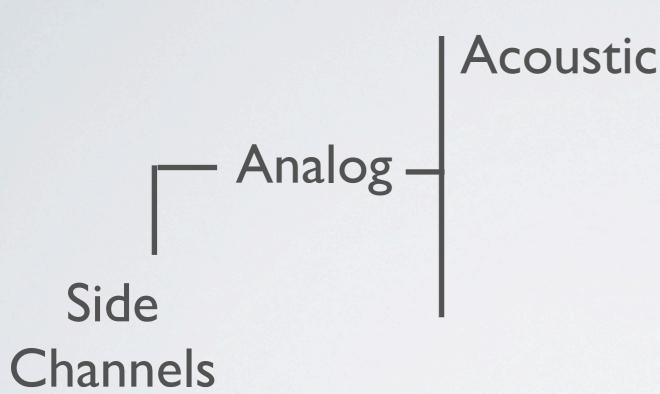
Measuring Side-channels

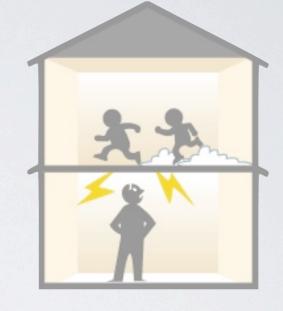
Cache systems: a case study

• Future work

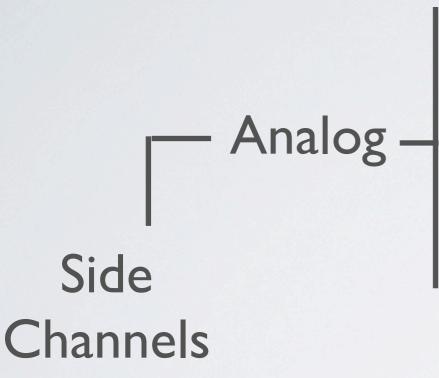
Side Channels

### Analog Side Channels



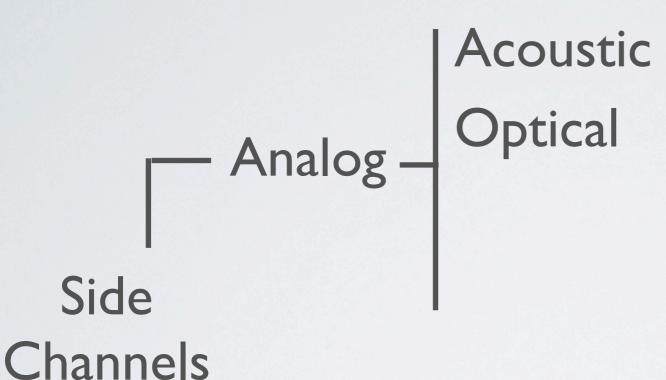


Acoustic



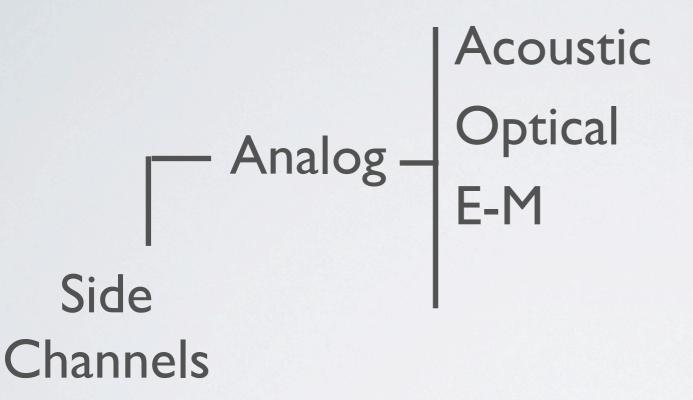


[Asonov et al. 2004] [Backes et al. 2010]

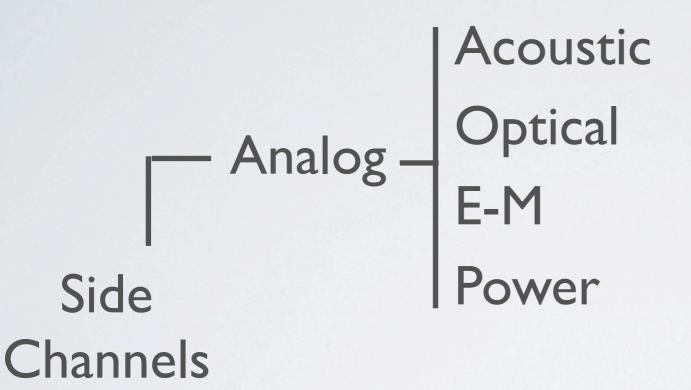




[Loughry et al. 2002]

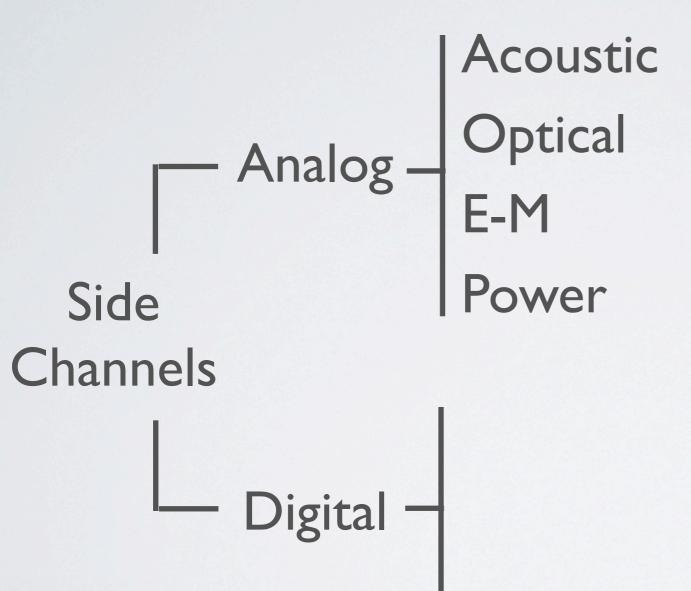


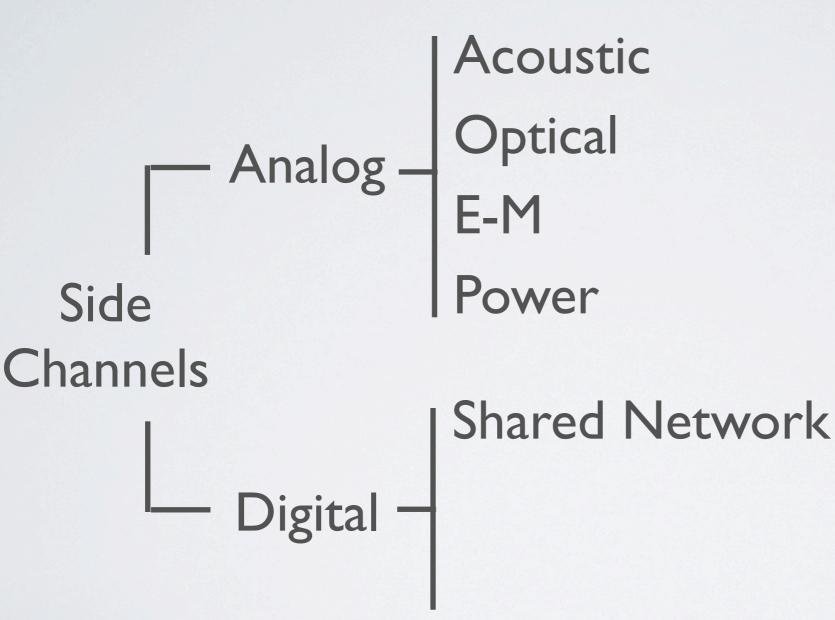






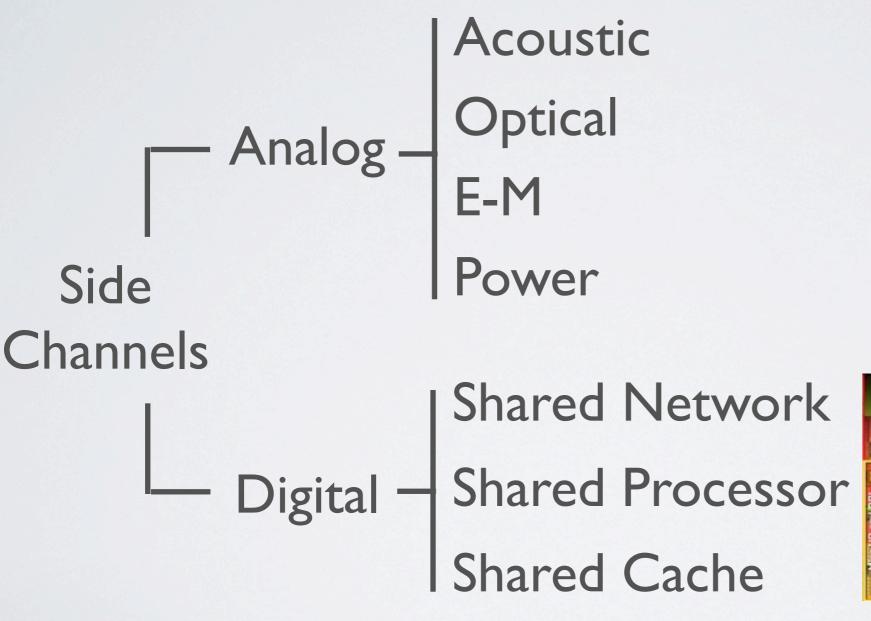
[Messerges et al. 1999]

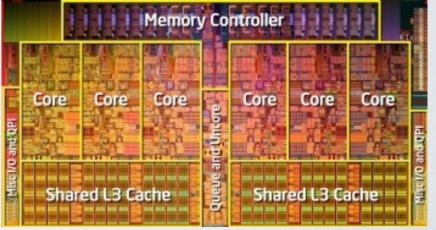




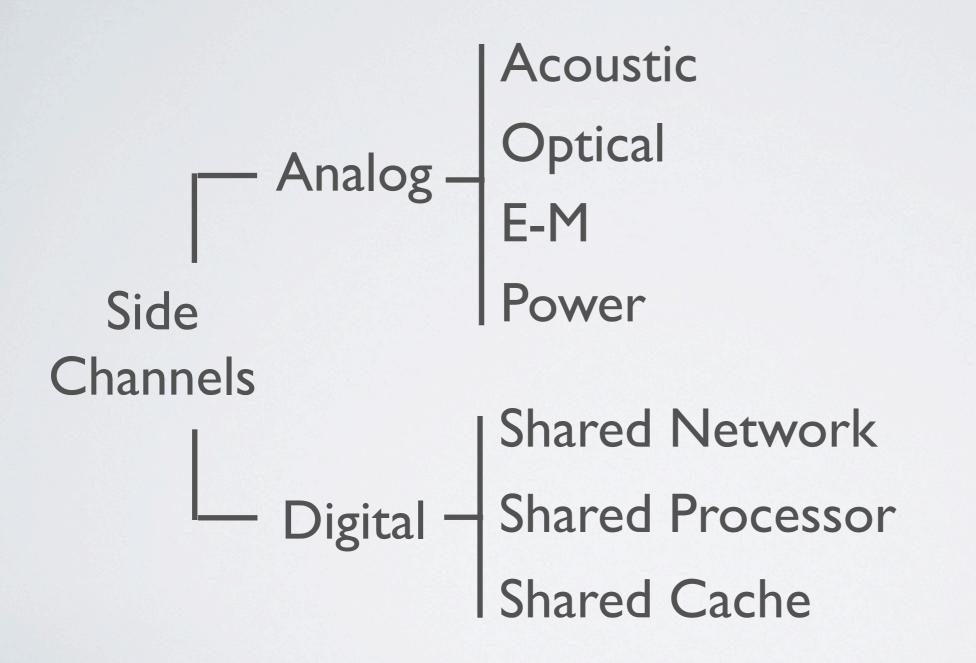


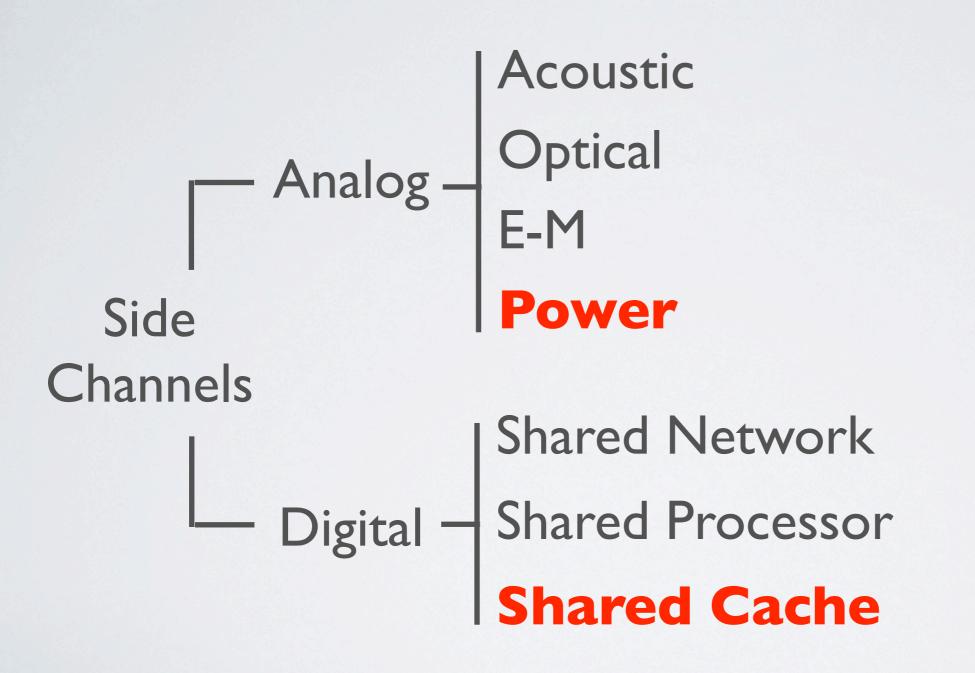
[Chen et al. 1999]





[Gullasch et al. 1999]





# **Power Side Channels**

#### Power usage during RSA encryption operation

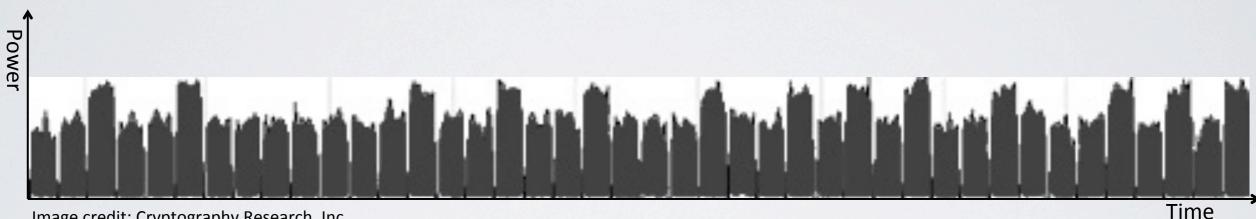


Image credit: Cryptography Research, Inc

#### Power spikes for periods at seemingly random points

# Power Side Channels

Power usage during RSA encryption operation

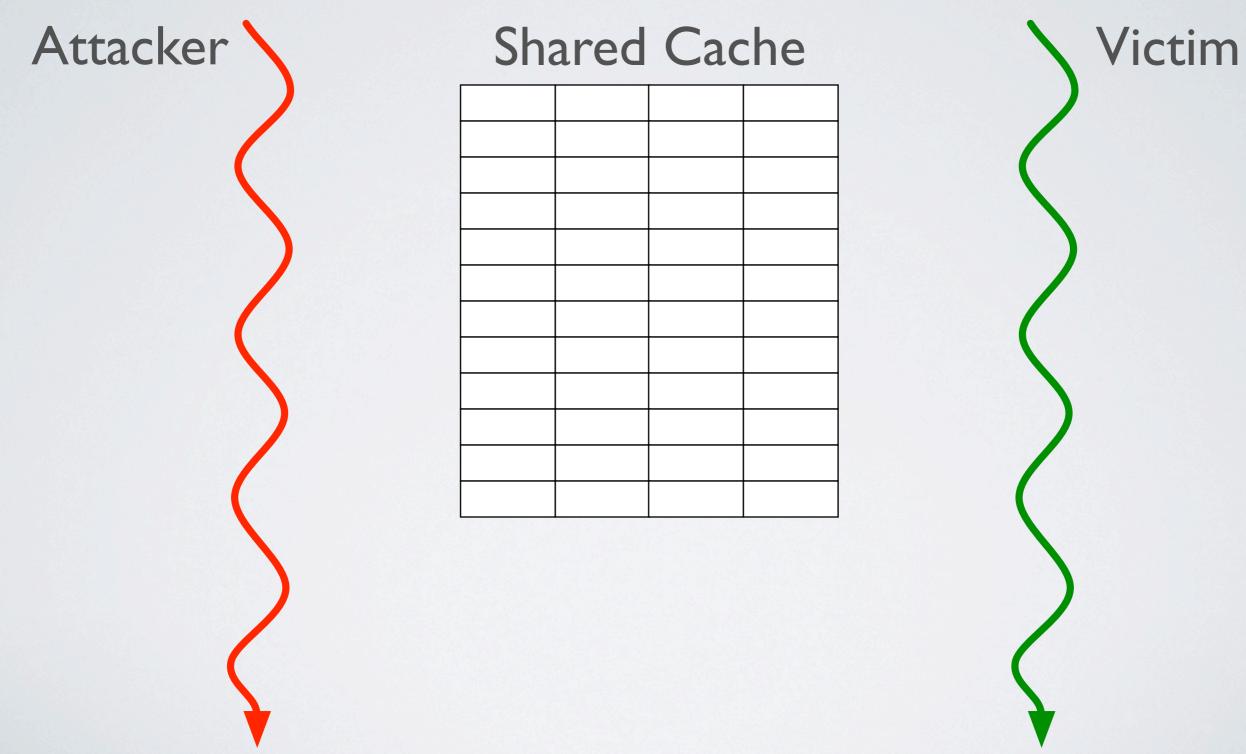


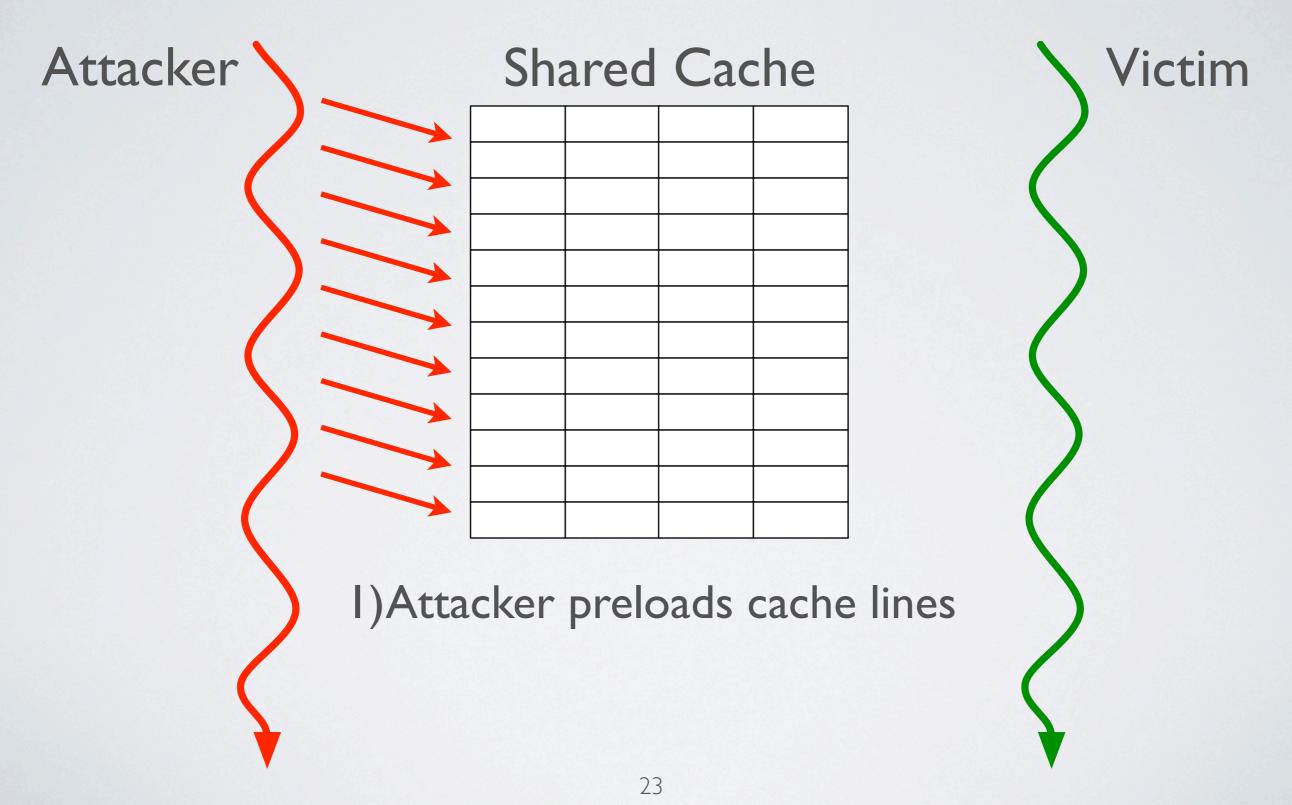
# Power Side Channels

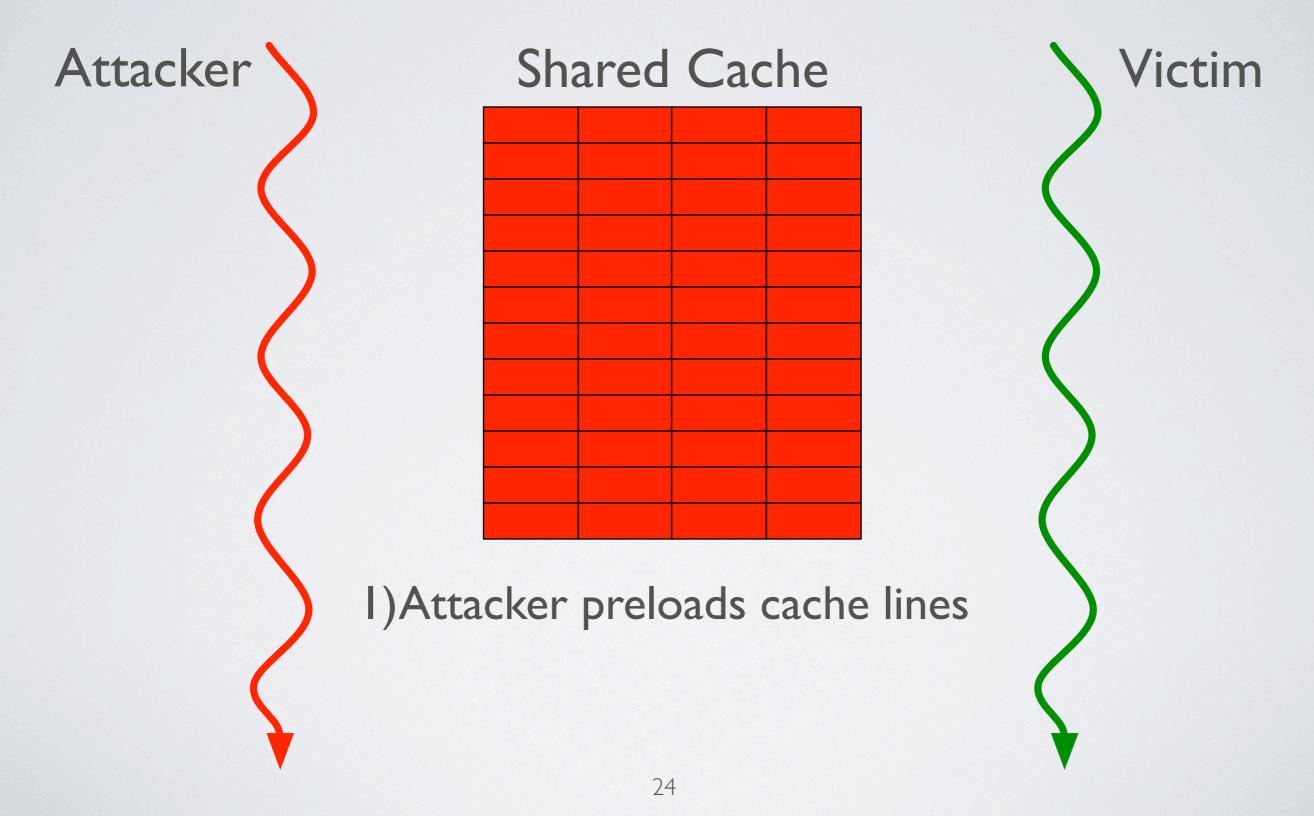
Power usage during RSA encryption operation

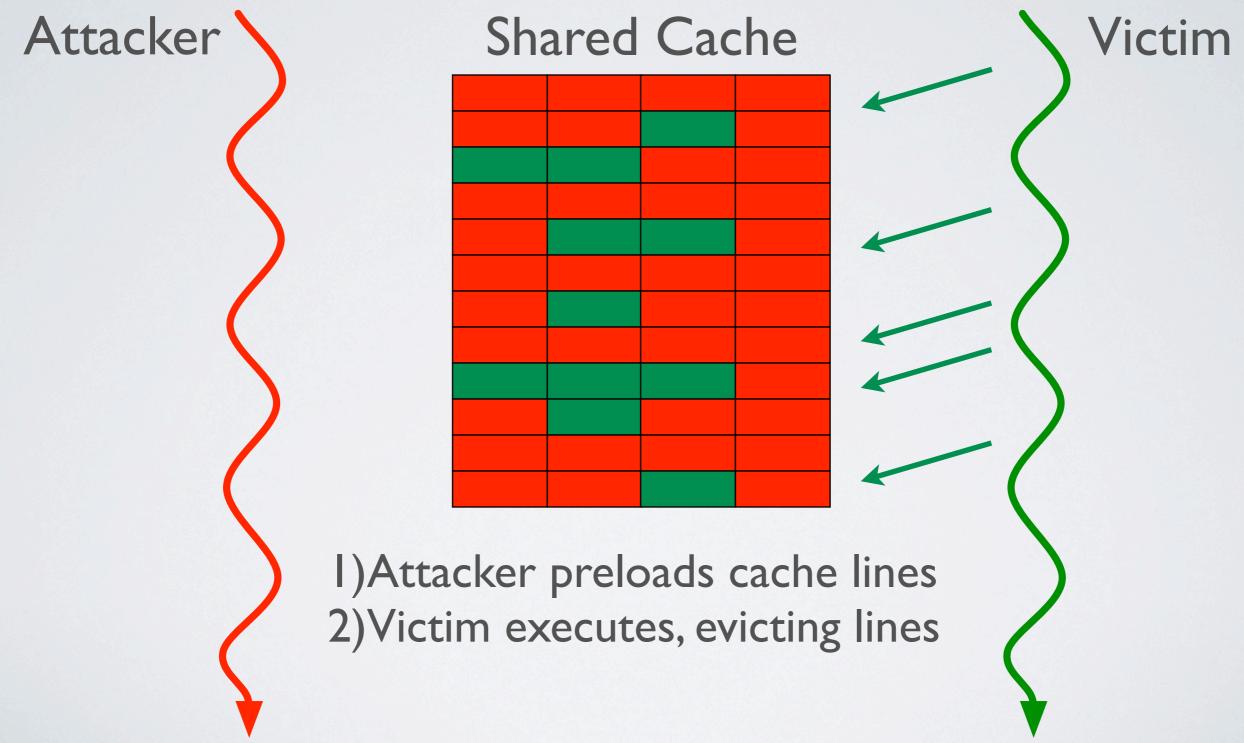


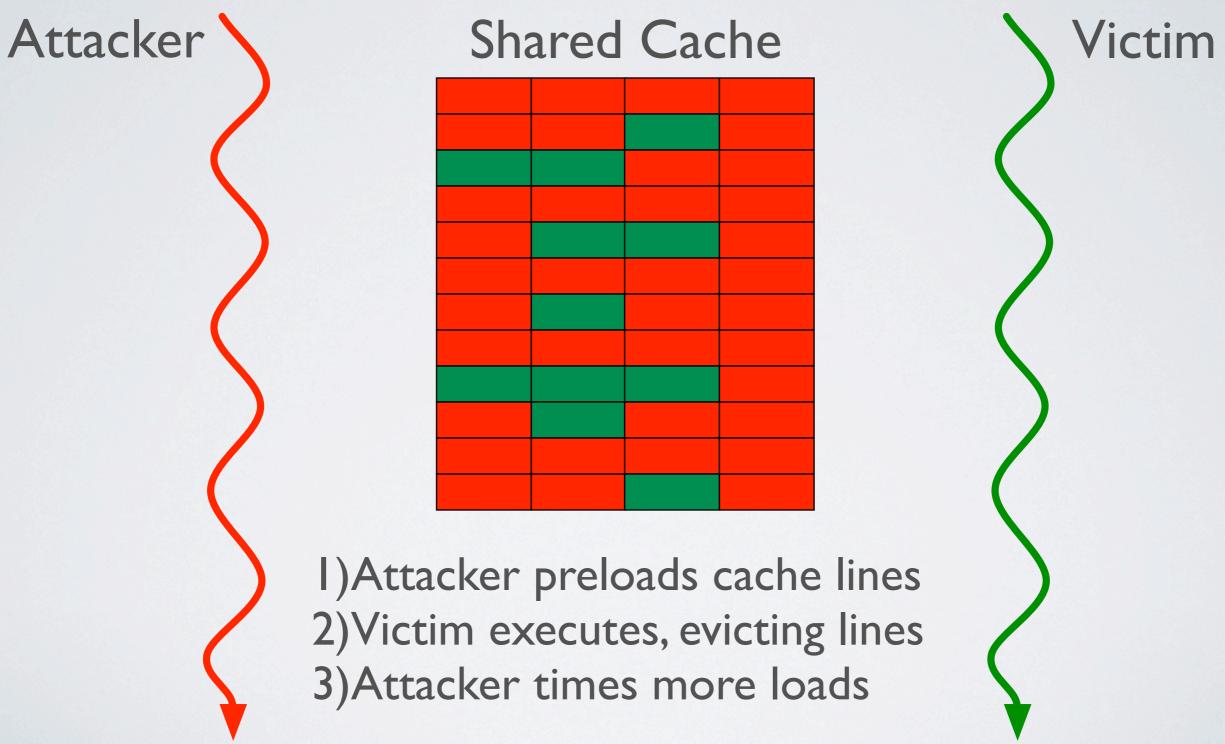
# Attackers look for correlation between secret key & observed patterns

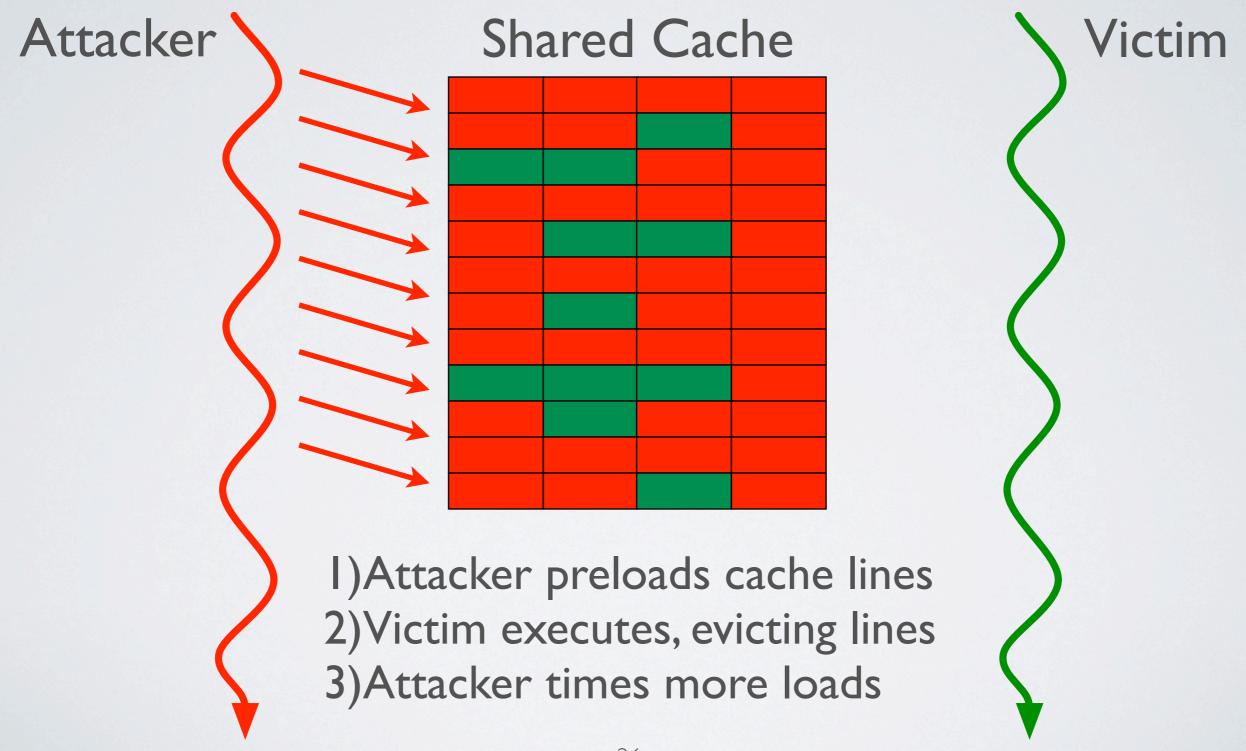


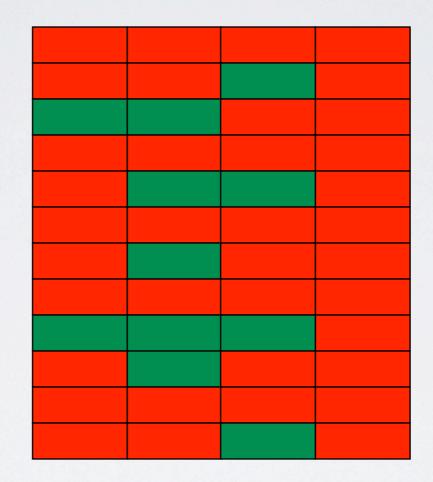




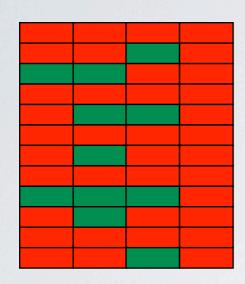






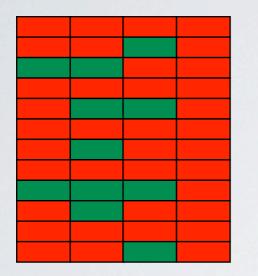


### Time



Cache Snapshots

### Time

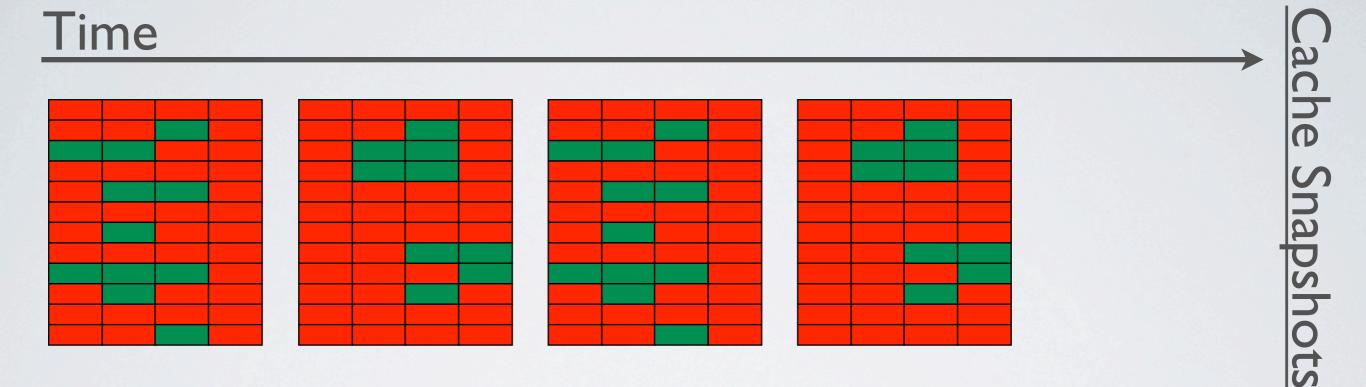


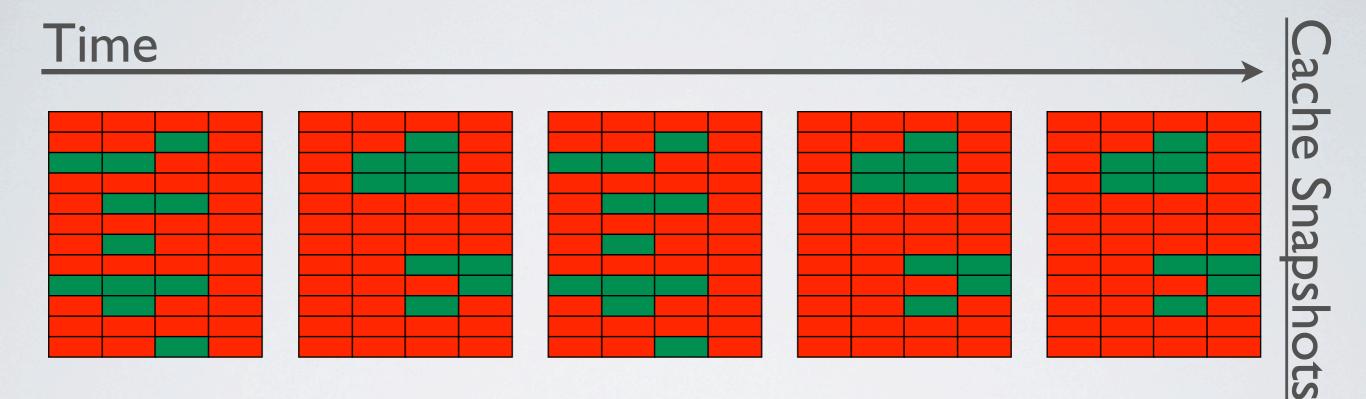
Cache Snapshots

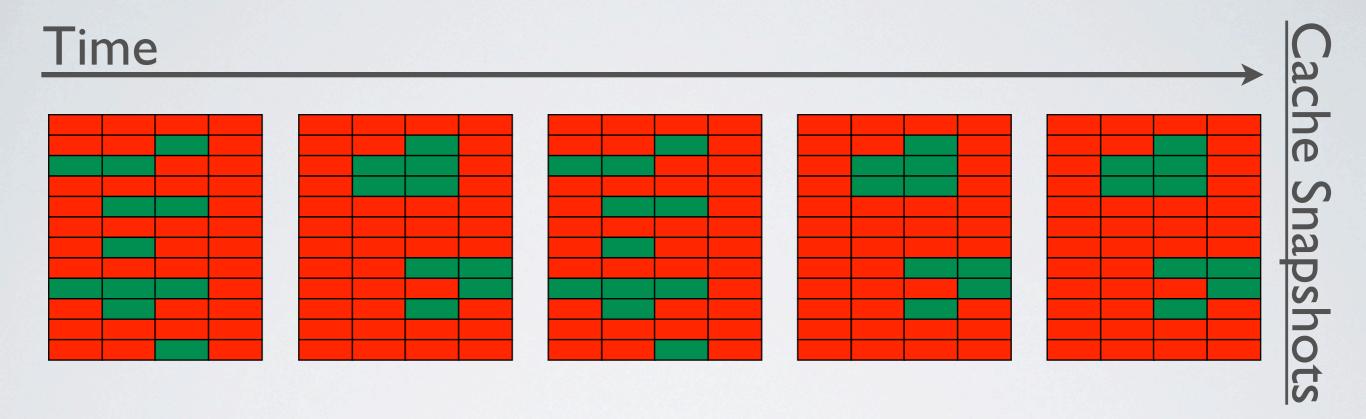
### Time

		1.1

Cache Snapshots

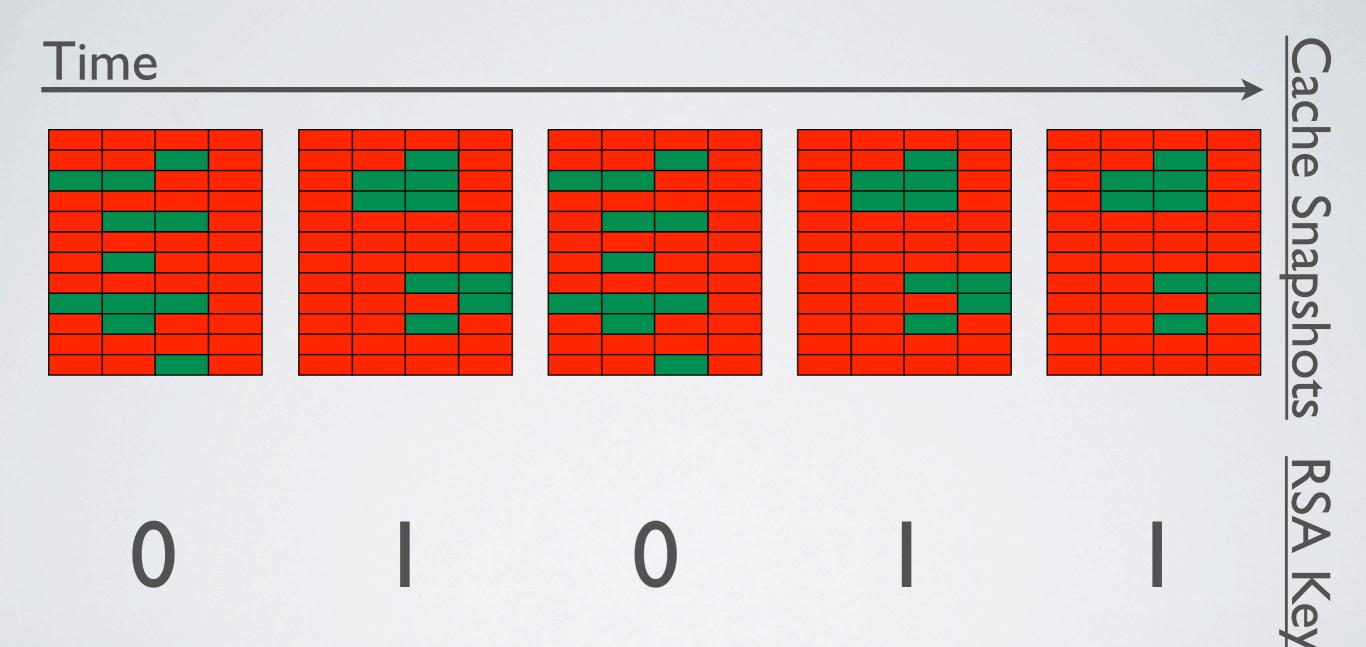






 $\mathbf{O}$ 

 $\left( \right)$ 



### Key Observation

### Attackers look for patterns

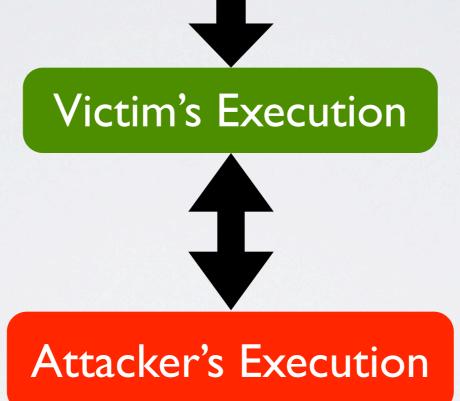
## Side-channel Vulnerability Factor

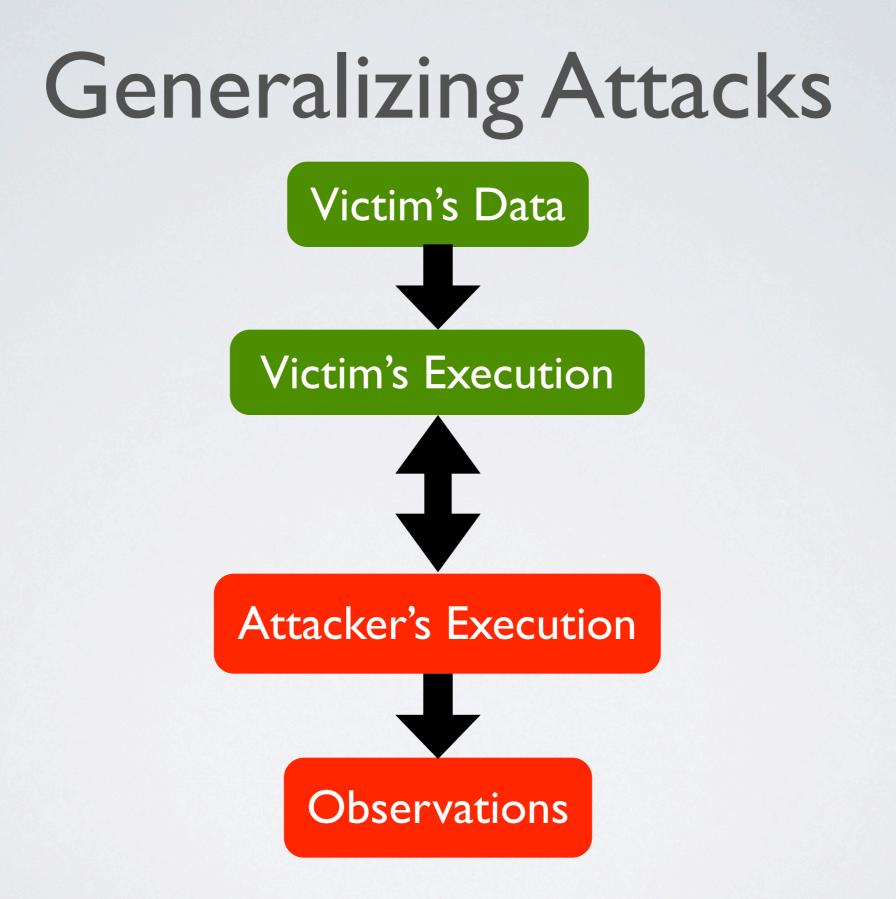
Measuring information leakage

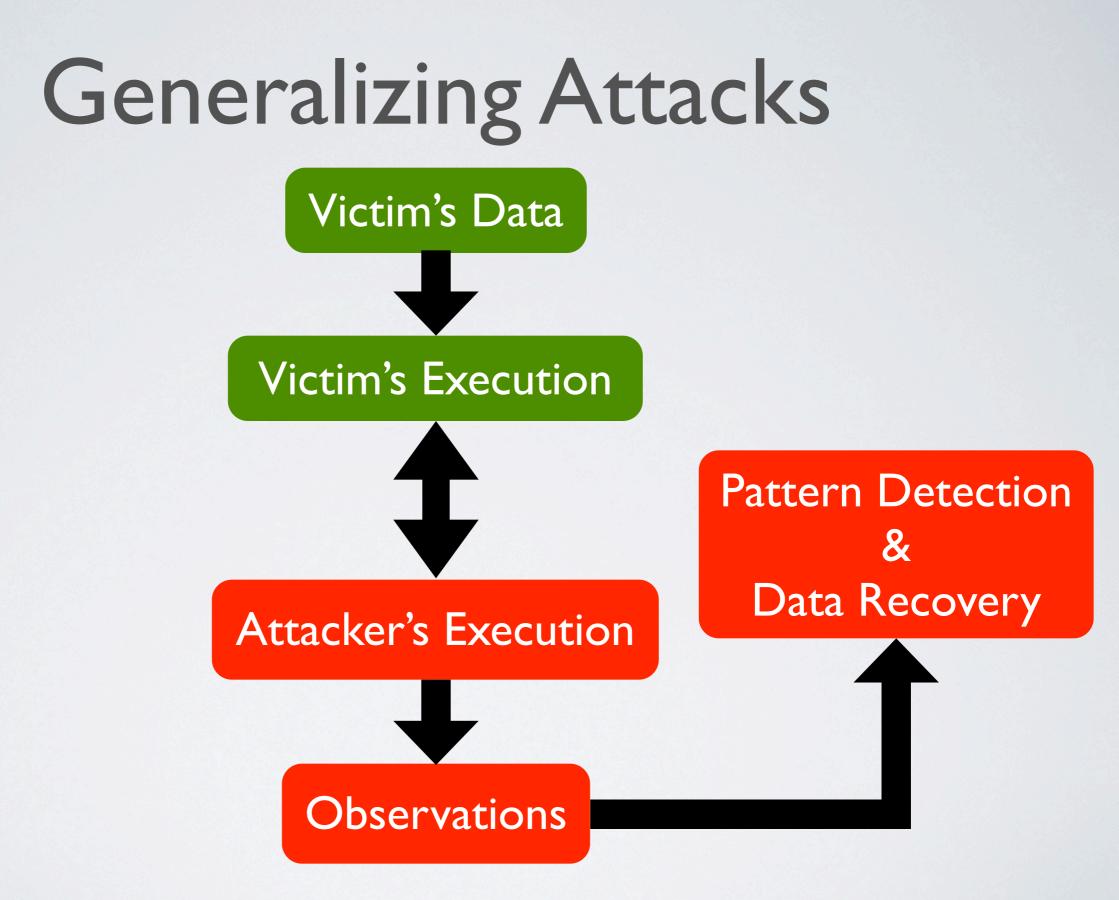
Victim's Data



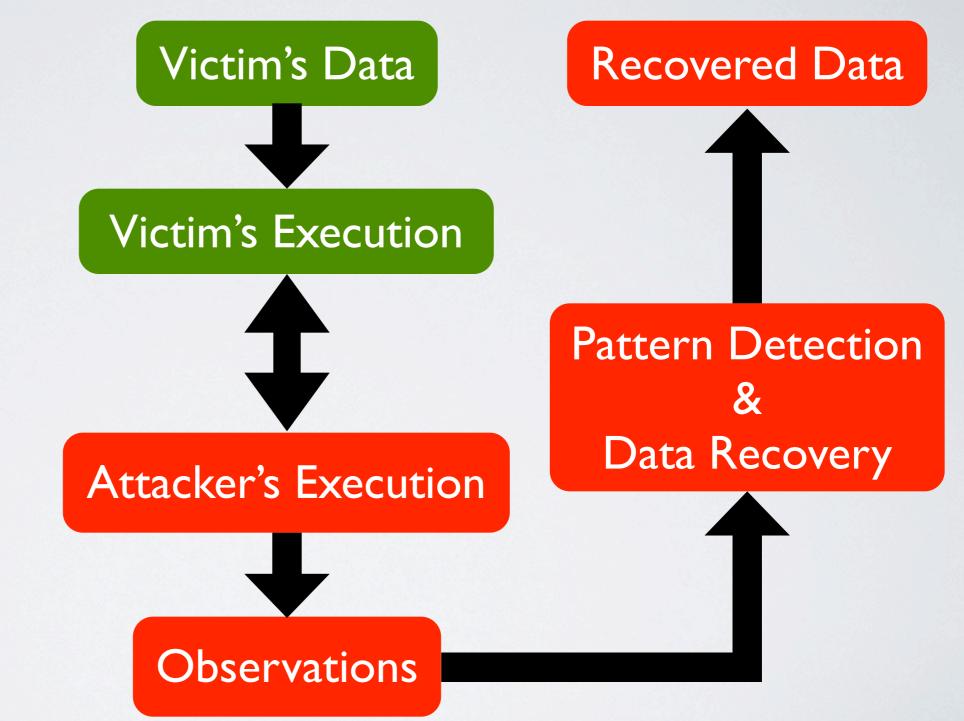
# Generalizing Attacks Victim's Data

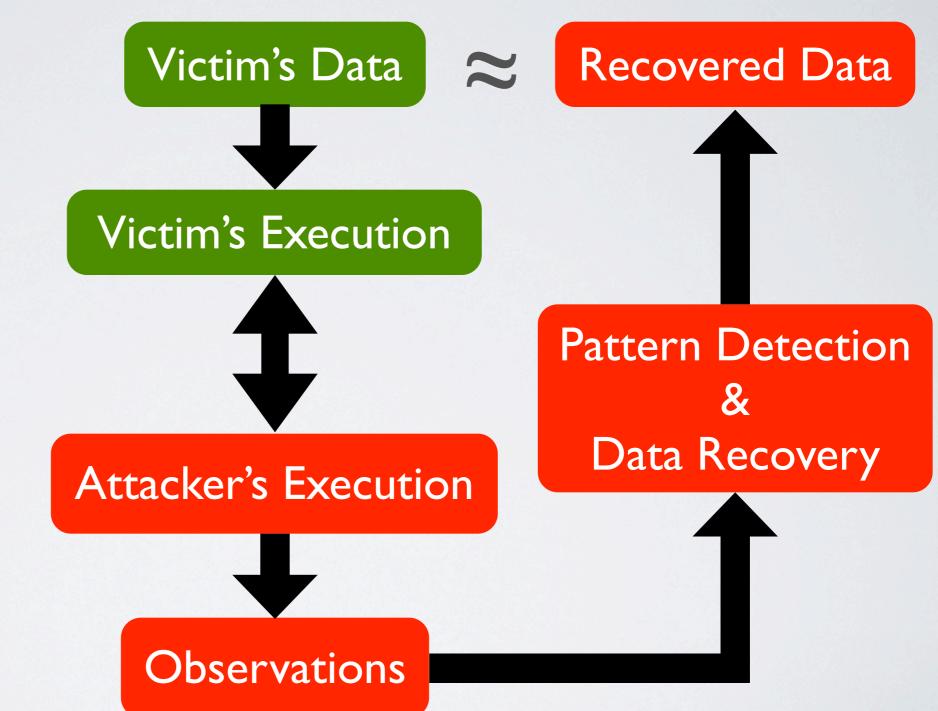




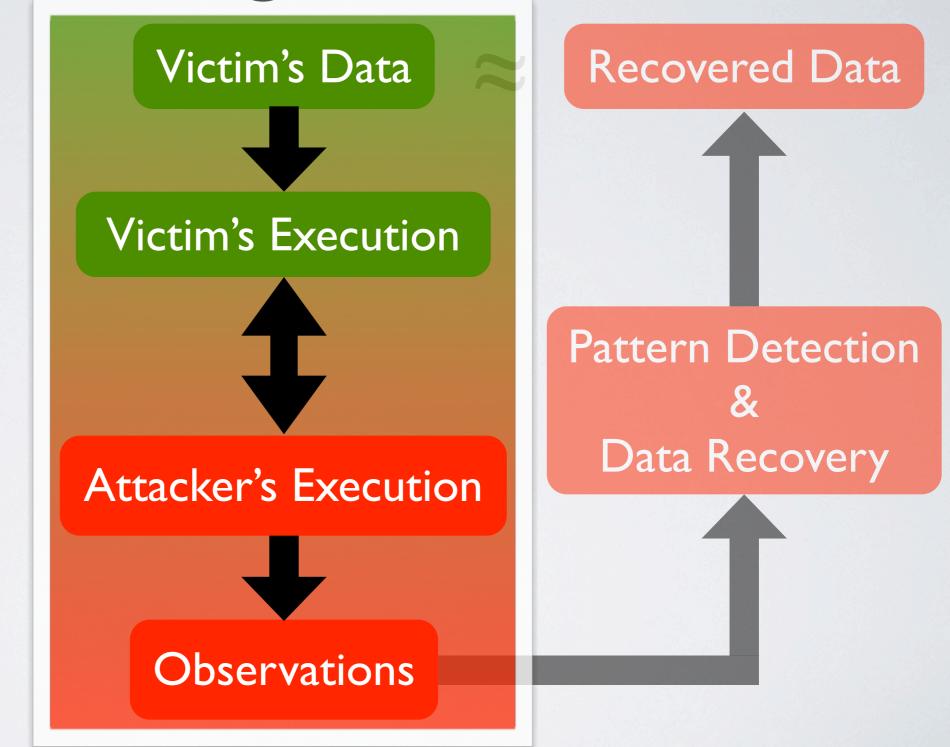


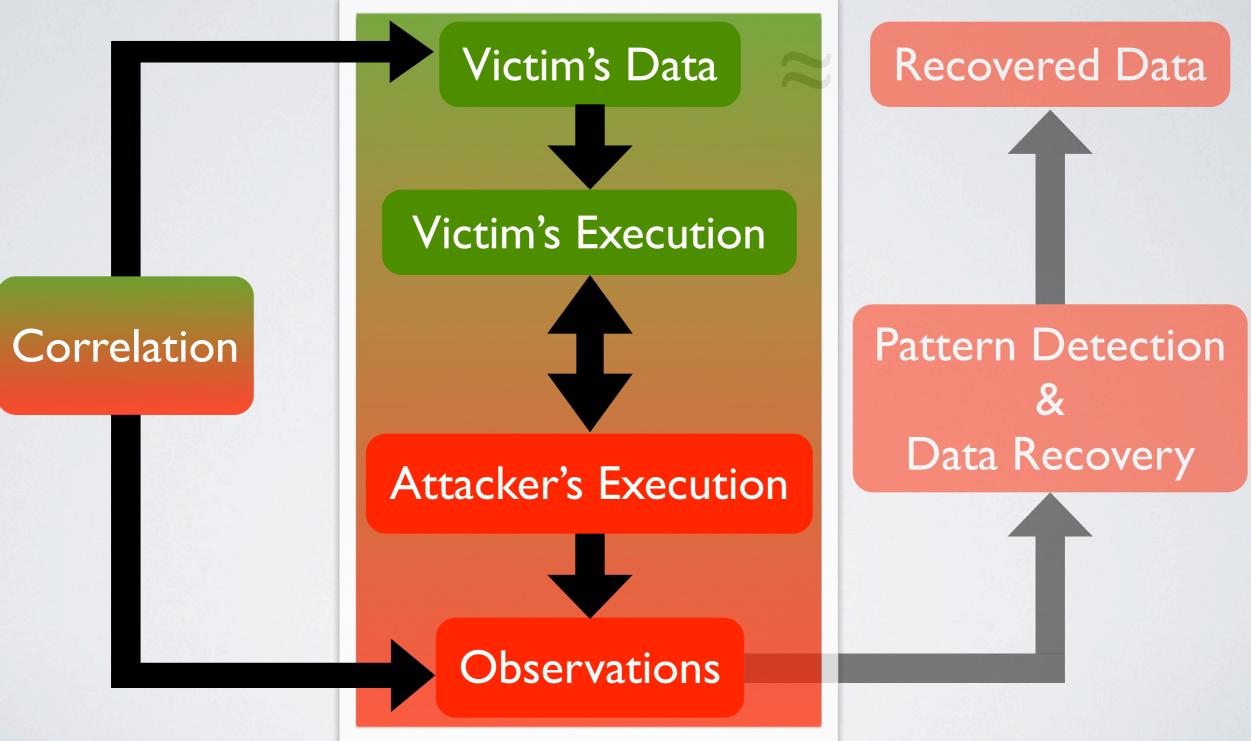
#### 

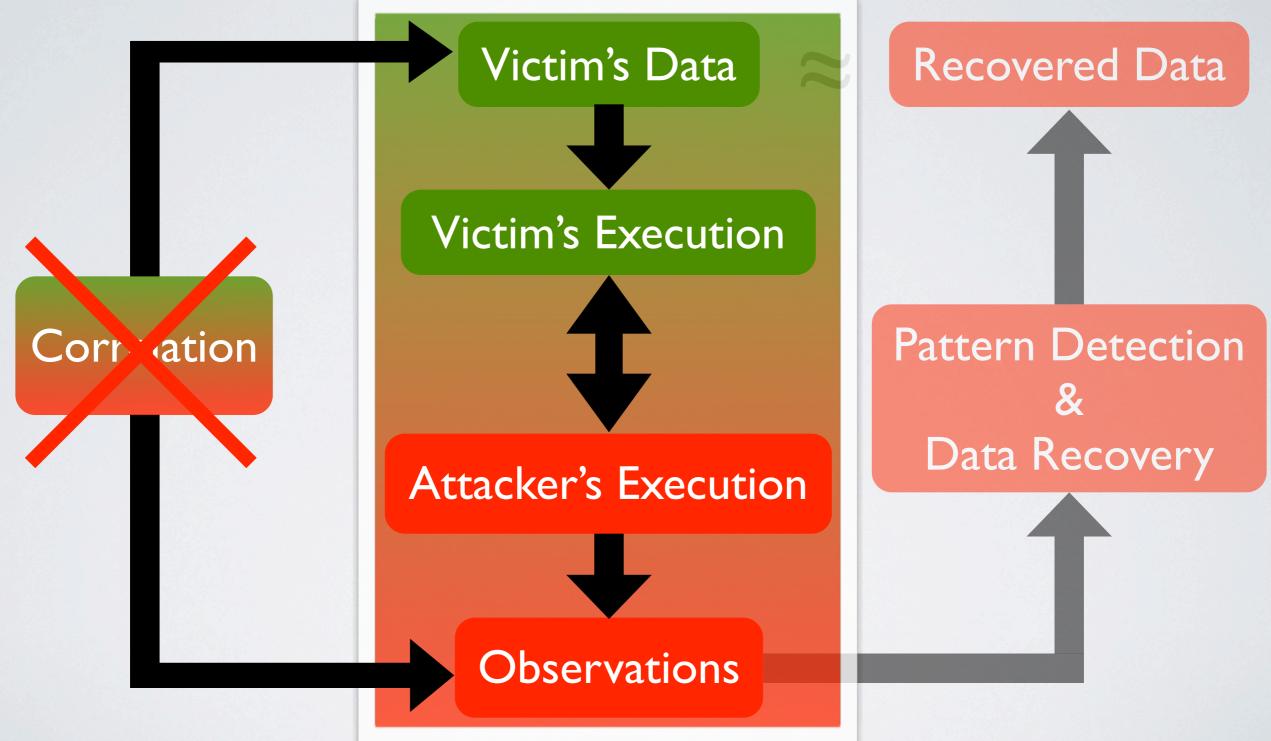


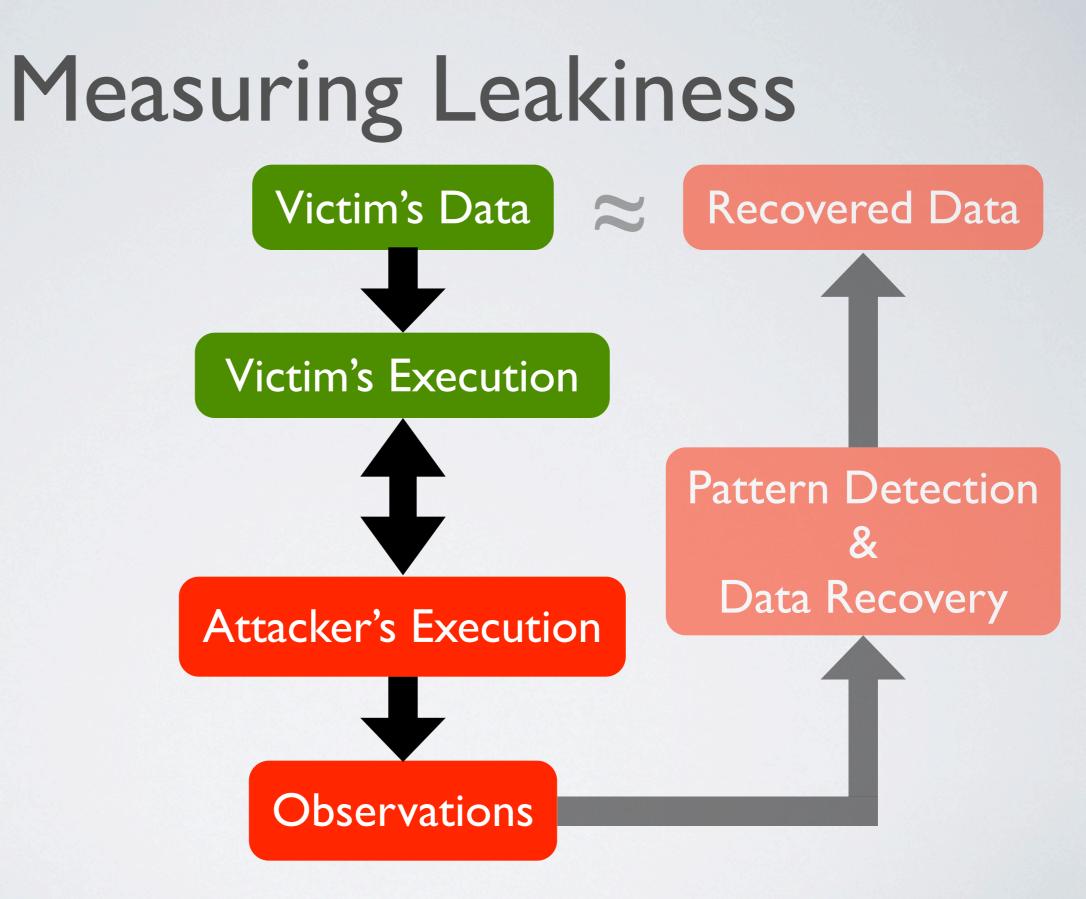


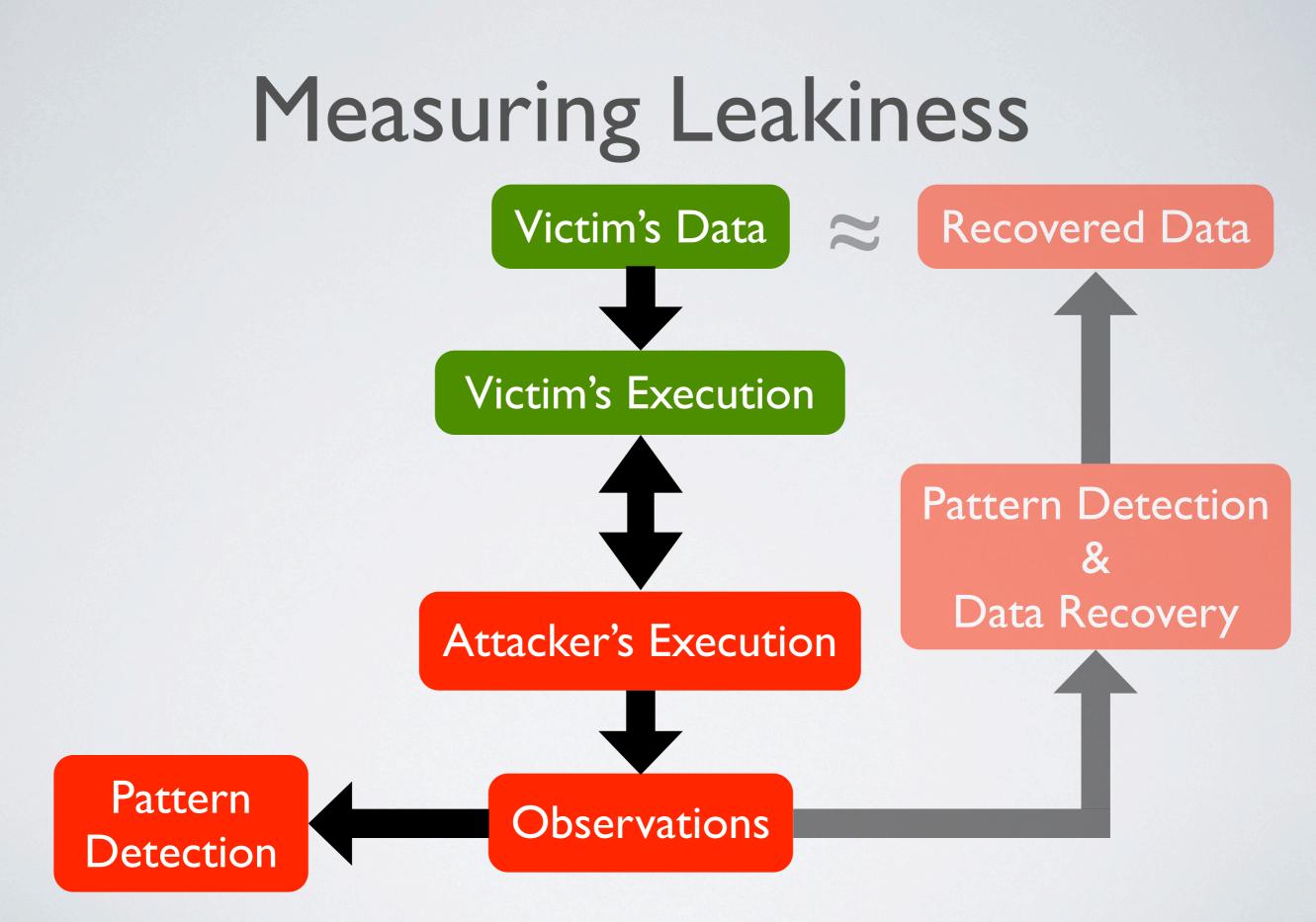


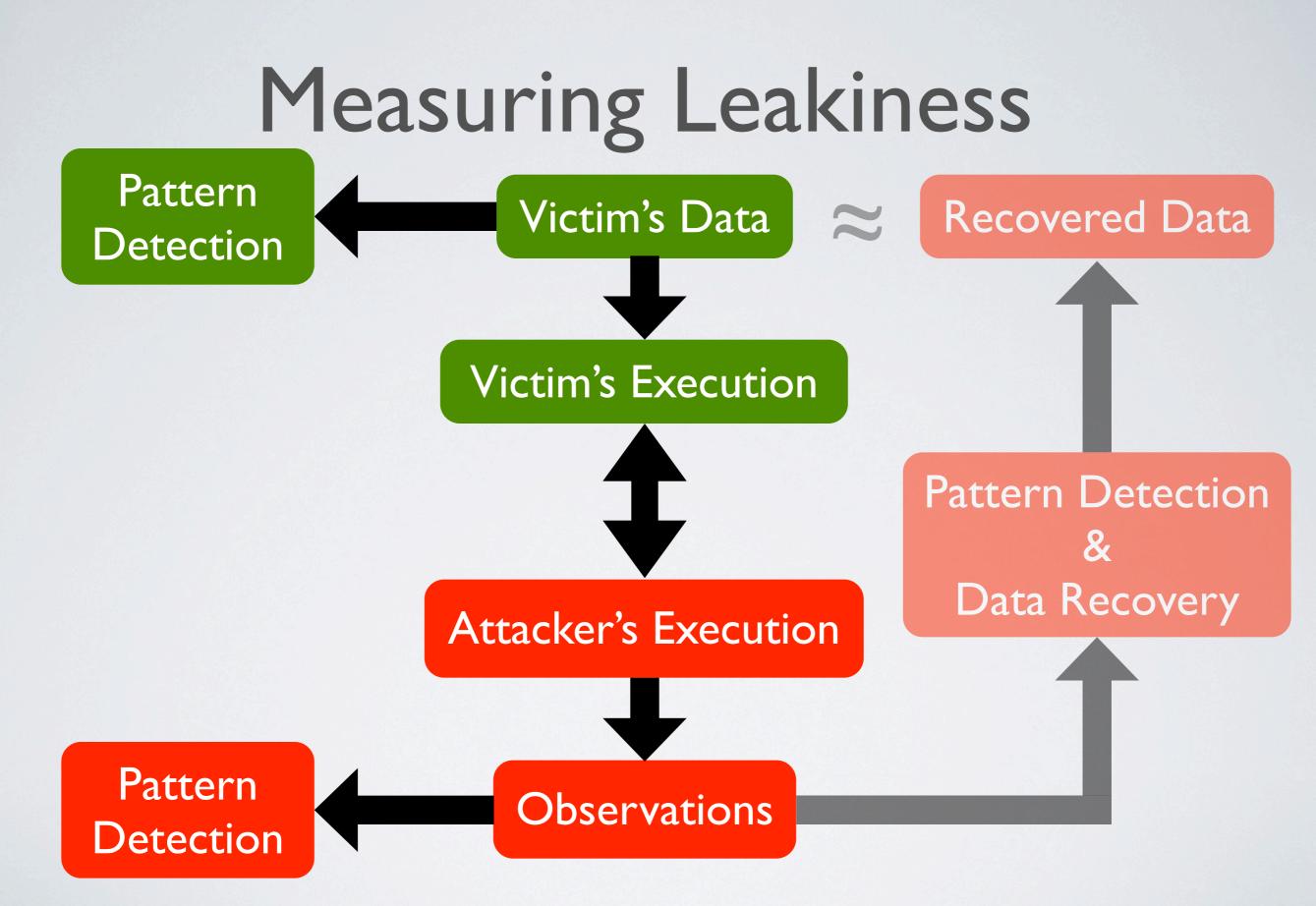


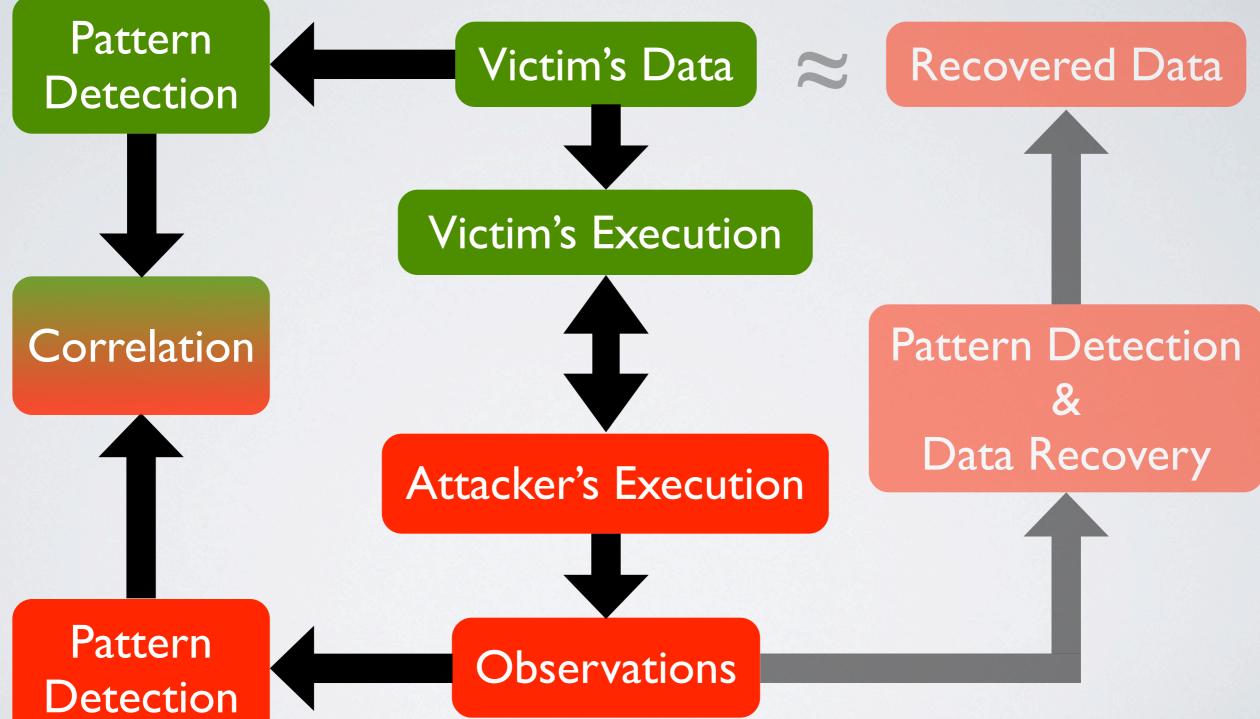




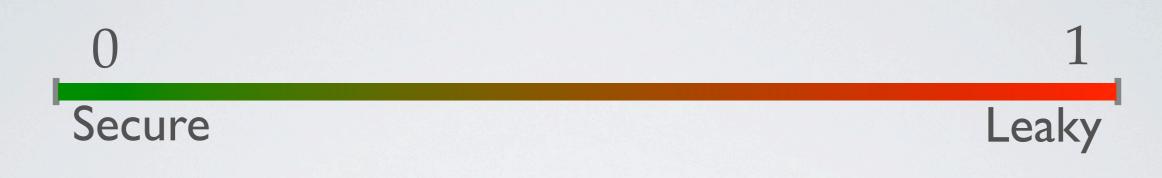


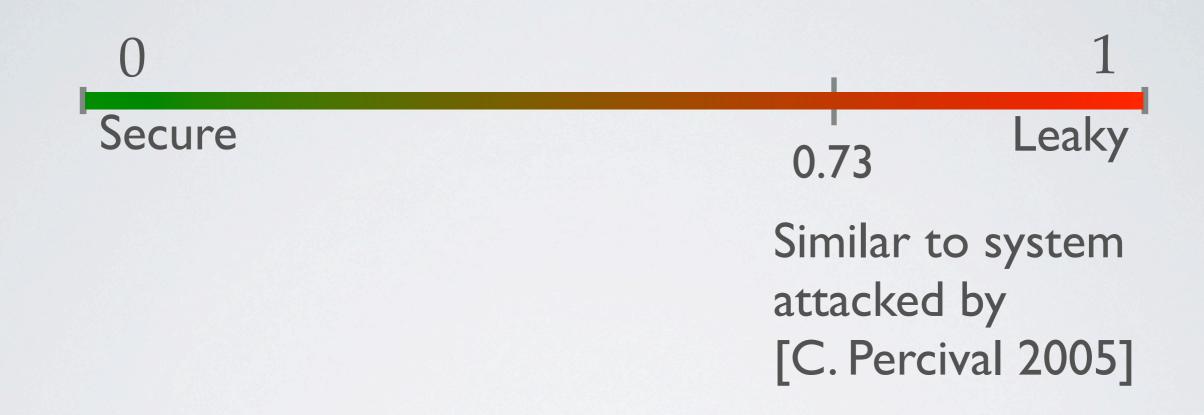


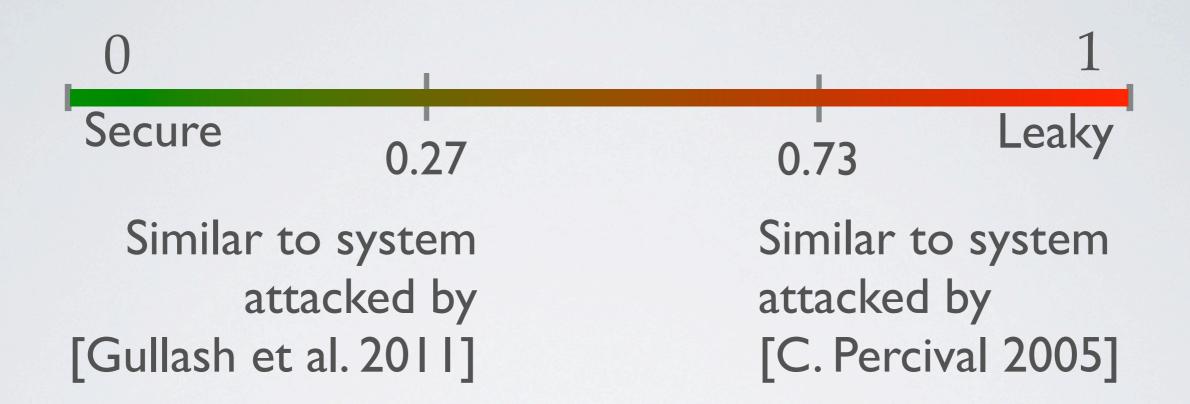


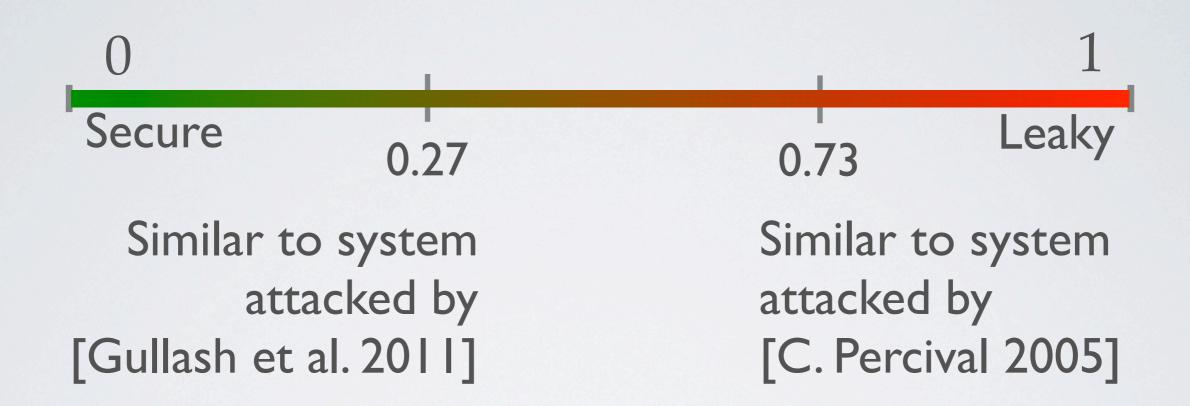


### SVF is the **correlation** between **patterns** in attacker observations and **patterns** in victim's execution



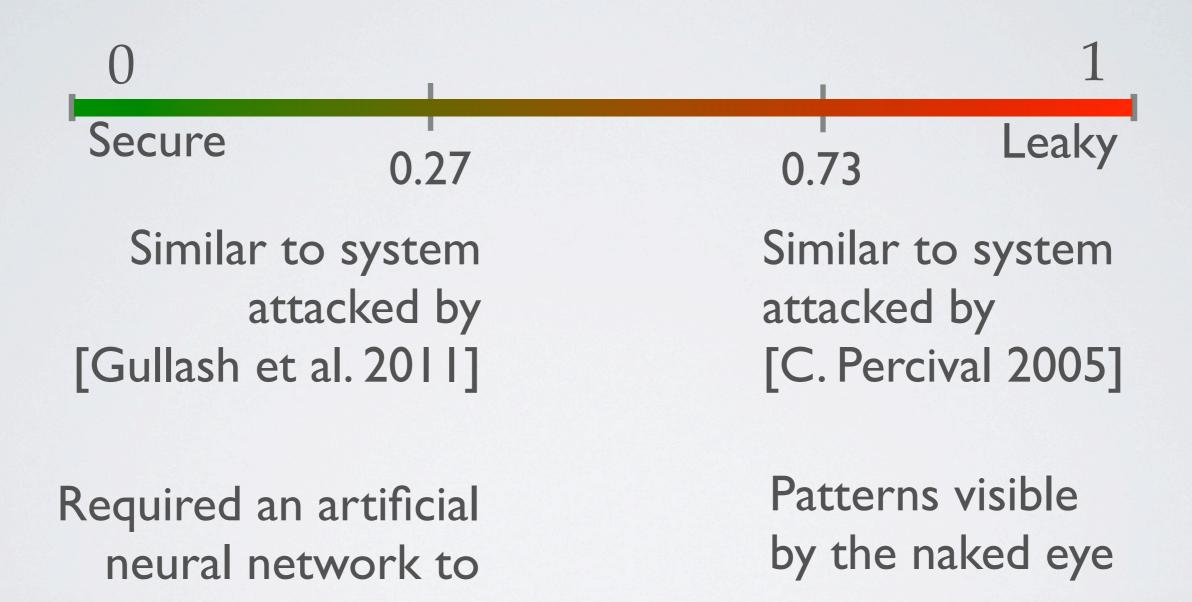






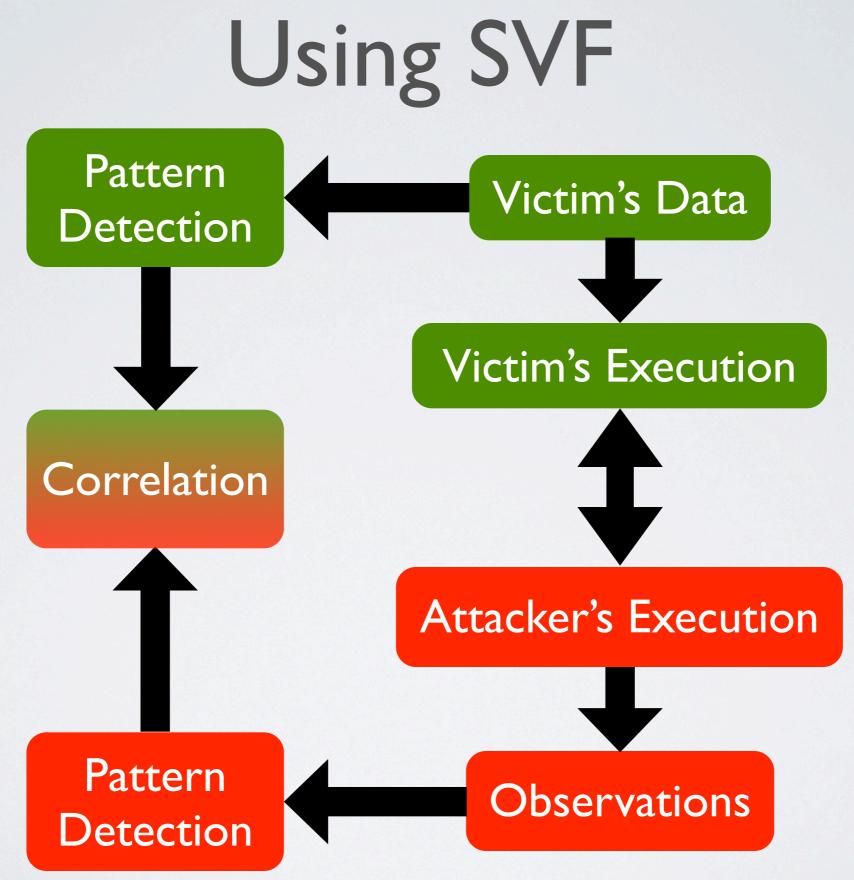
Required an artificial neural network to classify measurements

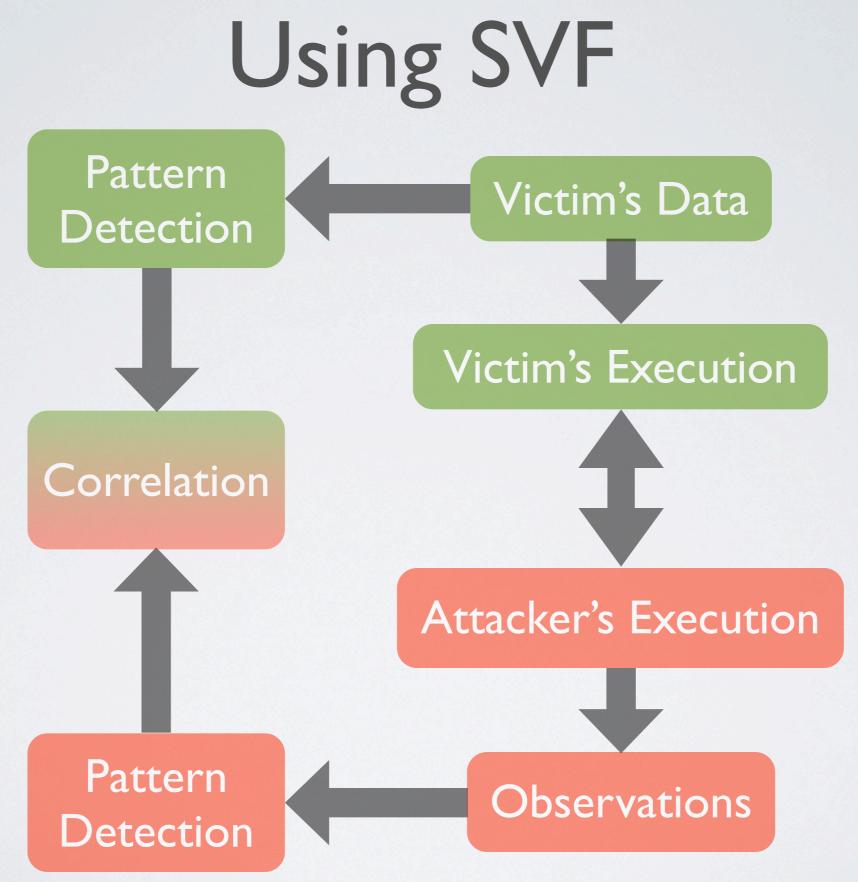
35

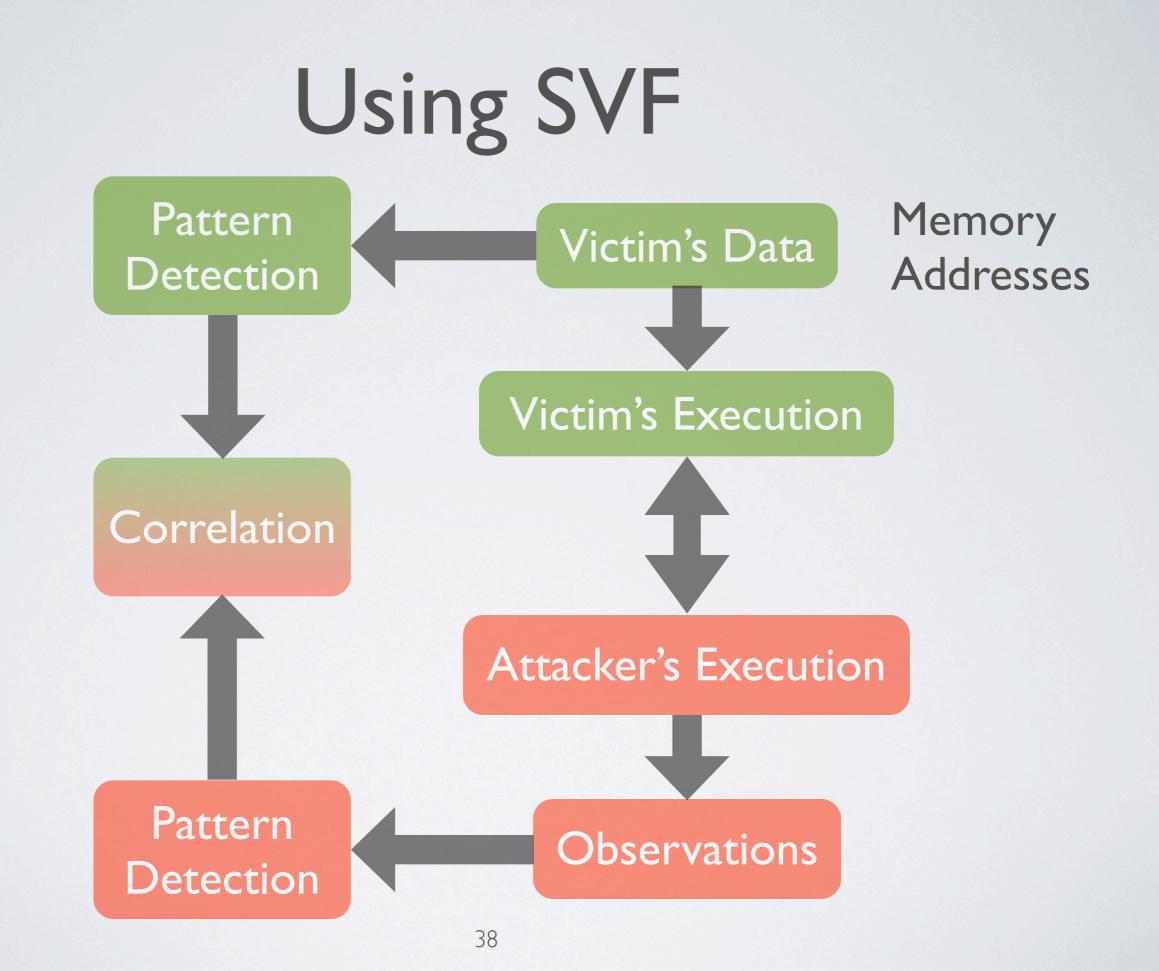


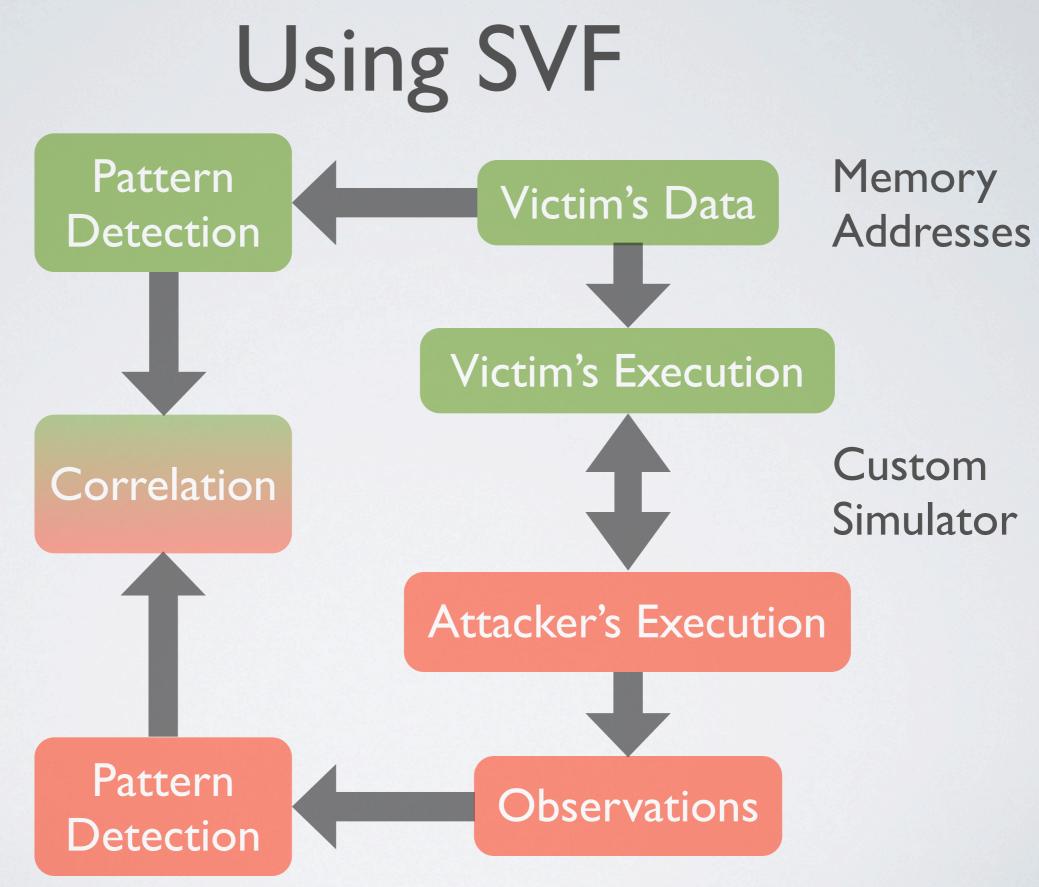
classify measurements

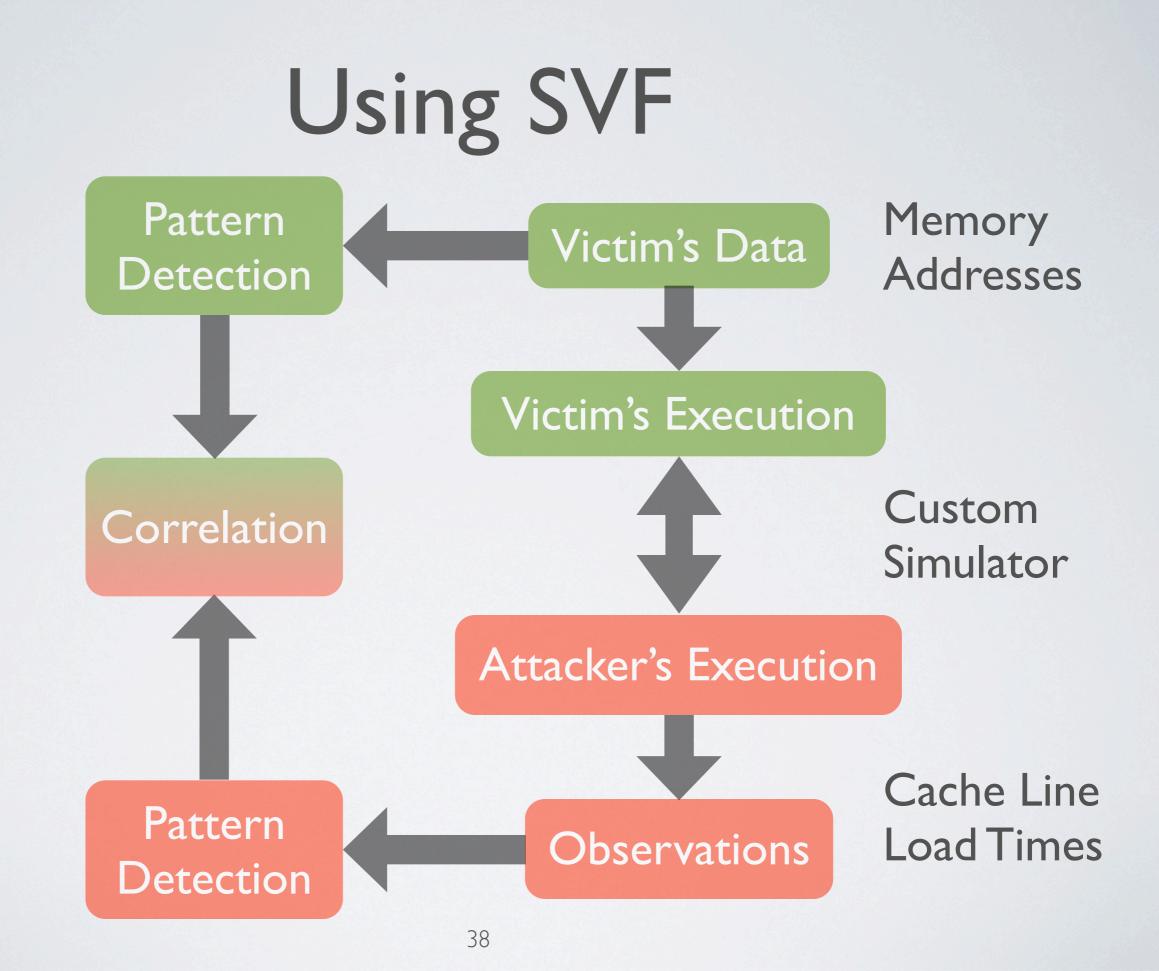
**SVF** Illustration

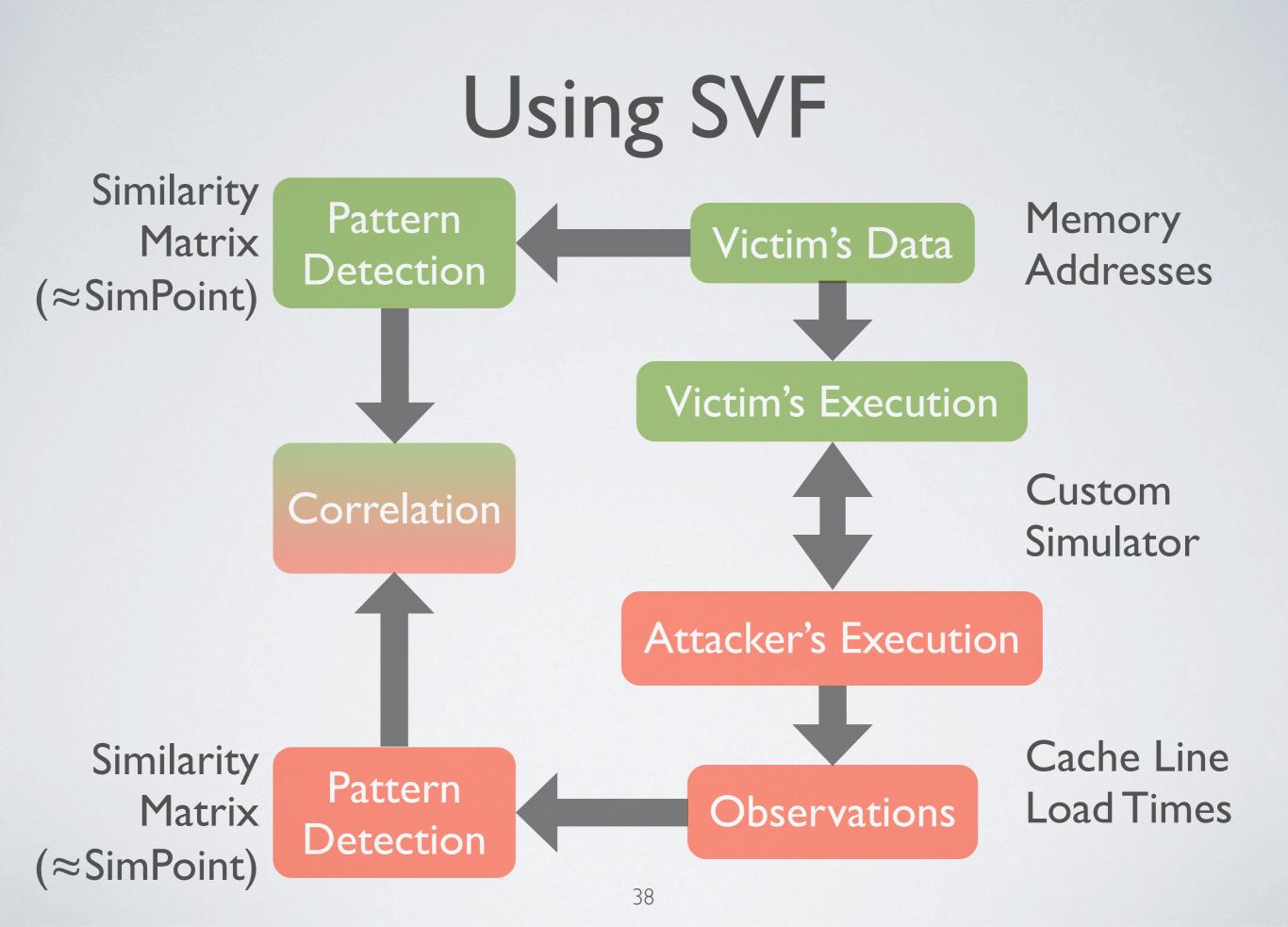


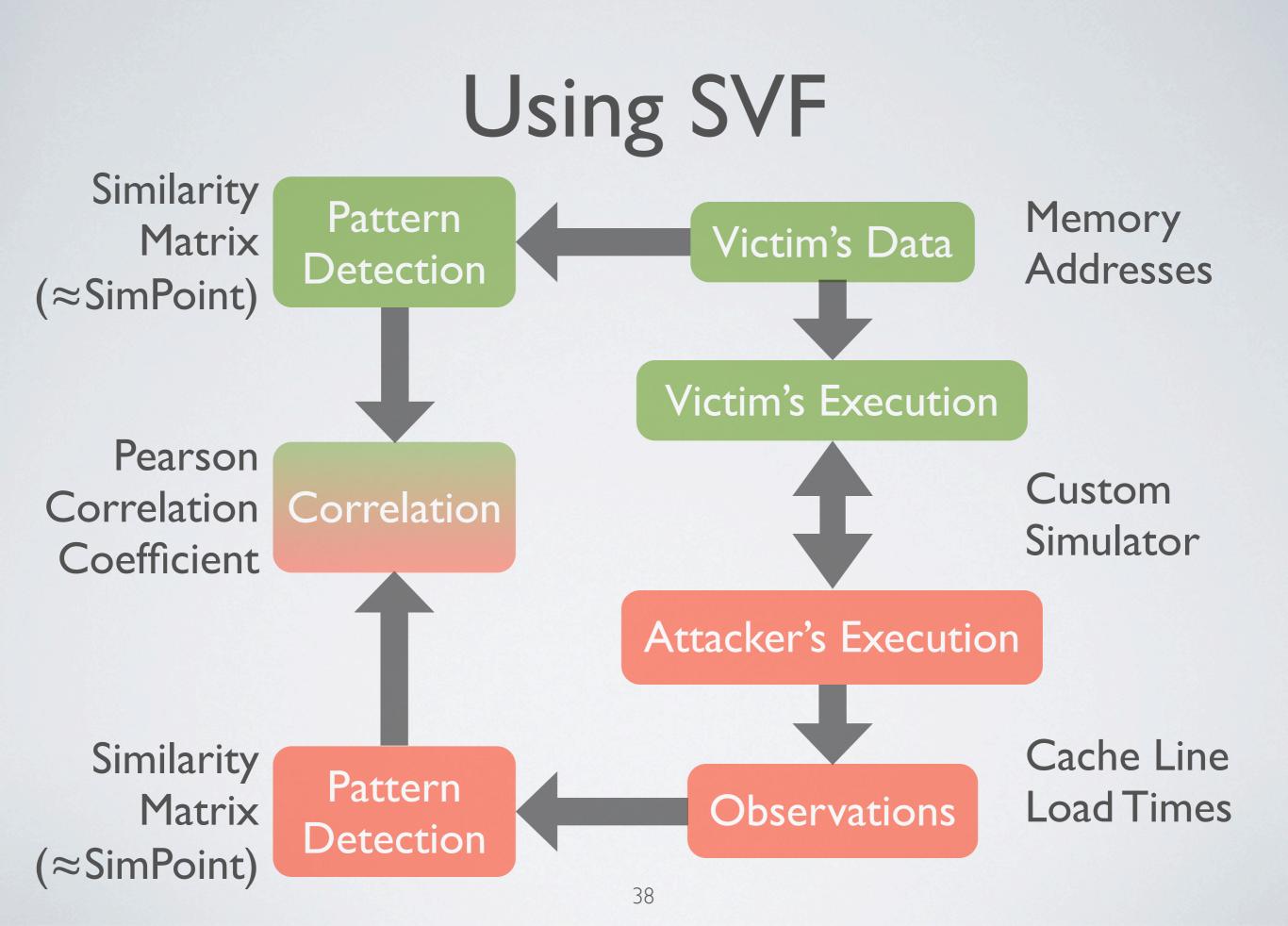












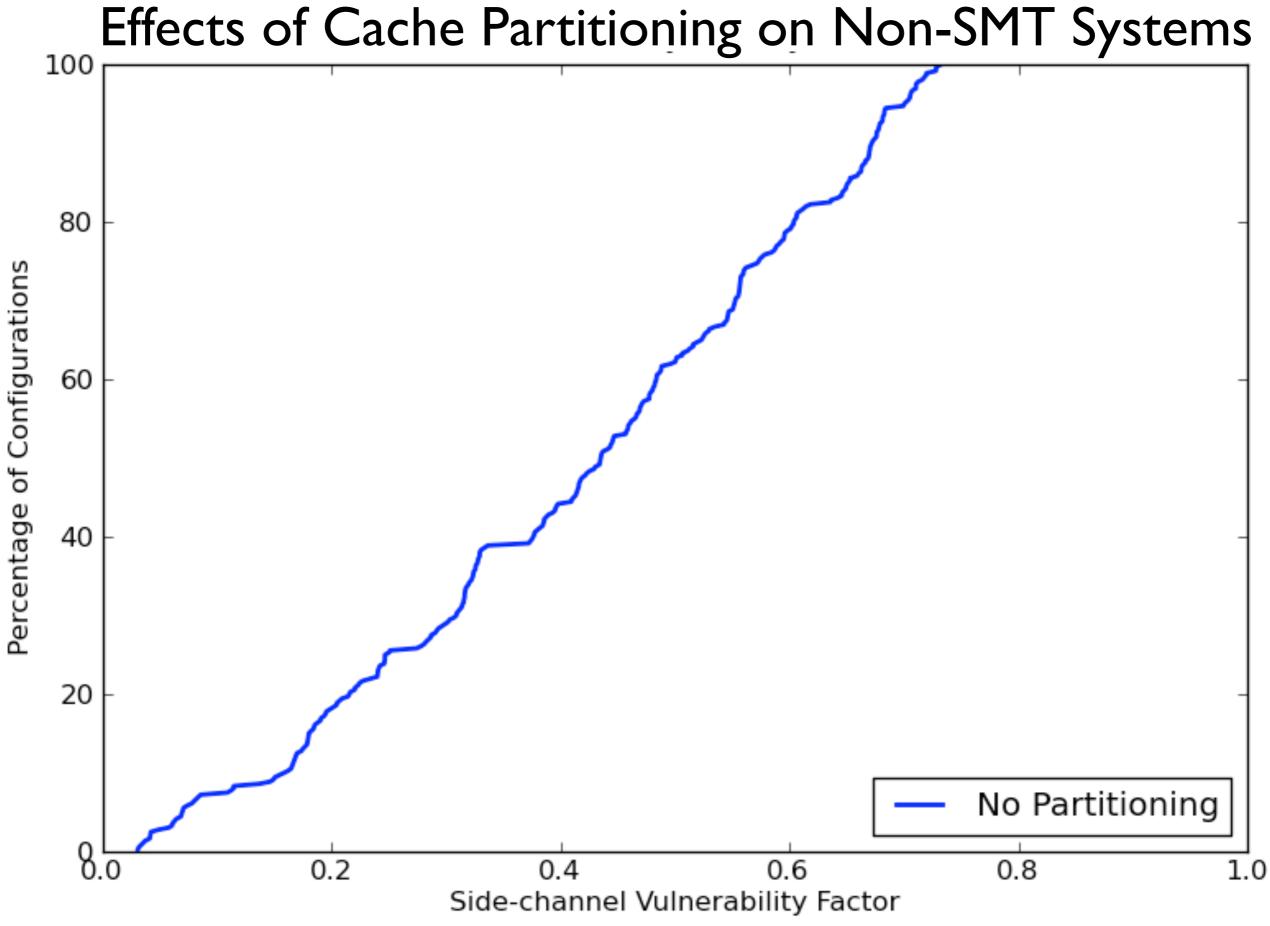
# A Large Design Space

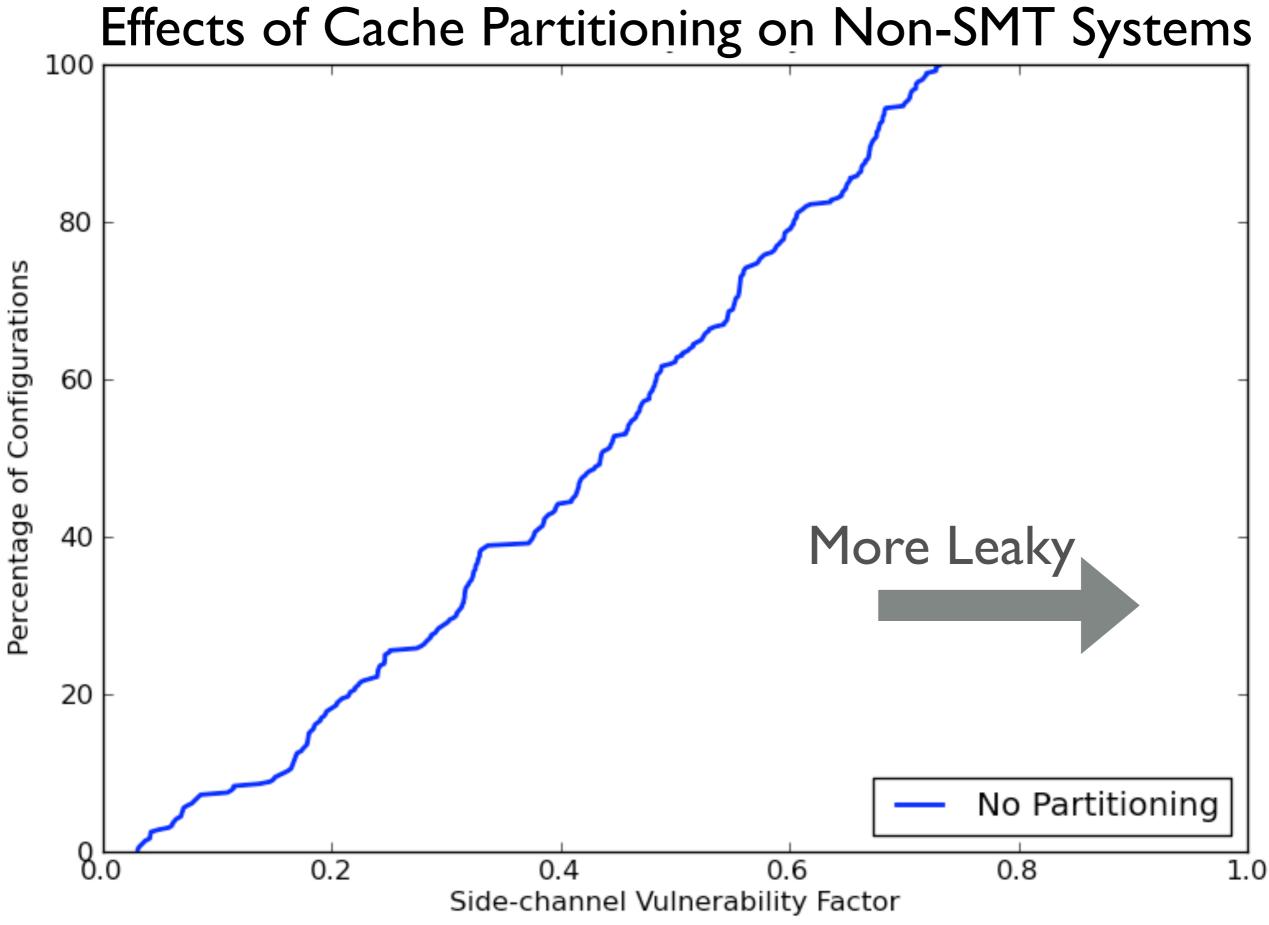
SMT x Cache Size x Line Size x Associativity x Hashing x Prefetching x Partitioning x Protection

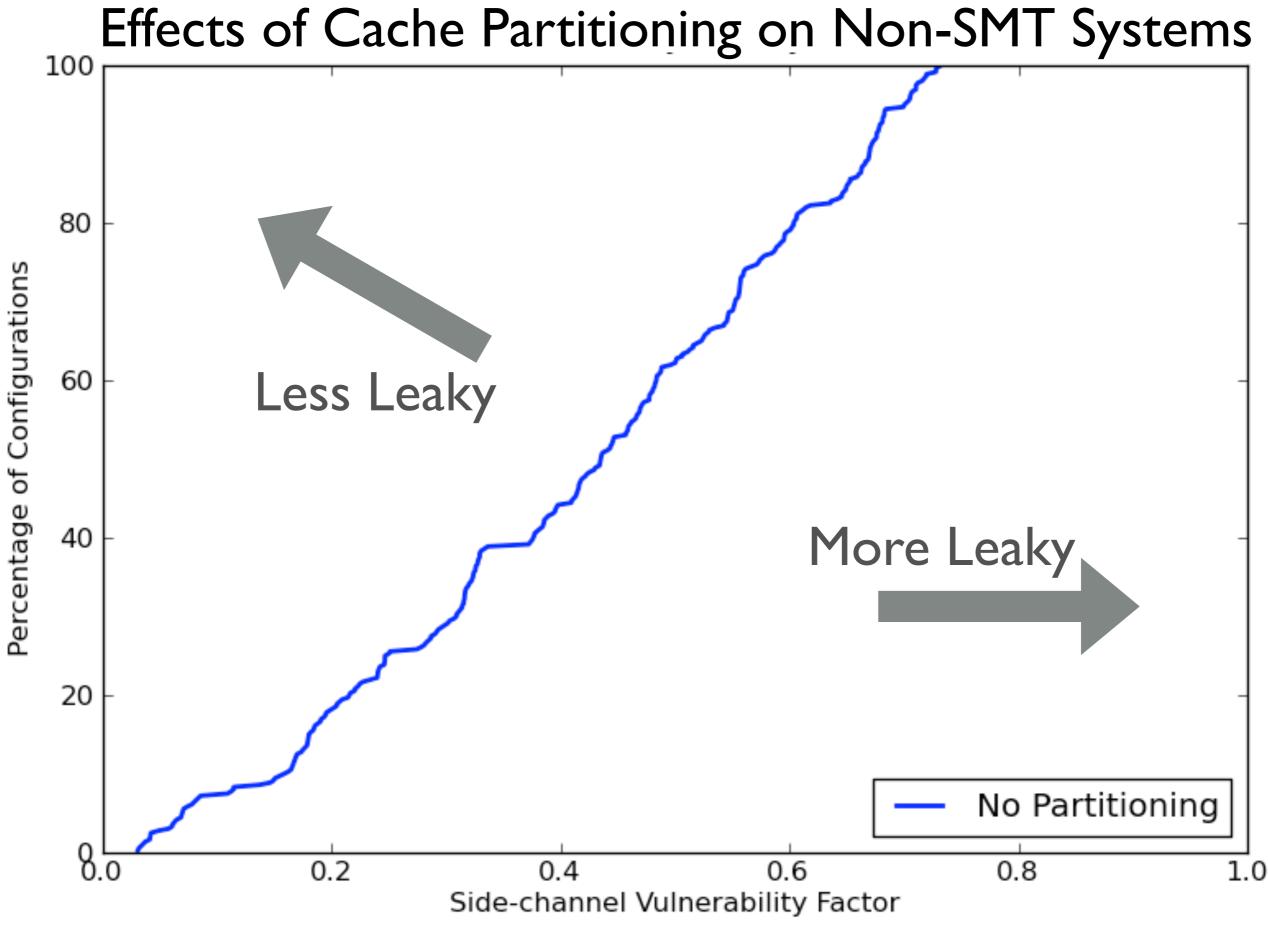
#### 34,020 Simulations

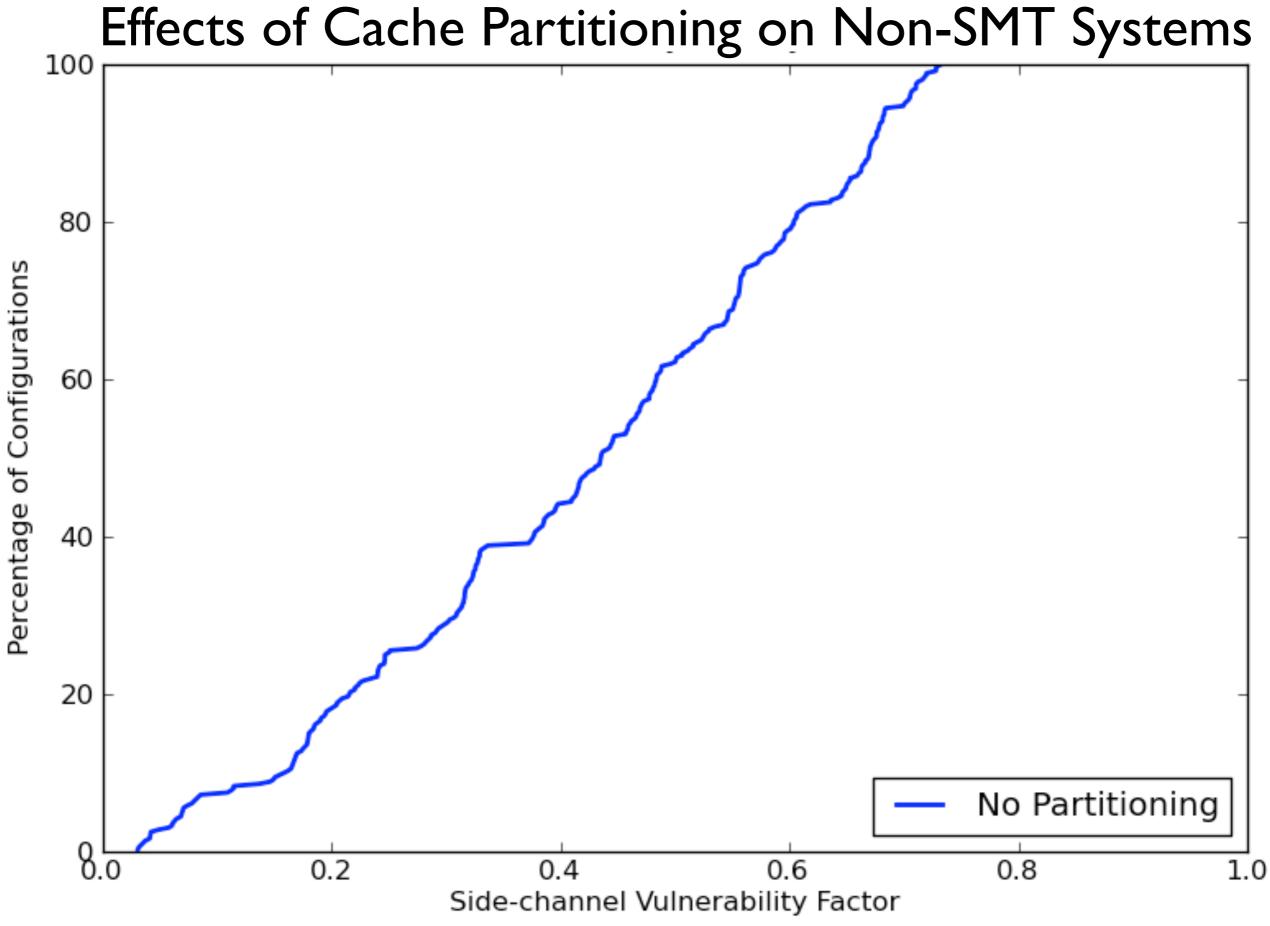
### • We examine PRS with our policies, not RPCache

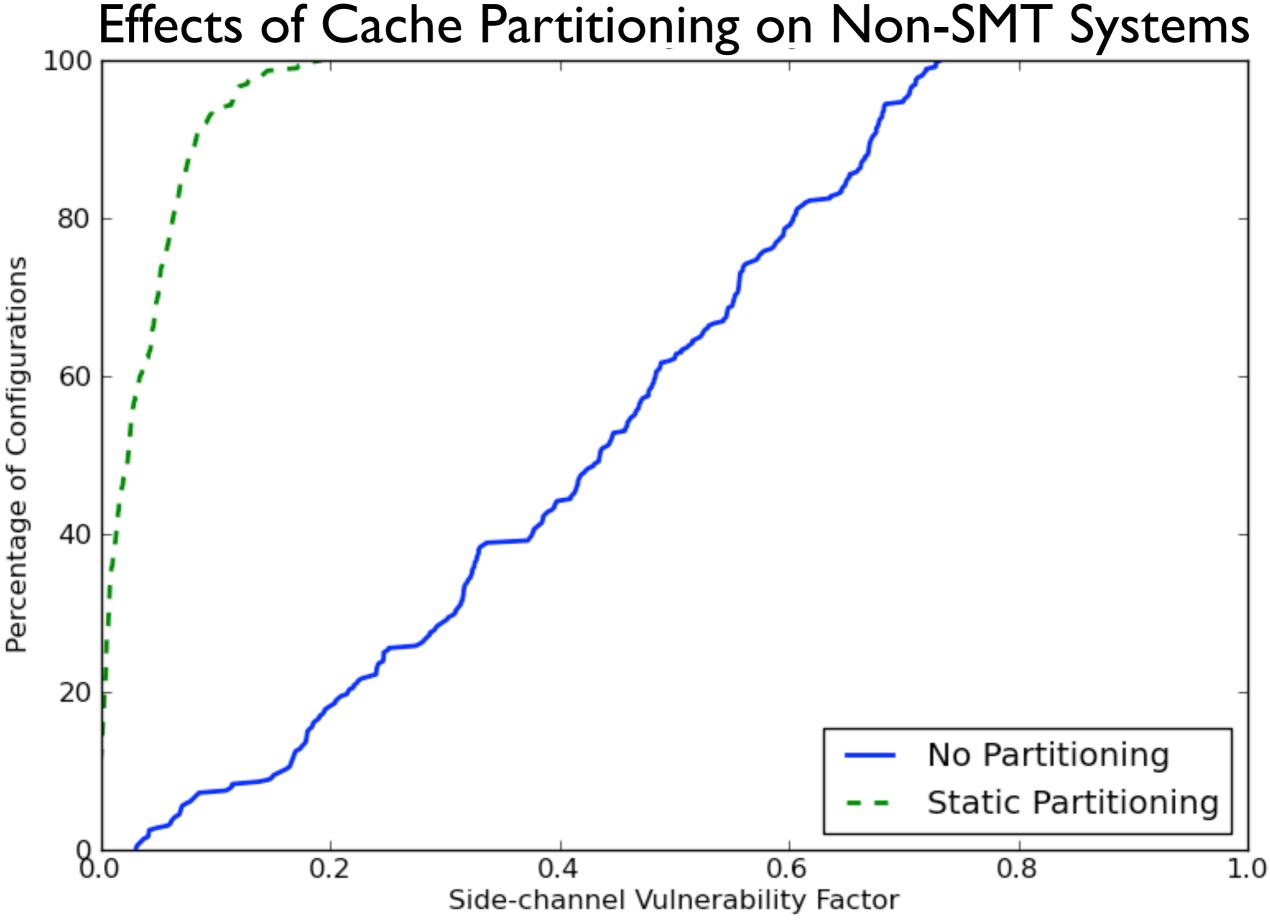
- Refer to: Z. Wang and R. B. Lee. Covert and side channels due to processor architecture. ACSAC '06
- Results are specific to our simulator
  - While SVF can be a comparative tool, this is not a comparative study

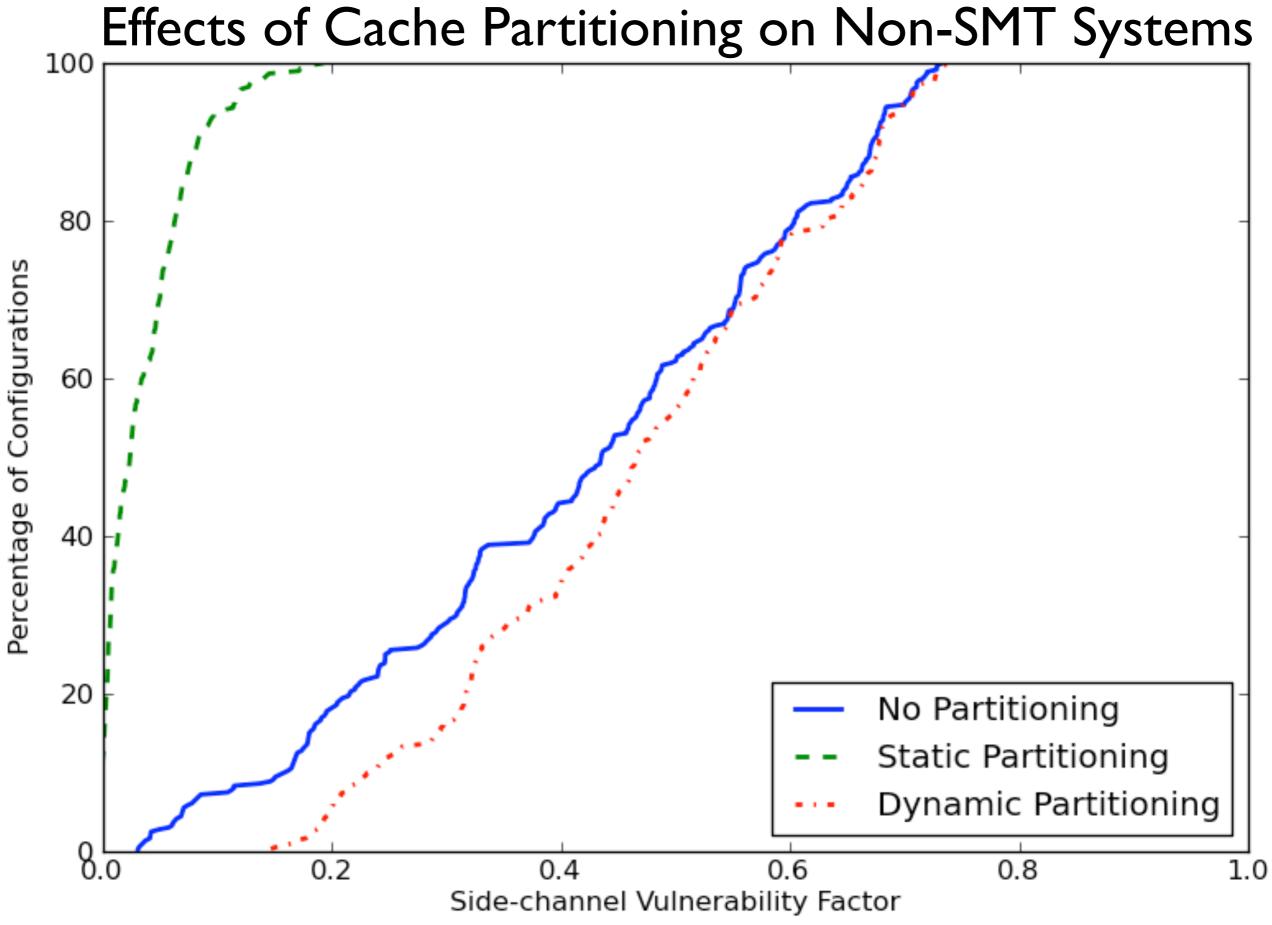




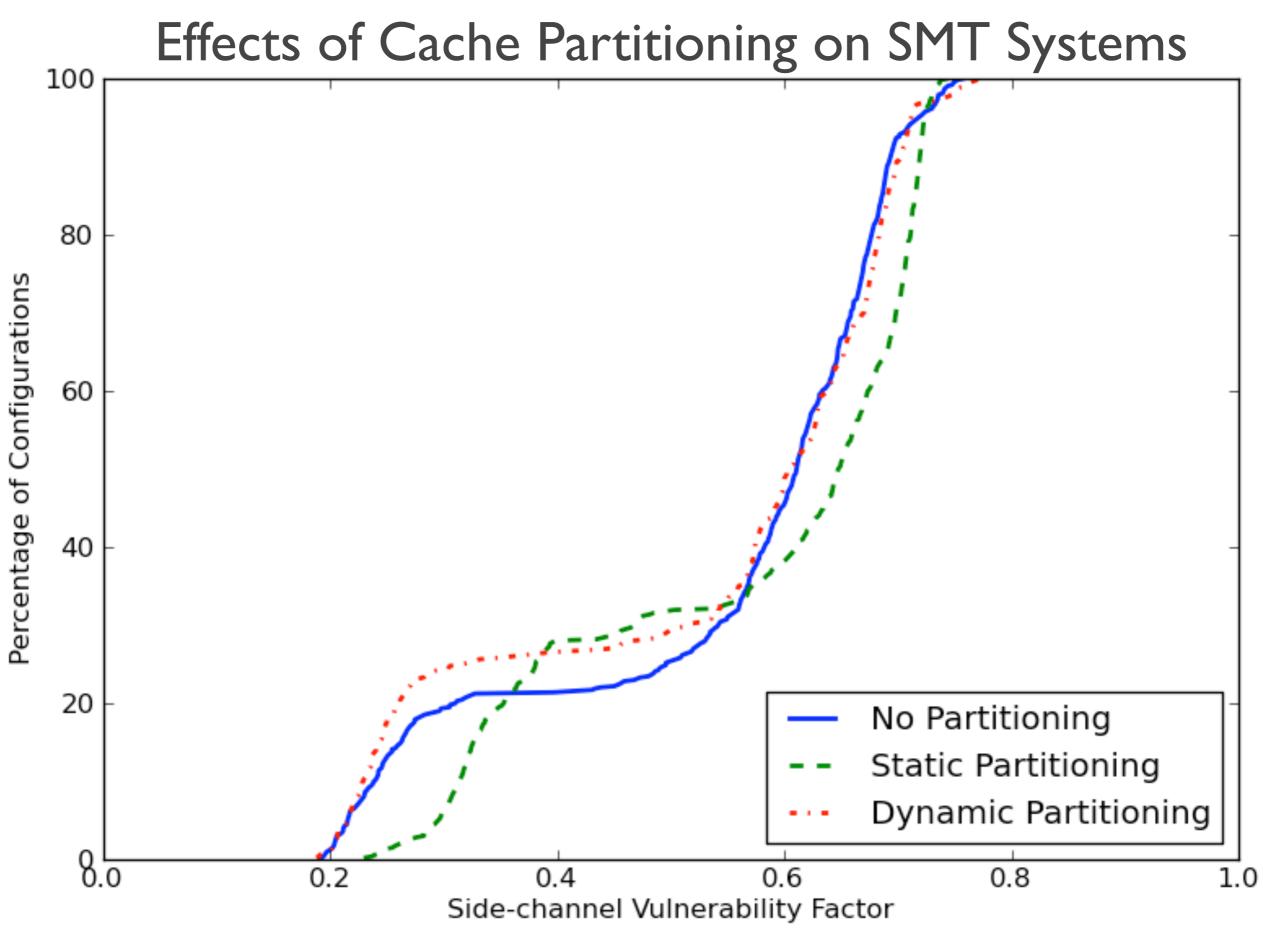








#### Effects of Cache Partitioning on SMT Systems



### **Related Work**

- Physically Observable Cryptography [Micali & Reyzin 2004]
- Predictive Cache Leakage Model [Dominister et al. 2010]

SVF is practical and generally applicable

### Conclusions

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- SVF: Measures information leakage
  - General, practical, quantitative

## Conclusions

- SVF: Measures information leakage
  - General, practical, quantitative

- Key Insight
  - Attackers correlate measured patterns to victim's secrets

# Impact & Future Work

# Impact & Future Work

- Uses / impact
  - Early design-phase security analysis
  - Performance-security tradeoffs

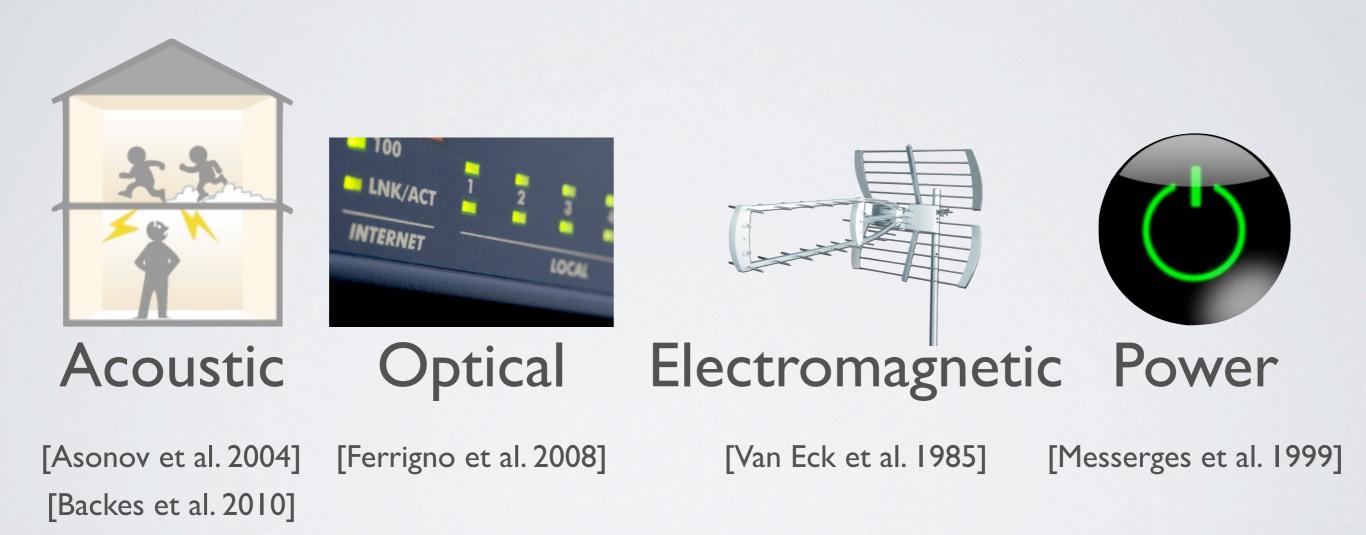
# Impact & Future Work

- Uses / impact
  - Early design-phase security analysis
  - Performance-security tradeoffs

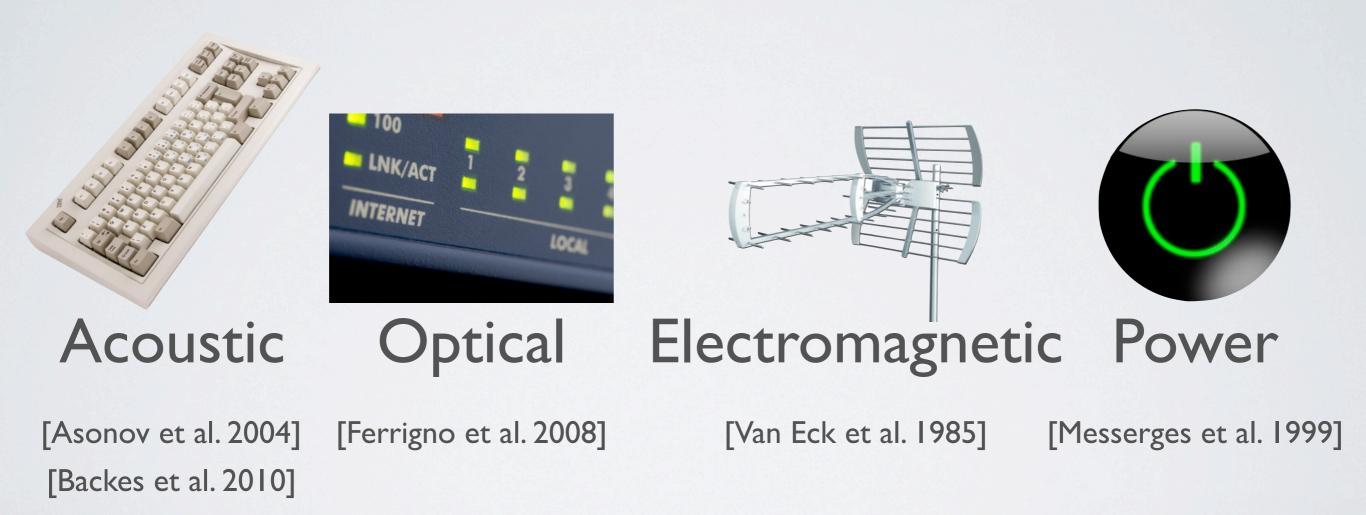
- Future Work
  - Further applications of SVF and improvements
  - Implementing SVF on real systems
  - Automatic identification of side-channels

#### Backup Slides Man down! Need backup!

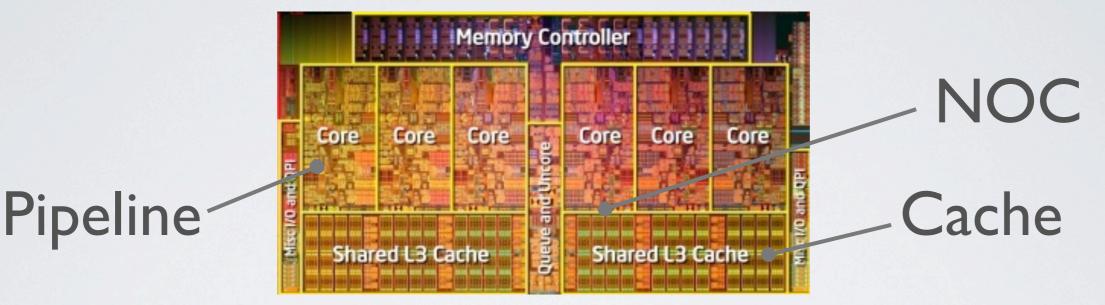
### Types of Side Channels Physical Side Channels



### Types of Side Channels Physical Side Channels



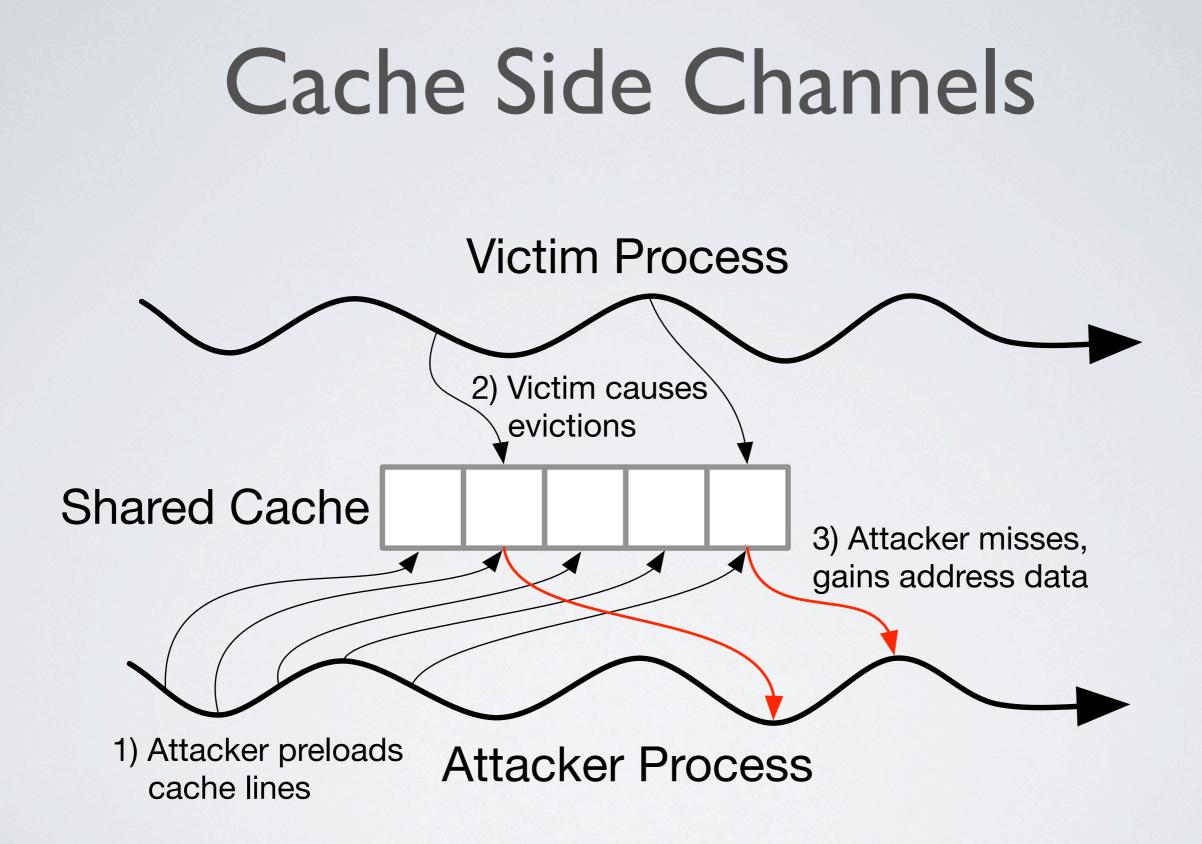
### Types of Side Channels Contention Side Channels



Processor



Network



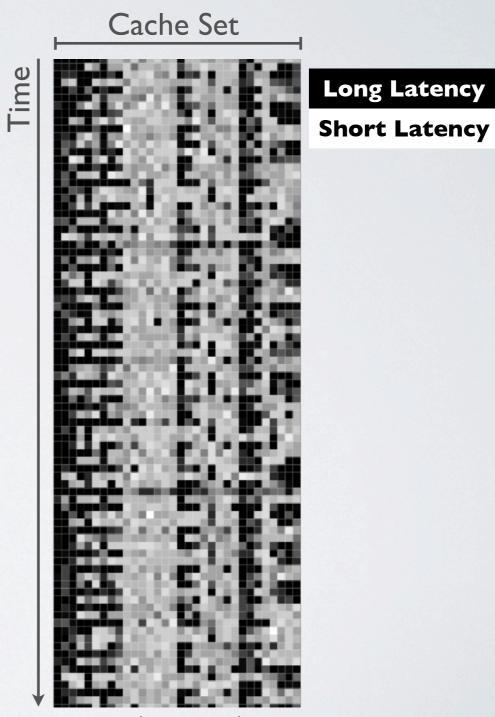
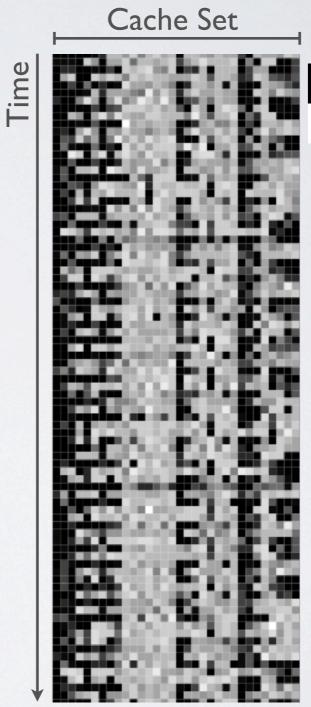


Image Credit: C. Percival 2005

Ĥ

I) Measure usage over time



Long Latency Short Latency

Image Credit: C. Percival 2005

I) Measure usage over time

2) Look for patterns

Cache Set Time

Long Latency Short Latency

I) Measure usage over time

2) Look for patterns

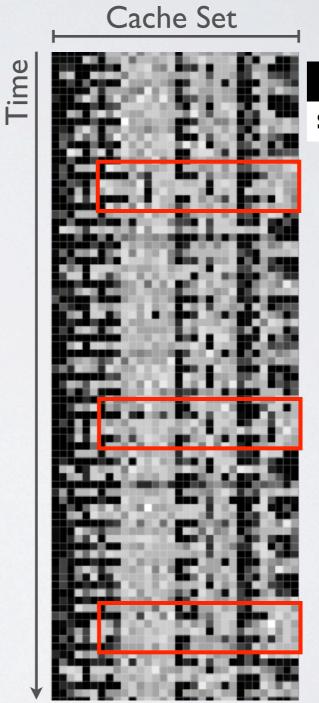
Cache Set Time

Long Latency Short Latency

I) Measure usage over time

2) Look for patterns

3) Find correlation to victim



Long Latency

**Short Latency** 

Image Credit: C. Percival 2005

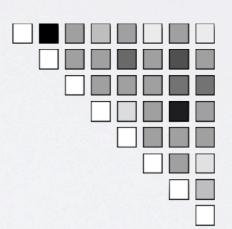
Measure

Analyze



Analyze

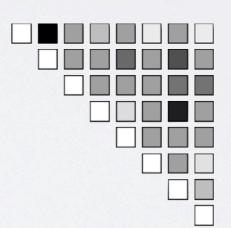




Analyze

#### Side Channel Trace



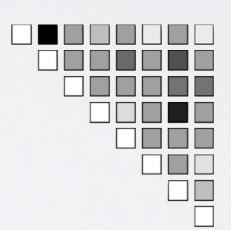


Analyze

#### Oracle Trace

#### Side Channel Trace





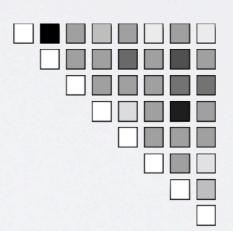
Analyze

#### Oracle Trace

#### Side Channel Trace



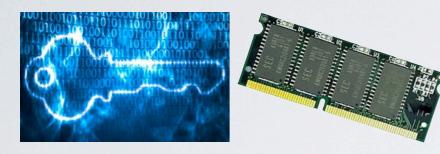




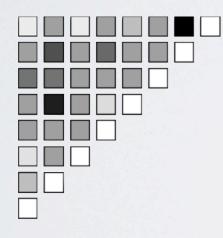
Analyze

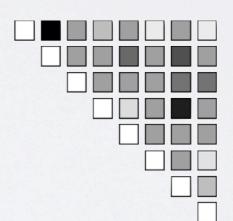
#### **Oracle Trace**

#### Side Channel Trace









Analyze

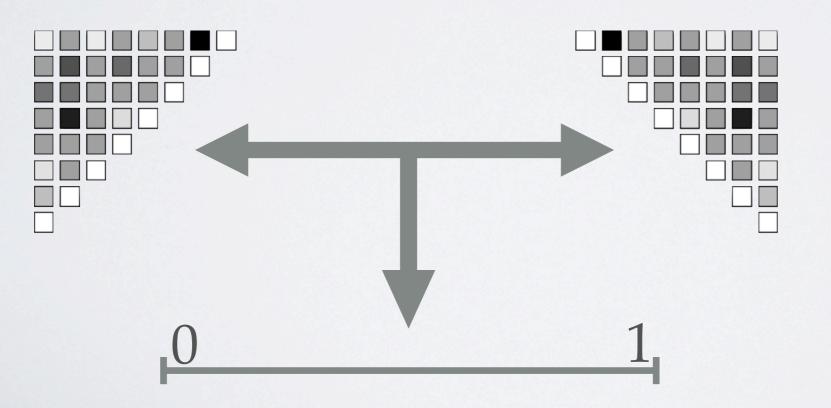
## Measuring Side Channels

#### **Oracle Trace**

### Side Channel Trace



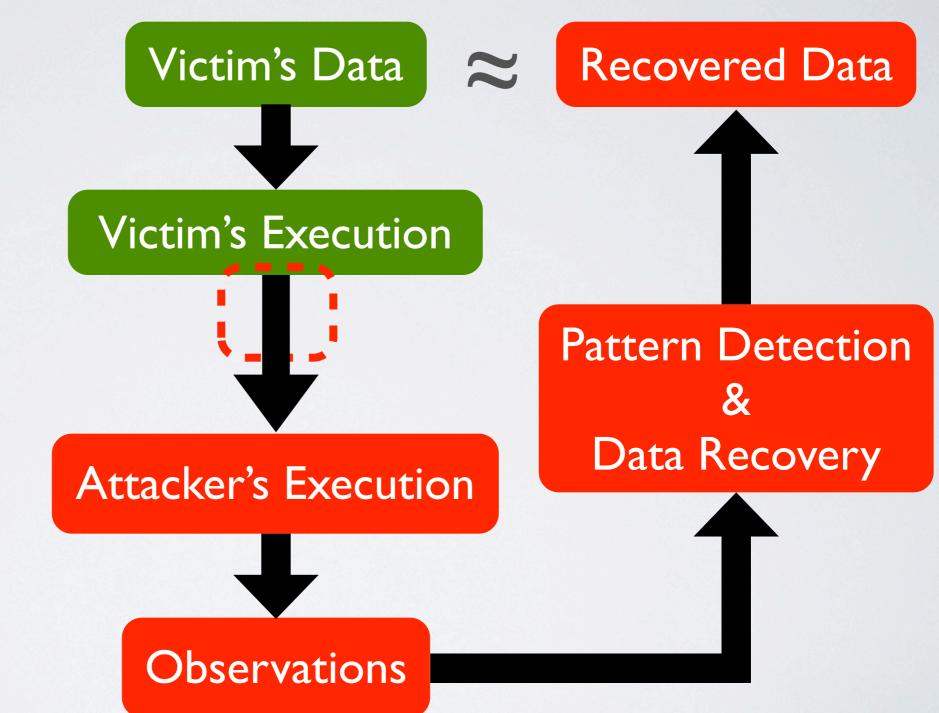
Measure

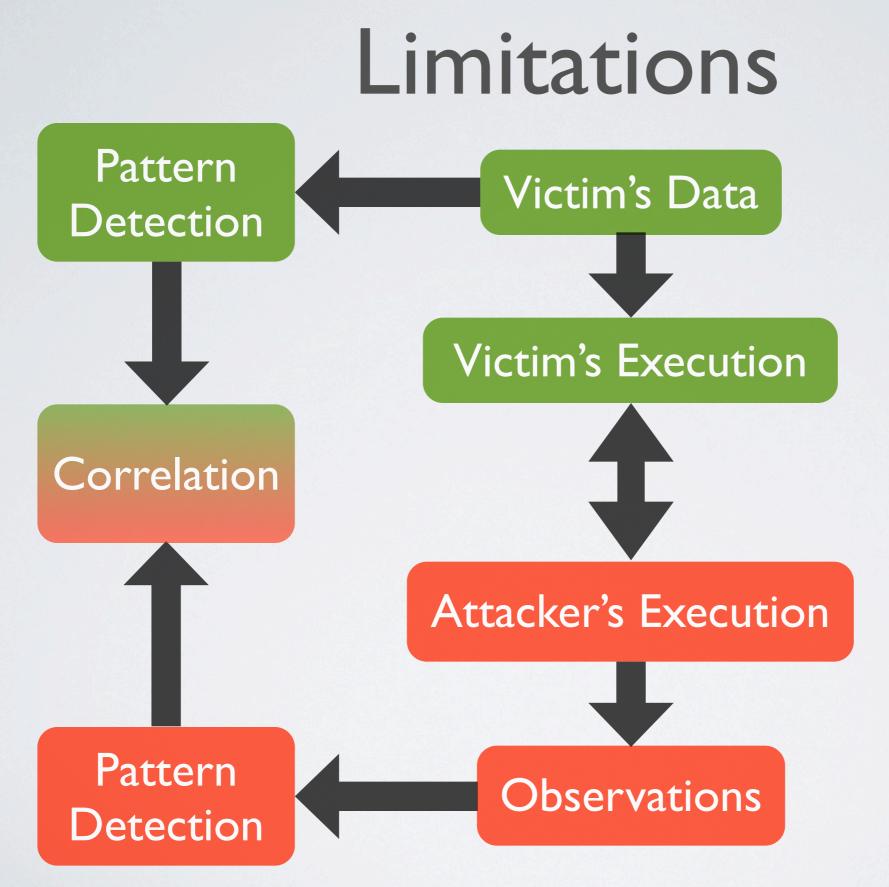


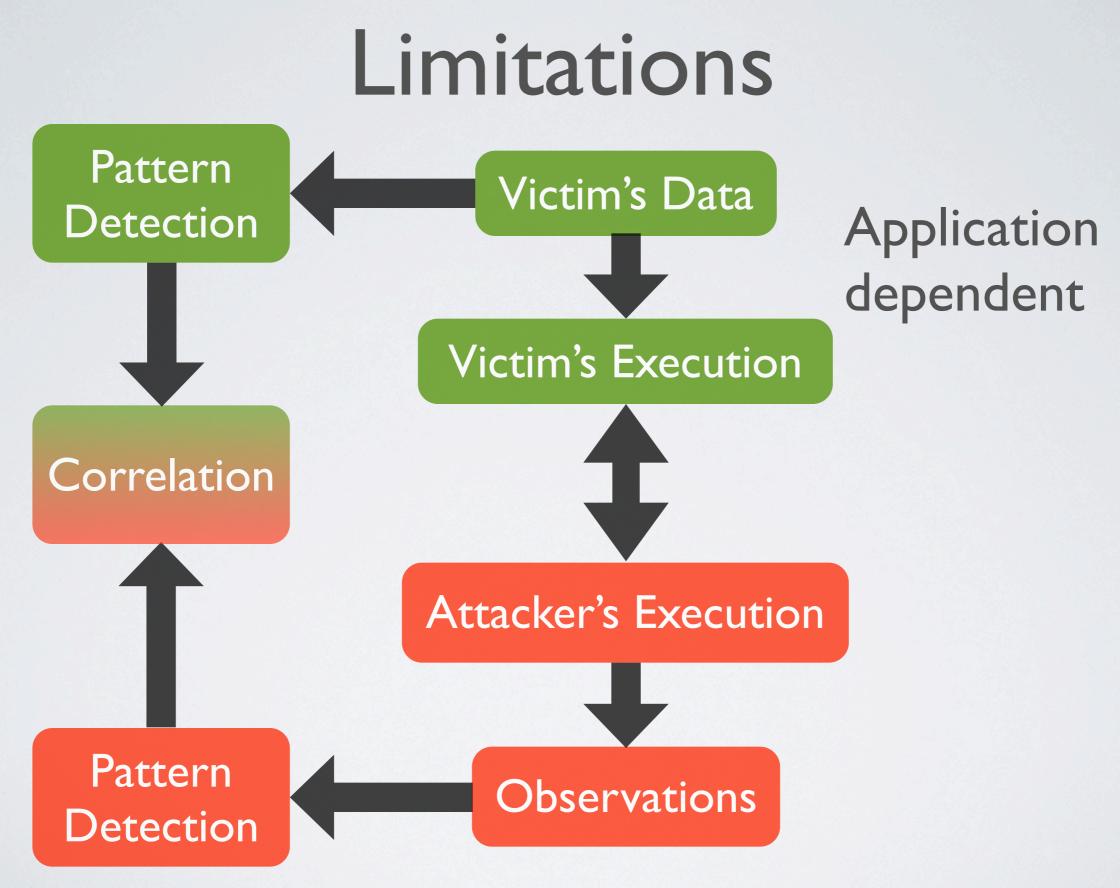
Analyze

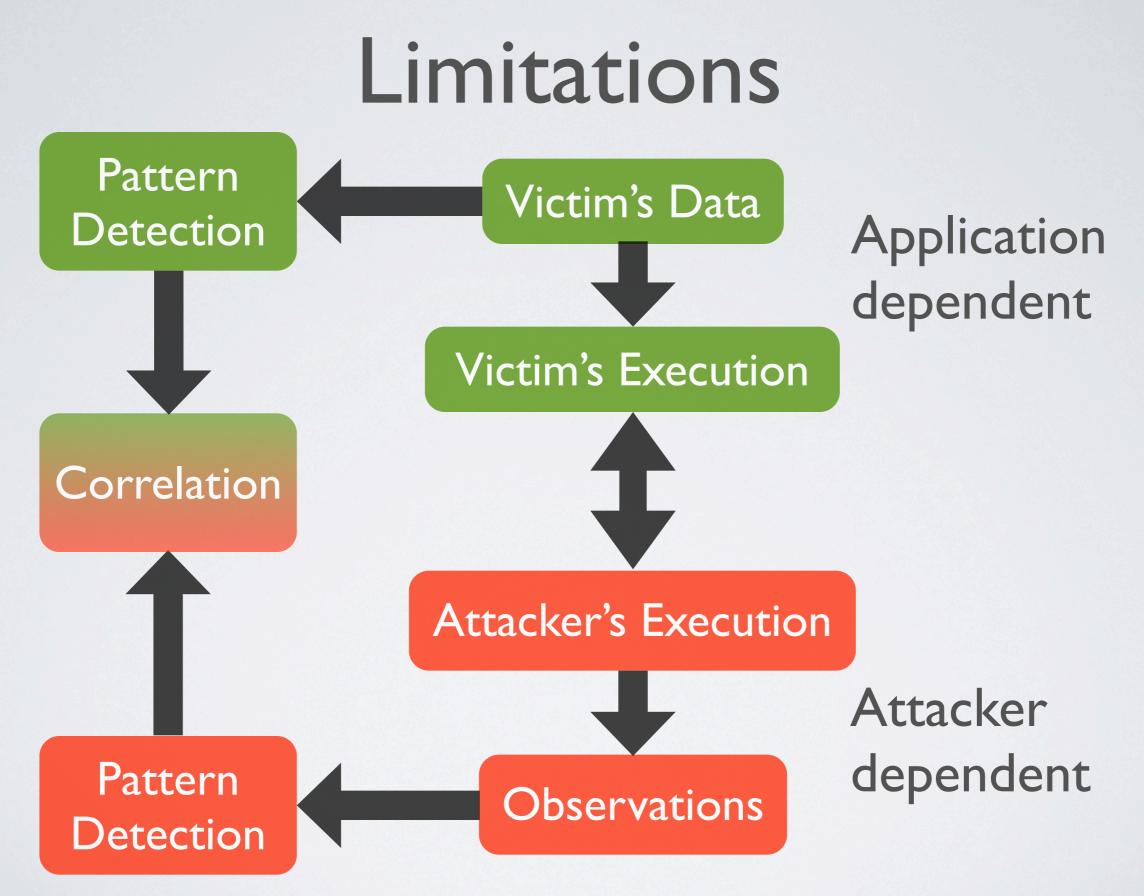
Correlate

### Generalizing Attacks

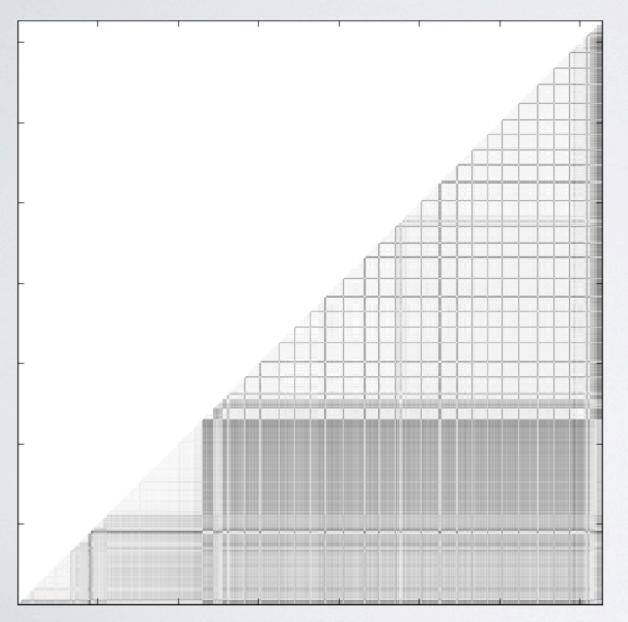




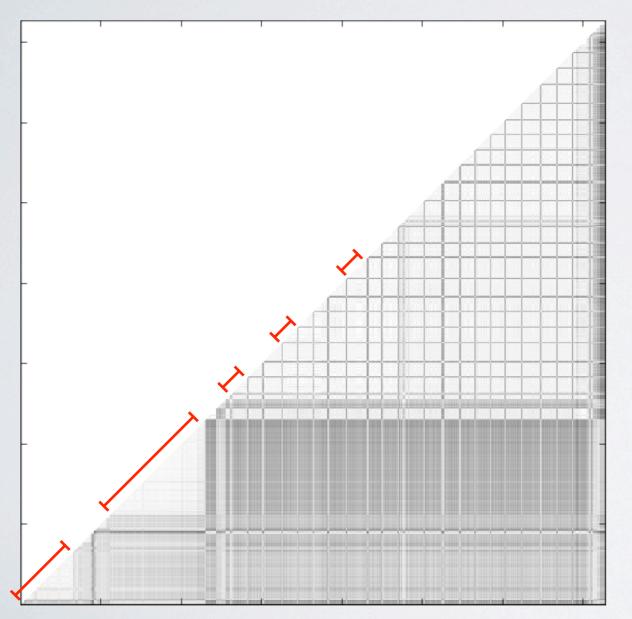




### Oracle

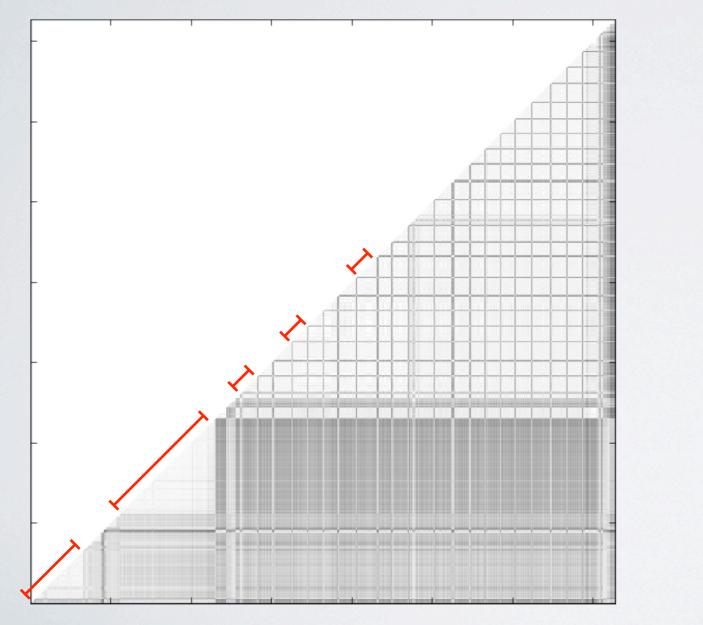


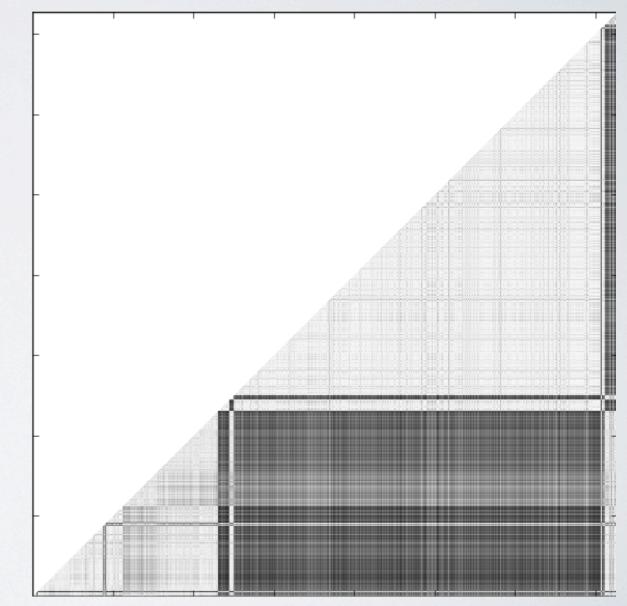
### Oracle



### Oracle

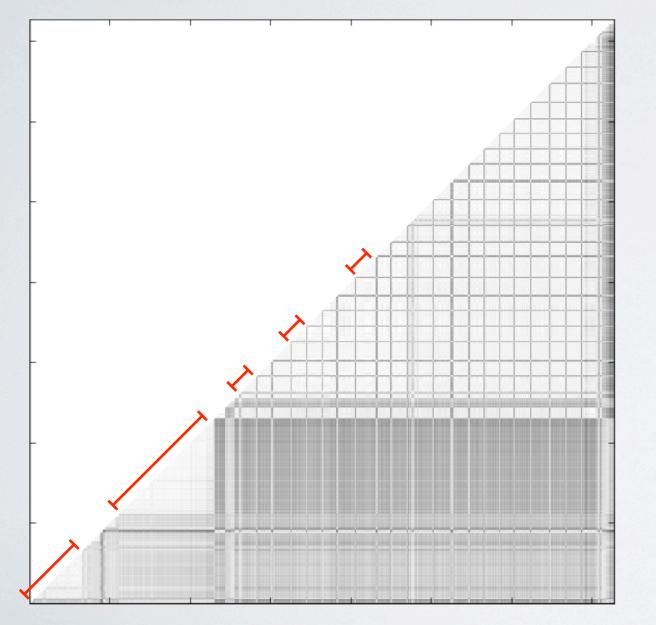
### Side Channel

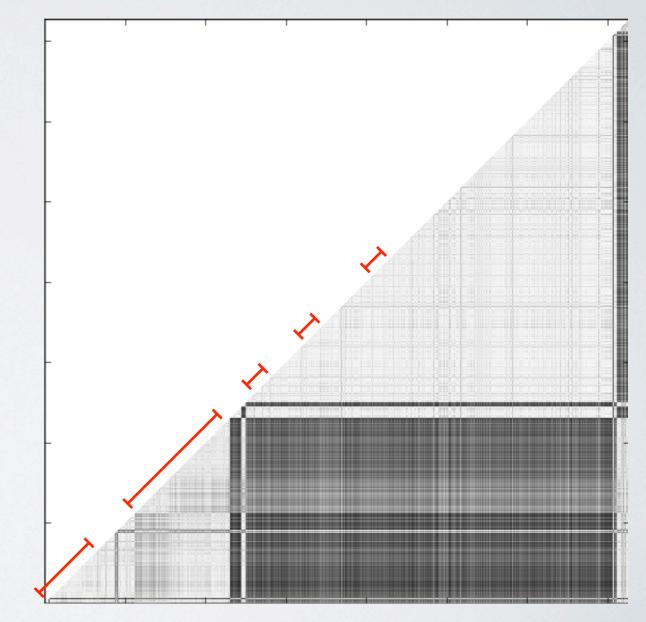




### Oracle

#### Side Channel

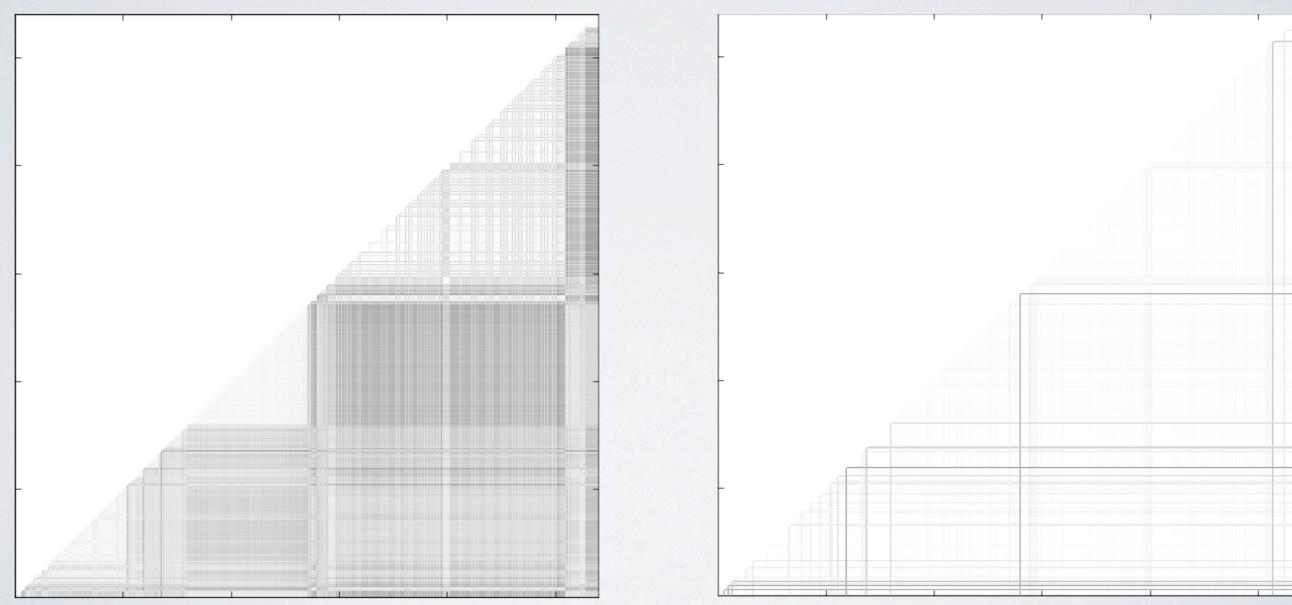




## Secure Example Matrices (0.098)

### Oracle

#### Side Channel



### Errata / Clarification

- We examine PRS with our policies, not RPCache
- This citation is wrong:
  - [16] Z. Wang and R. B. Lee. New cache designs for thwarting software cache-based side channel attacks. ISCA '07
- It should be:
  - [16] Z.Wang and R. B. Lee. Covert and side channels due to processor architecture. ACSAC '06

## Methodology

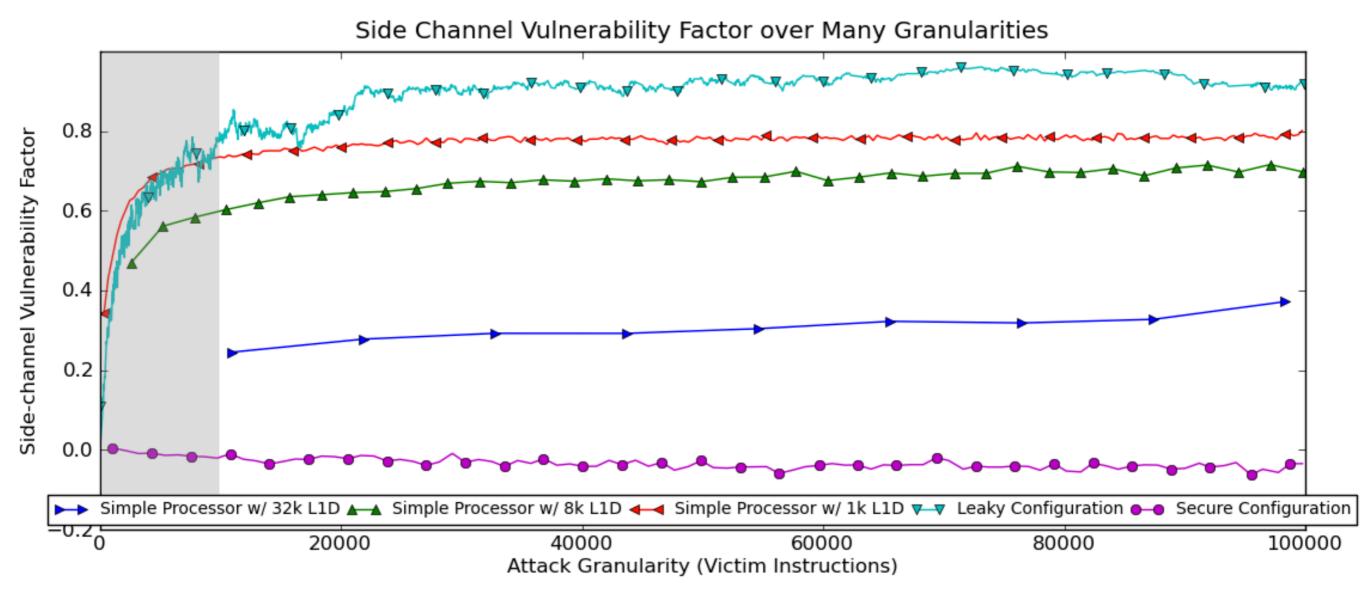
- Victim: OpenSSL 0.9.8k -- RSA Signing
  - Trace: memory location accesses
    - Indicates working set in memory
- Attackers
  - Cache Scanning Types
    - In order
    - Random
    - Random subset
  - Prefetcher
    - Has no effect on attacker, only victim
    - Operates on attacker and victim
  - Trace: latency to access each cache set

### **Simulation Parameters**

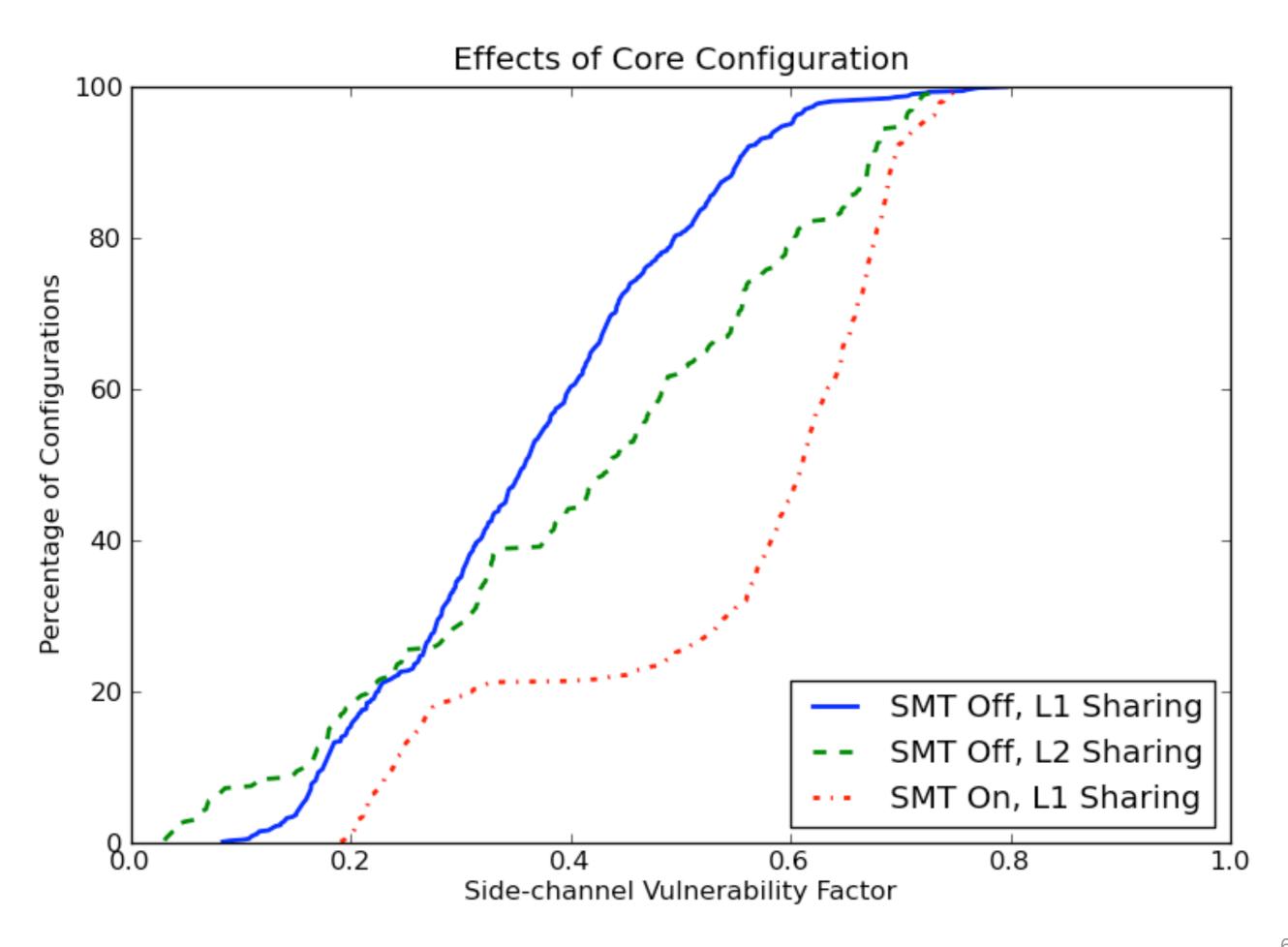
- SMT On/Off
- Cache sharing
   –L1 vs. L2
- Cache size
  -1k, 8k, 32k L1
  -8x L2, 256x L3
- Line size
   –8B, 64B
- Set associativity
  - -1, 4, and 8 way

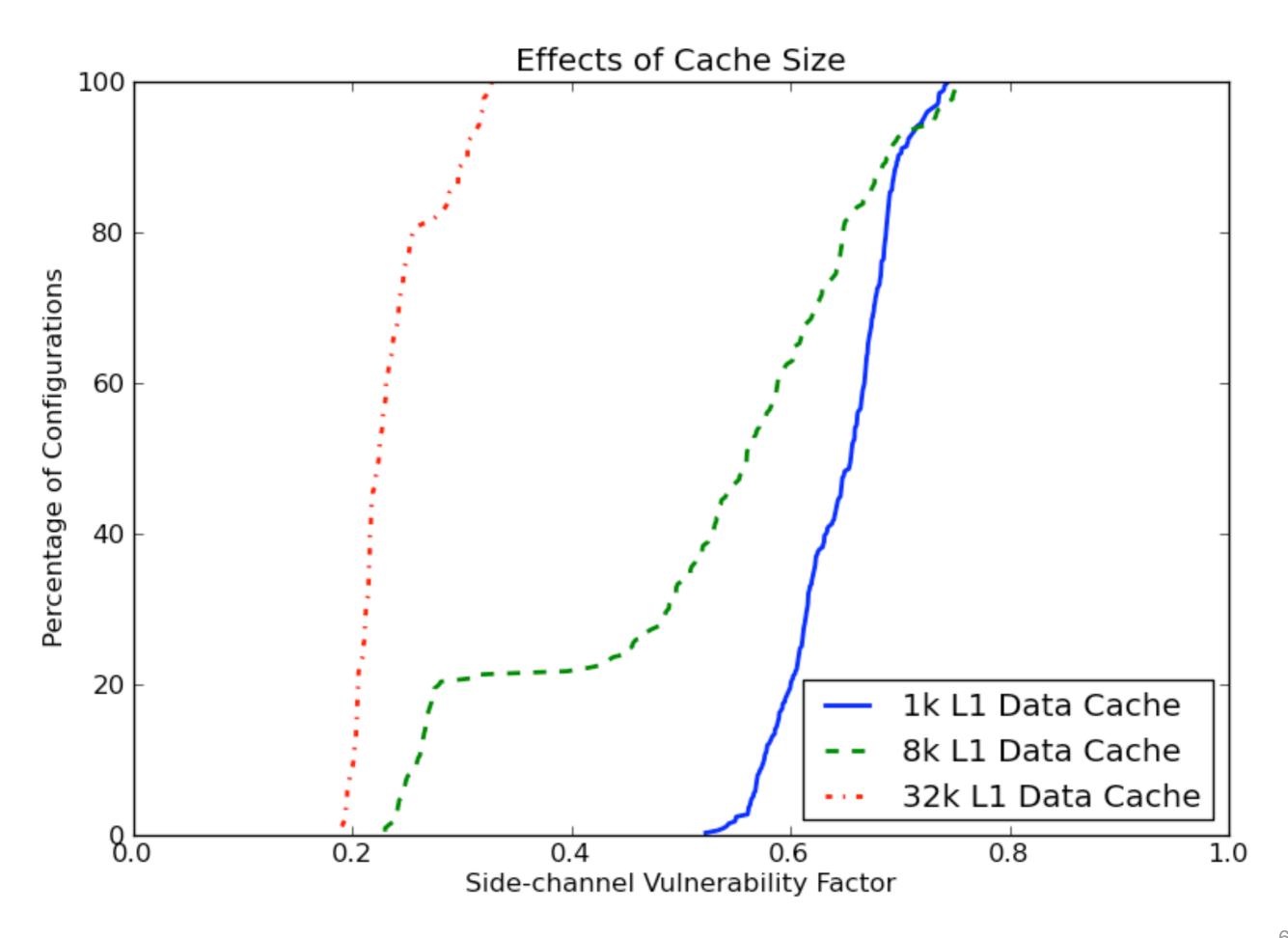
- Hashing Low bits, XOR, PRS
- Prefetching
   None, Next line, Arithmetic, GHB/PCCS, GHB/PCDC
- Cache Partitioning None, Split, Dynamic
- Random Eviction

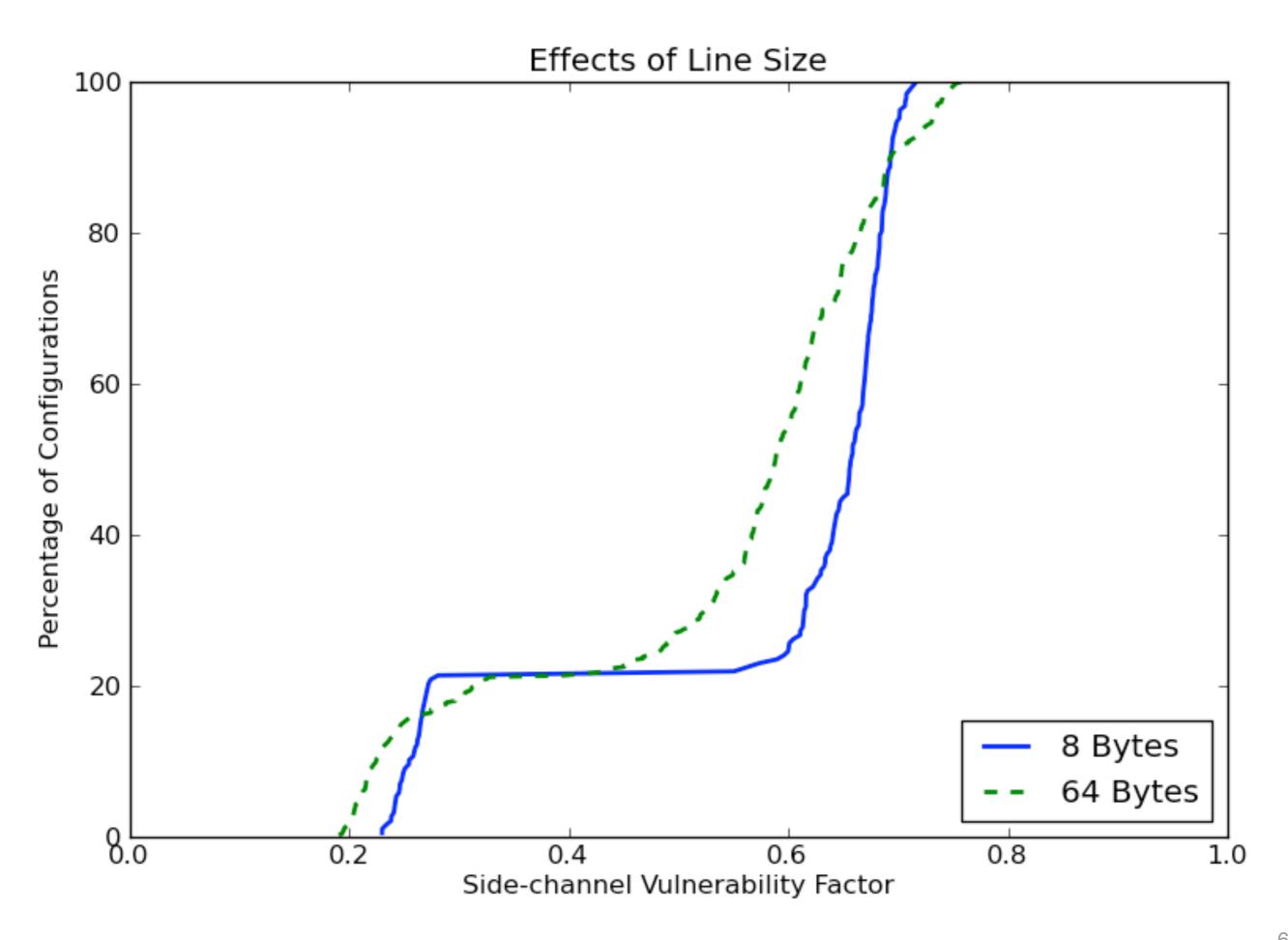
### **Example Results**

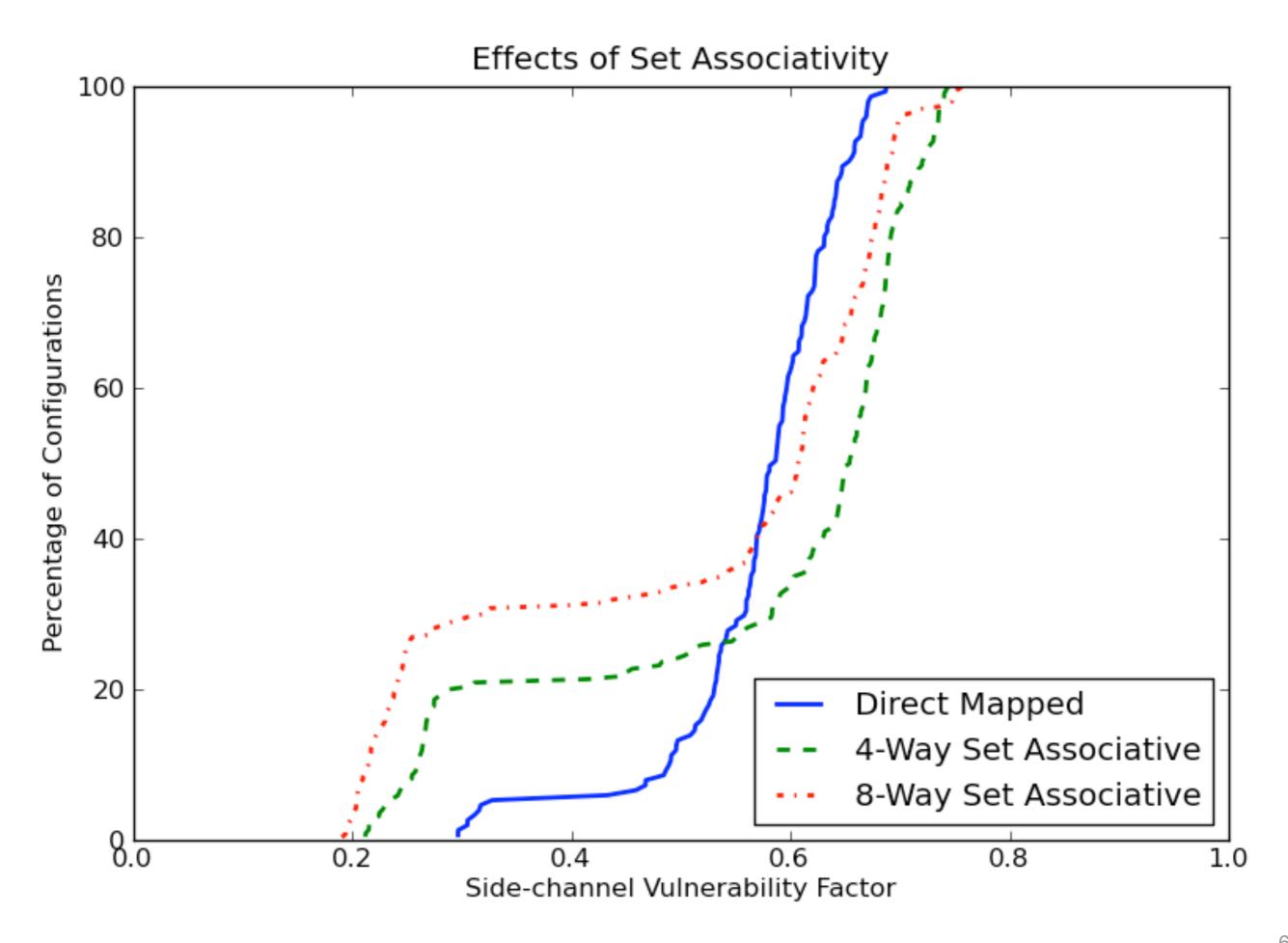


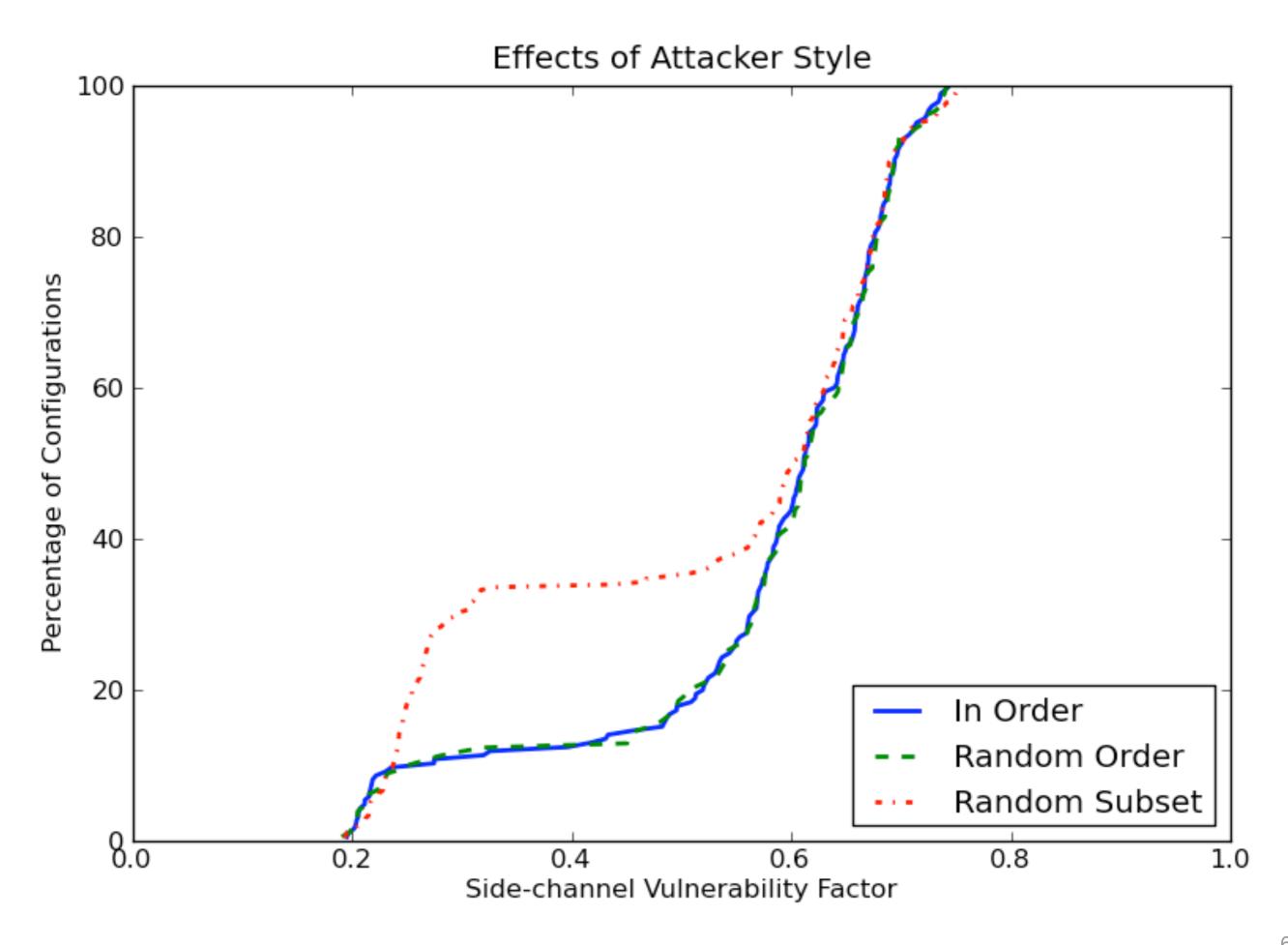
61

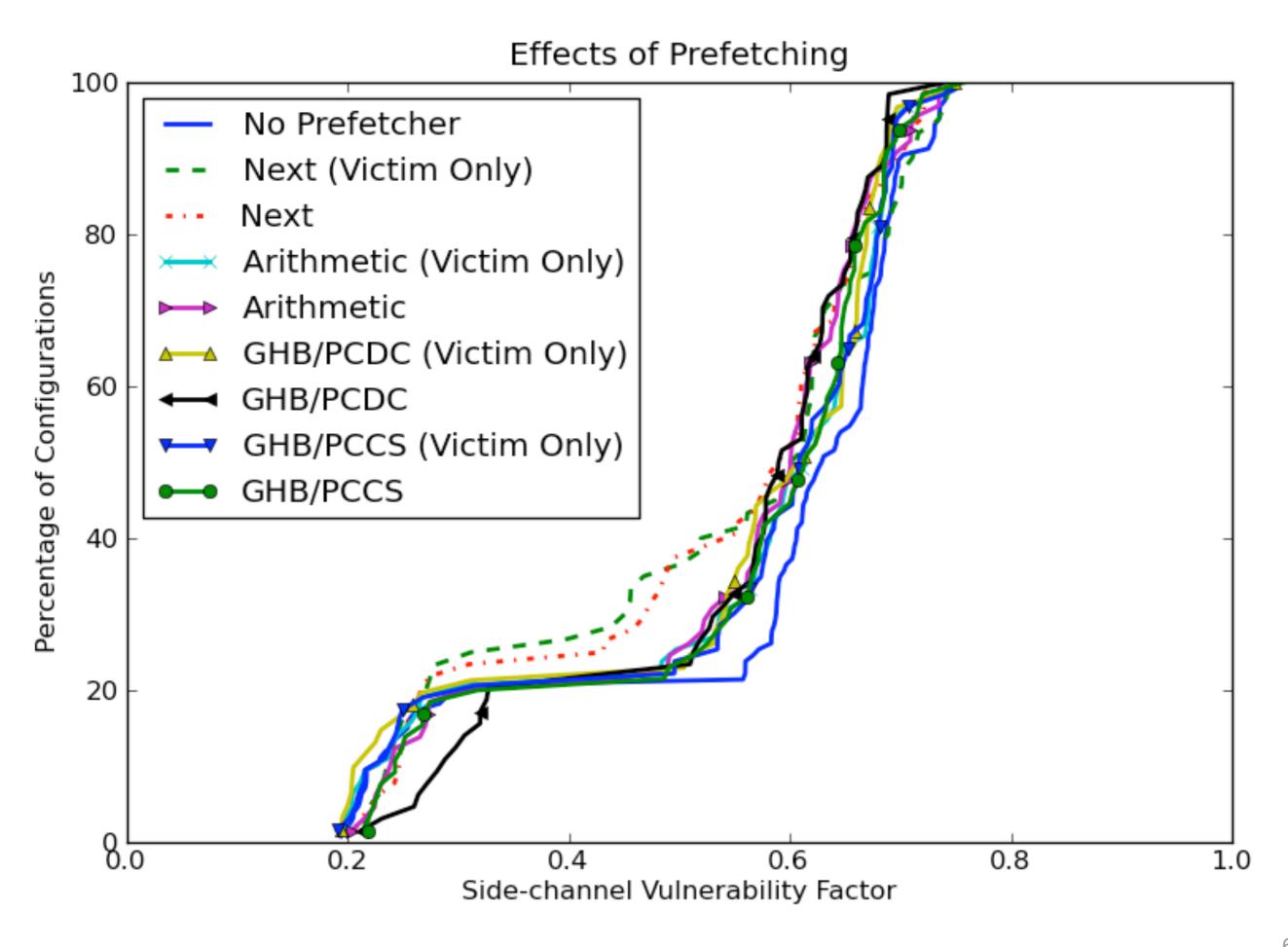




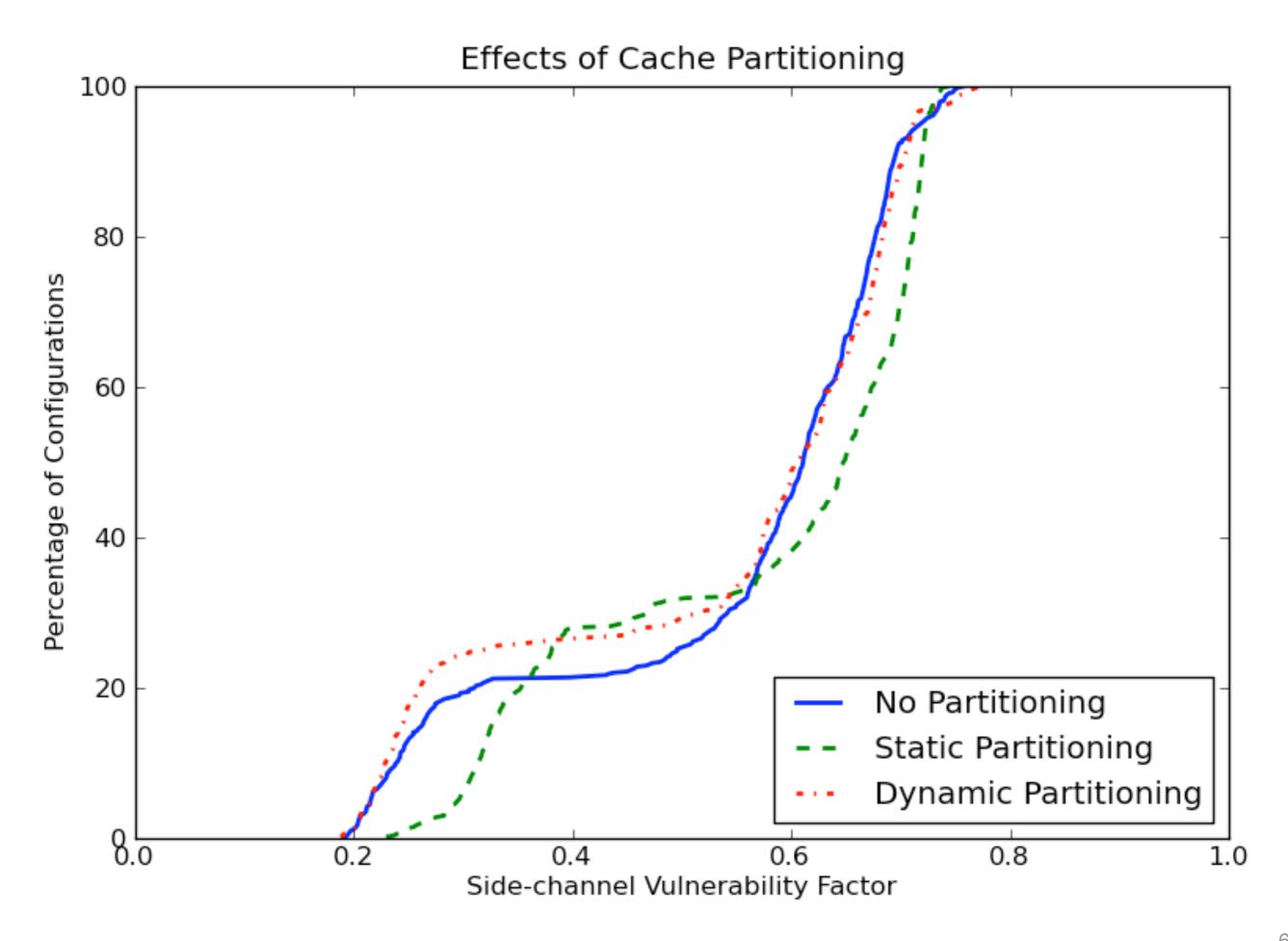


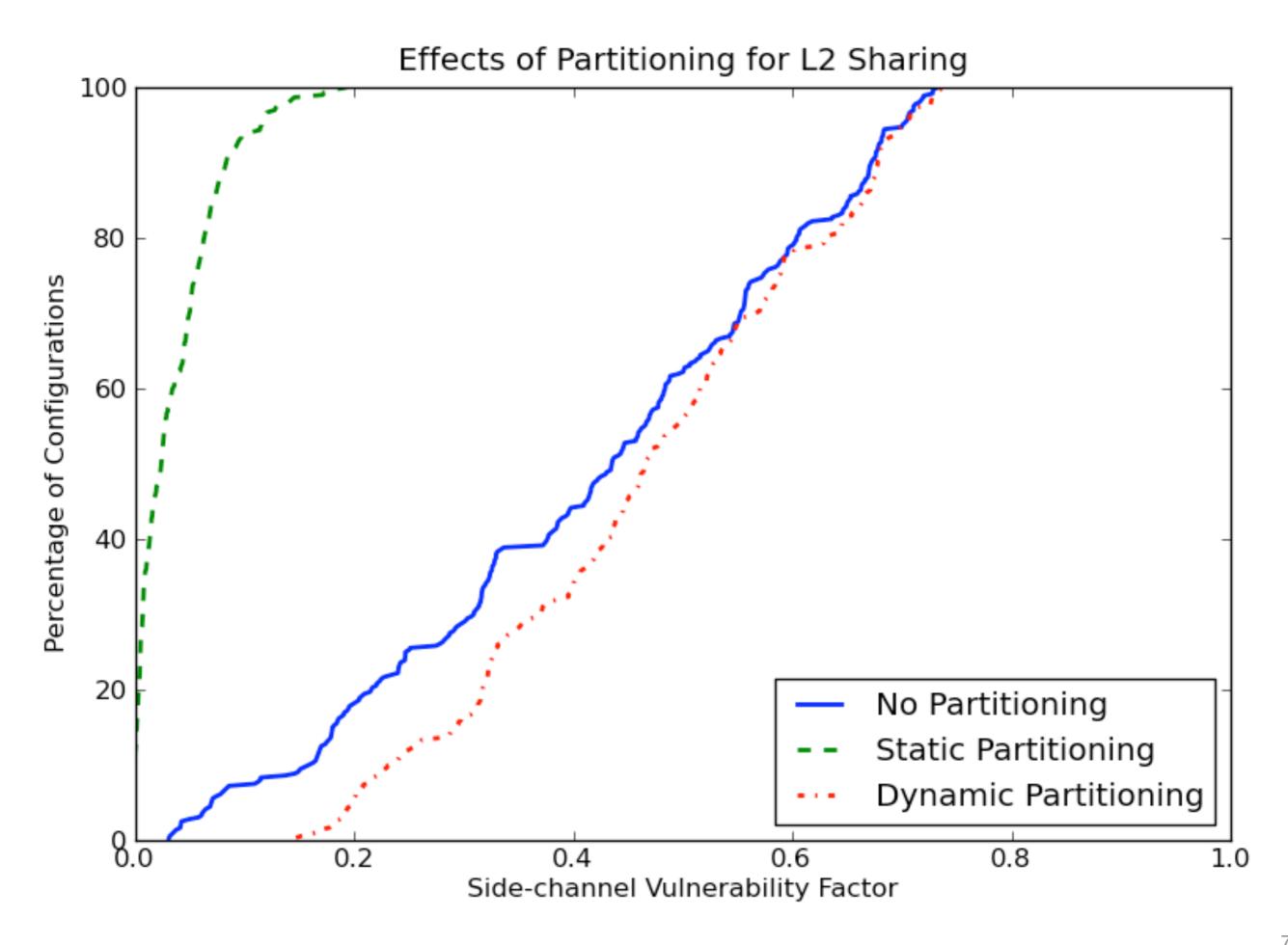


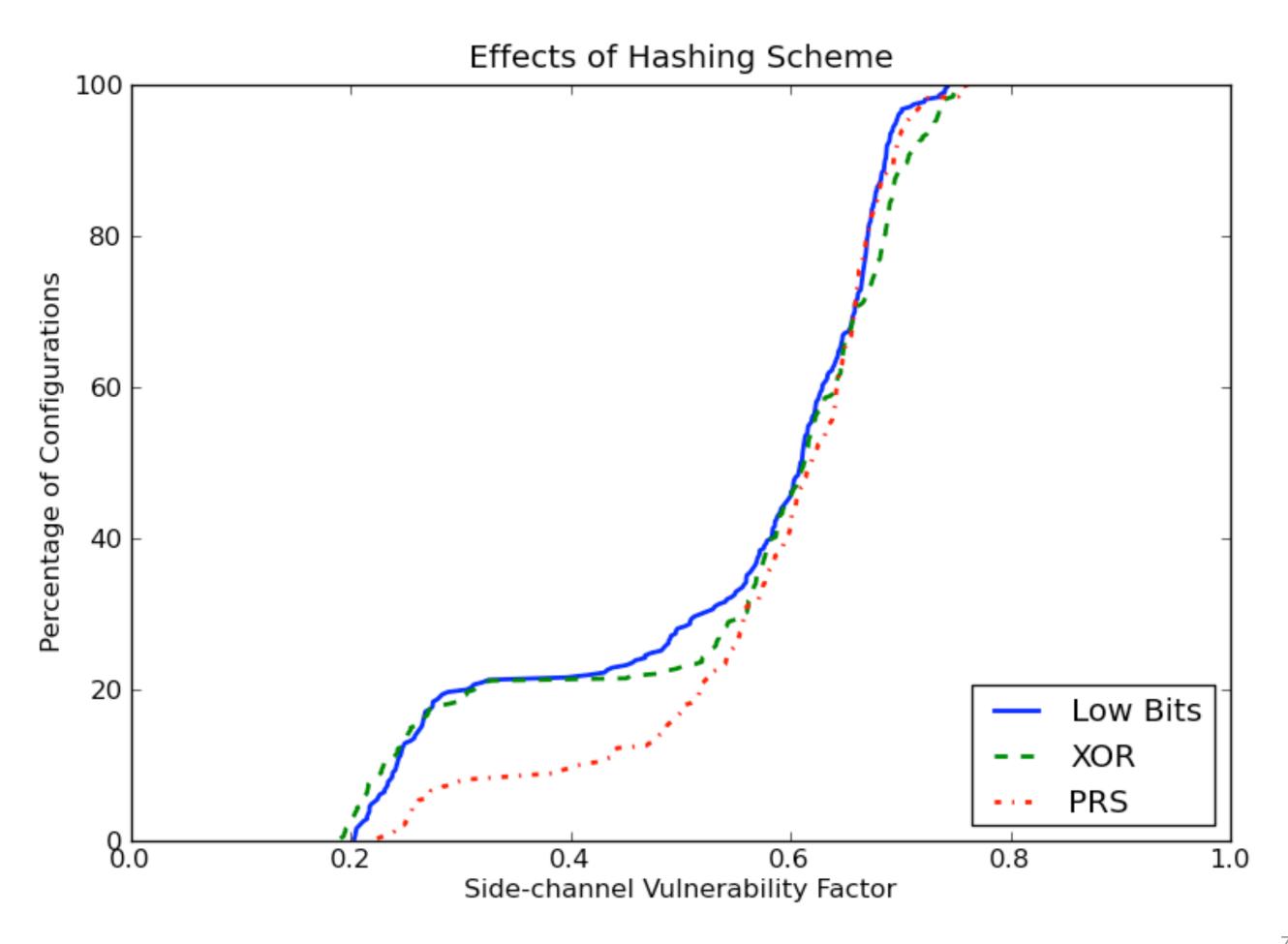


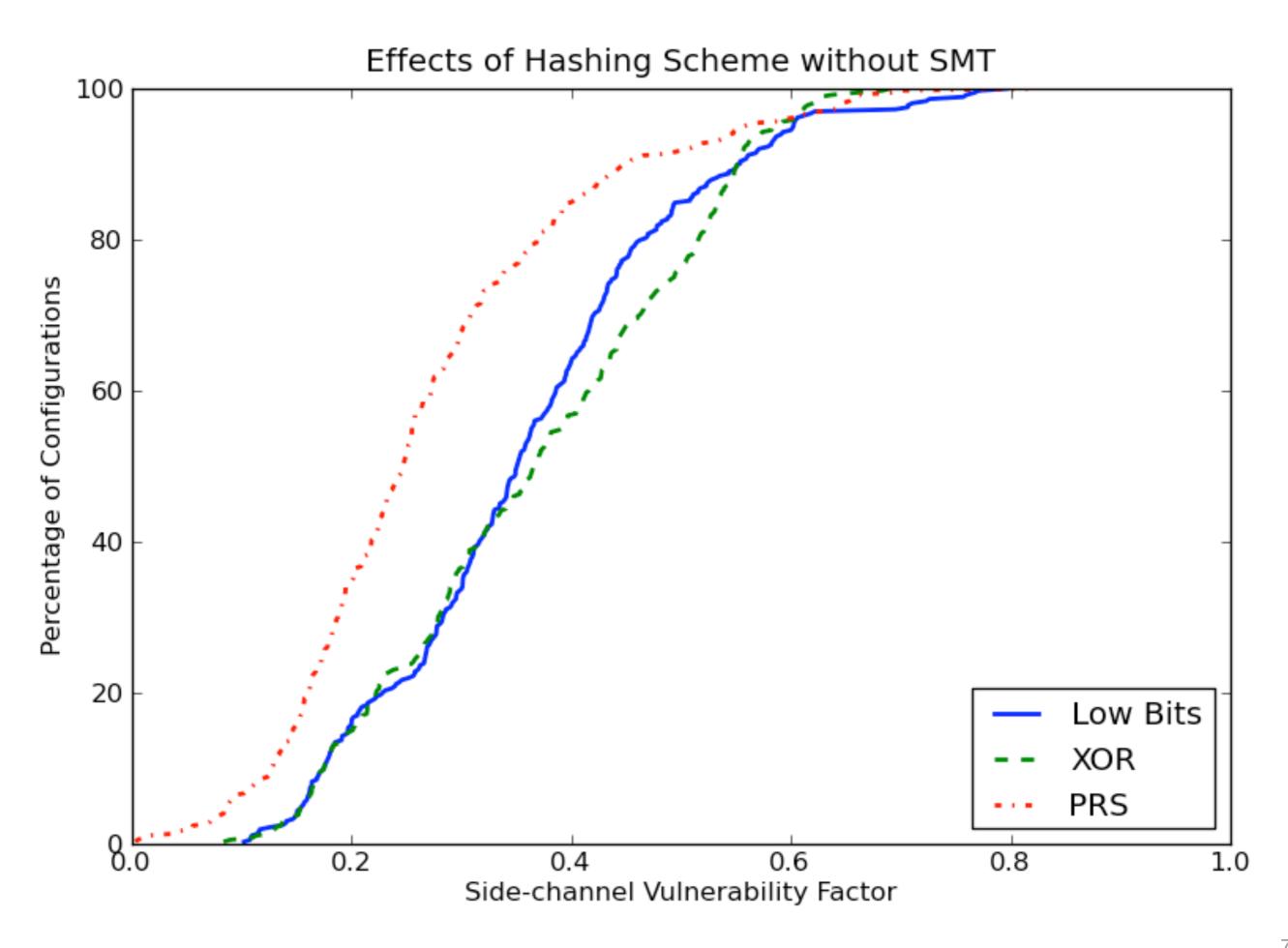


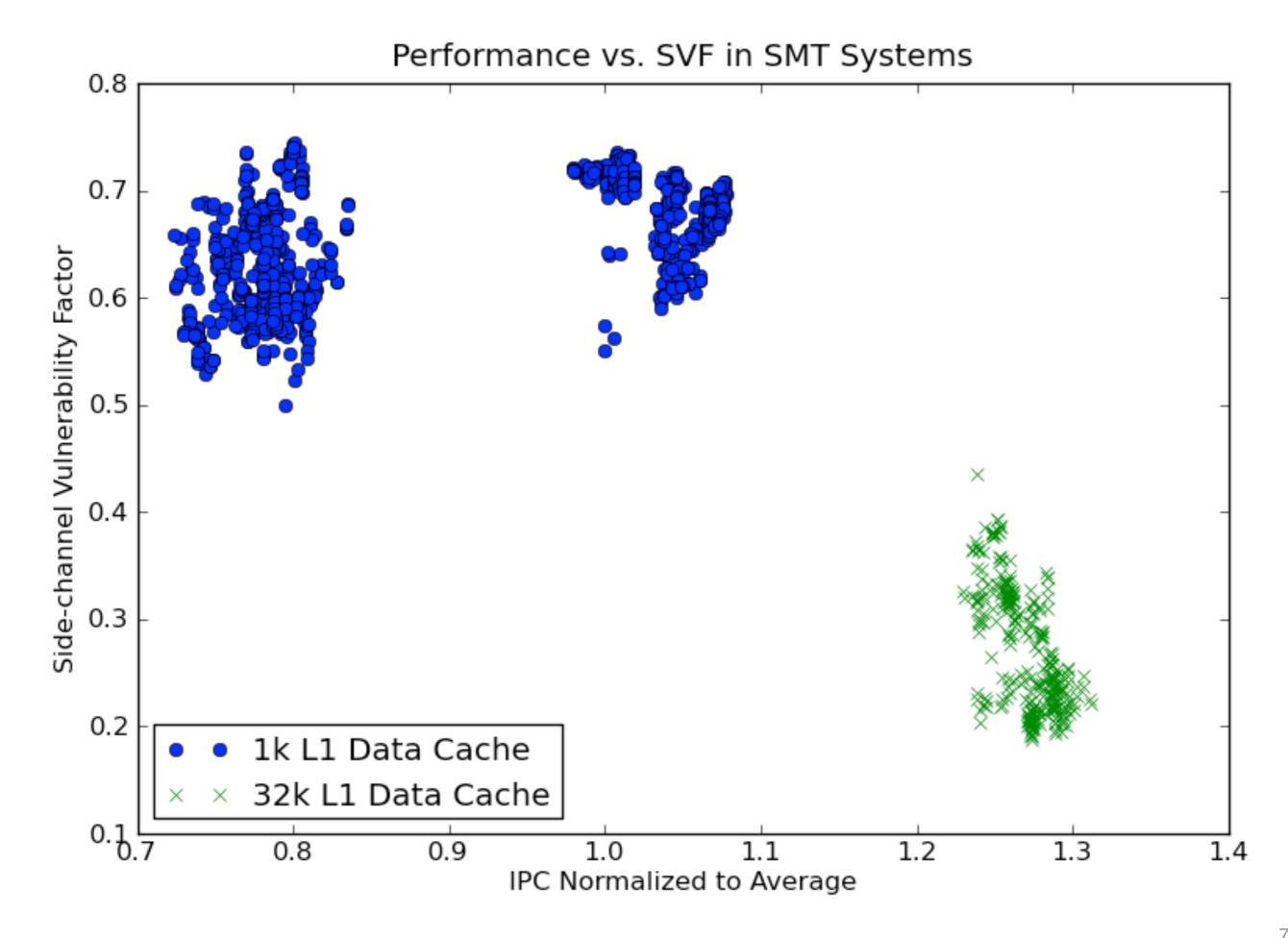


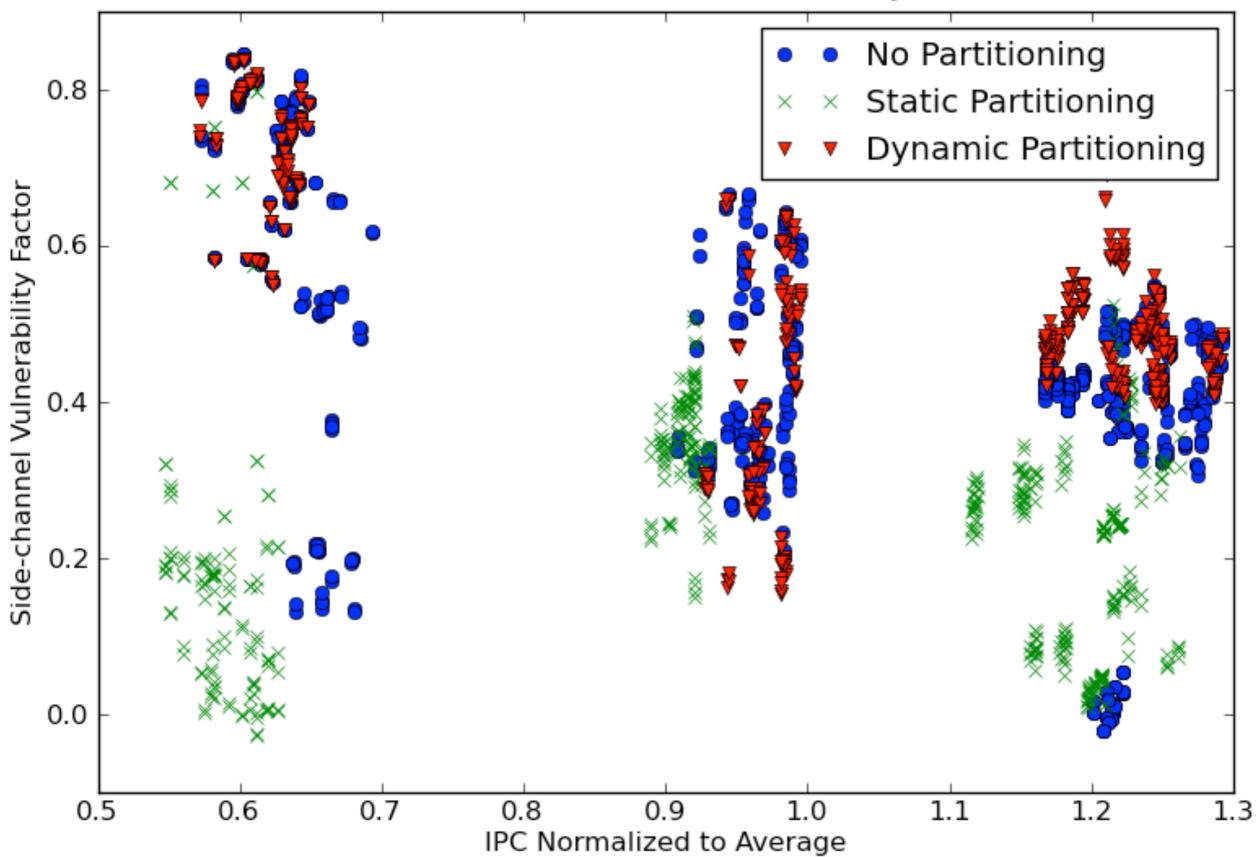












Performance vs. SVF in Non-SMT Systems