Guy Eichler

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Education

Columbia University in the City of New York *– New York, New York – Sep. 2018 – May 2025*

- **PhD in Computer Science,** Defended successfully in Feb. 2025 – Dissertation title: *"System-Level Design in the Era of Brain-Computer Interfaces"*
- **MSc in Computer Science**, Graduated Feb. 2020. GPA: 4.0/4.0
- **MPhil in Computer Science**, Graduated May 2022. GPA: 4.0/4.0
- **Teaching and Mentorship** – *CSEE W4868 System-on-Chip Platforms*: Fall 2019, Fall 2021. *CSEE E6868 Embedded Scalable Platforms*: Spring 2022-2024.

Technion – Israel's Institute of Technology – *Haifa, Israel – Oct. 2012 – Dec. 2016*

- **BSc in Electrical Engineering,** Graduated Dec. 2016. GPA: 88/100

Honors & Awards

- ***Columbia – The Andrew P. Kosoresow Memorial Award*** for Excellence in Teaching and Service (2022).
- ***Technion – Dean's List*** for outstanding academic achievements (2014, 2015, 2016).
- **CPS-IoT Week 2023 –** ***Best Presentation Award*** – Real Time and Intelligent Edge Computing Workshop (RAGE)
- **Design Automation and Test in Europe (DATE) 2025** – **PhD Forum Award for Best Poster** – Presenting the PhD dissertation

Programming Skills and Tools

Code Languages - C, C++, SystemC**,** Python**,** Verilog, System Verilog.
Tools - Vivado, Catapult HLS, Stratus HLS, Vivado high-level synthesis (HLS), Jupyter Notebooks, GitHub, FPGA, ASIC, MATLAB, Eclipse, PYNQ, RISC-V.

Research Projects

Columbia University in the City of New York – *Computer Science Department – System Level Design group (SLD)*

- Developed digital circuits in Verilog and SystemVerilog for **implantable brain-computer interface (BCI) systems** that integrate large-scale data acquisition through thousands of sensors and wireless communication. Designed microcontrollers targeting electrocorticography (ECoG), and optogenetic-based single-photon avalanche diodes (SPAD) and LEDs. Participated in **multiple ASIC chip tapeouts** and **in-vivo experiments** on non-human primates. Developed **embedded hardware-software infrastructure** using Verilog, SystemC and Python for **FPGA-based wearables** to interact seamlessly with implantable devices.
- Implemented **artificial intelligence (AI) and machine-learning (ML) hardware accelerators** in Verilog, SystemC and HLS and integrated them in **heterogeneous system-on-chip (SoC) architectures**. Focused on accelerating BCI applications and optimizing for **low power, high speed and energy efficiency for IoT and edge devices**. Developed software applications in C and C++ to run on **RISC-V CPUs in embedded FPGA devices**.
- **Over 10 published papers** in top venues including: VLSI symposium, DATE, DAC, CICC, ICCD, IEEE Micro (**publications on the next page**)
- **Two provisional patent applications**

Technion – Israel's Institute of Technology – *Electrical Engineering Department*

- Majored in Computer Architectures, Signals & Image Processing and Biological Signals & Systems.
- Conducted two final projects: (1) **Mapping the Hodgkin-Huxley action potential model** through the design of a simulation tool in MATLAB to investigate combinations of different model parameters, (2) **Developing an IoT device for real-time ECG signal processing** using sensors, Arduino, C programming and a mobile Android device.

Work Experience

Arm *– Architecture Research Intern* **–** *Austin, Texas – Summer 2022*

- Explored the design-space of interconnects using Catapult HLS for emerging Network-on-Chip (NoC) designs in future Arm processing systems.

IBM – *Hardware Design and Verification Engineer – Haifa, Israel – 2015-2018*

- Developed and verified logic for superscalar, multicore processors using Linux, Eclipse, and C++ programming – **IBM POWER9 and POWER10** – focused on verifying address translation components and interfaces with external accelerators (openCAPI).
- Contributed to the early development of **cutting-edge programmable machine-learning (ML) accelerators** – IBM Sentient AI.

Elbit Systems – *Application Developer – Netanya, Israel – 2011-2012*

- Designed software applications with an in-house custom tool for data analysis designated for intelligence organizations.
- Coordinated between multiple teams including system engineering, software engineering, and clients in order to constantly improve **product design**.

Military Service

Israel Intelligence Corps – Unit 8200 *– Squad Leader – 2008-2011*

- Led a team of 11 soldiers to analyze special intelligence in real-time. Managed shifts of up to 25 people. Conducted large-scale project management and data analysis in a highly sophisticated technological environment with many software tools, requiring a high degree of multitasking.

Miscellaneous

Languages: Fluent: English, Hebrew. Conversational: Spanish, Arabic.

Volunteering: Magen David Adom **–** First Aid, Think Positive **–** Math and English tutor, ATID – Mentor for high-school children.

Hobbies: Table tennis, HIIT, functional training, yoga, books.

Publications

- "An Energy-Efficient Kalman Filter Architecture with Tunable Accuracy for Brain-Computer Interfaces", ACM/IEEE Design Automation Conference (DAC), June 2025 (to be published).
- "KalmMind: A Configurable Kalman Filter Design Framework for Embedded Brain-Computer Interfaces", Design Automation and Test in Europe (DATE), April 2025 (to be published).
- "WOLT: Transparent Deployment of ML Workloads on Lightweight Many-Accelerator Architectures", IEEE International Conference on Computer Design (ICCD), November 2024.
- "OPEN-CFR: Open-source Co-design Framework for Redundancy with DPR in COTS FPGA SoCs", IEEE Space Computing Conference (SCC), July 2024.
- "Stable, Chronic In-Vivo Recordings from a Fully Wireless Subdural-Contained 65,536-Electrode Brain-Computer Interface Device", bioArxiv, May 2024.
- "A Wireless Subdural Optical Cortical Interface Device with 768 Co-Packaged Micro-LEDs for Fluorescence Imaging and Optogenetic Stimulation", IEEE Custom Integrated Circuits Conference (CICC), April 2024.
- "MindCrypt: The Brain as a Random Number Generator for SoC-Based Brain-Computer Interfaces", IEEE International Conference on Computer Design (ICCD), November 2023.
- "SpikeHard: Efficiency-Driven Neuromorphic Hardware for Heterogeneous Systems-on-Chip," ACM Transactions on Embedded Computing Systems (TECS), September 2023.
- "A Wireless, Mechanically Flexible, 25μm-Thick, 65,536-Channel Subdural Surface Recording and Stimulating Microelectrode Array with Integrated Antennas," IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), June 2023.
- "EigenEdge: Real-Time Software Execution at the Edge with RISC-V and Hardware Accelerators," ACM Cyber-Physical Systems and Internet of Things Week (CPS-IoT), May 2023.
- "MasterMind: Many-Accelerator SoC Architecture for Real-Time Brain-Computer Interfaces," IEEE International Conference on Computer Design (ICCD), October 2021.
- "Accelerator Integration for Open-Source SoC Design," IEEE Micro, April 2021.
- "Ariane + NVDLA: Seamless Third-Party IP Integration with ESP", Workshop on Computer Architecture Research with RISC-V (CARRV), May 2020.