GABRIELE TOMBESI

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EDUCATION

Columbia University, New York City (GPA 3.97/4) *January 2021 - Present*
PhD in Computer Science

Turin Polytechnic-INP-EPFL, Turin / Grenoble / Lausanne *October 2018 - October 2020*
M.S in Micro and Nano Technologies for Integrated Systems.

Polytechnic of Turin, Turin,Italy *September 2015 - October 2018*
Bachelor of Physical Engineering

TECHNICAL STRENGTHS

EDA	**Profiecient:**Catapult HLS, Modelsim, Vivado, Stratus HLS, **Familiar:** Design Compiler, Virtuoso
HDL	VHDL, Verilog
Languages	C, C++, SystemC, Python, SQL, Bash
Libraries	TensorFlow and PyTorch

RELEVANT COURSEWORK

Digital Design	HDL Modeling, full/semi-custom EDA Labs, VLSI design
Machine Learning	Deep Learning, Convex and non-Convex optimization, Hyperparameter tuning
Nanotechnology	Nanomaterial synthesis and characterization , Litography, MEMS, Solid state physics

EXPERIENCE

Columbia University *January 2021 - Present*
Graduate Research Assistant (Advised by Prof. Luca Carloni)

- **ESP**: One of the lead developers of ESP, an open-source platform for heterogeneous system-on-chip design. Integrated Catapult HLS SystemC design flow with latency-insensitive MatchLib library into ESP.
- **TDU Implementation**: Implemented a Tile Debug Unit (TDU) for modular validation in 12nm SoCs, facilitating efficient chip bring-up for multi-application systems.
- **Convolutional NN Acceleration**: Developed baremetal and Linux apps to execute CNN inference tasks using Conv2D and GeMM accelerators on a reconfigurable SoC.
- Conducting research in computer architecture, specifically on tiled hardware accelerators for deep learning, with a focus on innovative intra-layer parallelism and inter-layer pipelining techniques.

COLUMBIA UNIVERSITY, New York City, NY *September 2022 - December 2022*
Teaching Assistant (System-on-Chip Platforms - CSEE 4868) *September 2023 - December 2023*

- Collaborated to develop course content for a System-on-Chip class, with a focus on Conv2D accelerator design in HLS.
- Led Stratus-HLS to Catapult-HLS transition, reshaping assignments, handouts, and grading processes for SystemC modeling, HLS and RTL simulation.
- Delivered lectures in latency-insensitive Matchlib Library and HLS techniques for Catapult HLS.

COLUMBIA UNIVERSITY, New York City, NY *March 2020 - October 2020*
Master Thesis intern

- Formulated a novel design-for-testing strategy for NoC-based heterogeneous SoCs.
- Designed a debug unit based on this strategy in VHDL and integrated it into ESP.

IBM-Almaden research center, San Jose, CA *June 2019 - September 2019*
Summer Research intern

- Processed and characterized vacuum-deposited Metal-Oxide-Semiconductor films for gas sensing.
- Explored annealing treatments to achieve orthogonal responses to different volatile compounds.
- Analyzed electronic transport trends to guide further materials development.

PUBLICATIONS

SoCProbe: Compositional Post-Silicon Validation of Heterogeneous NoC-Based SoCs
Gabriele Tombesi, Joseph Zuckerman, Paolo Mantovani, Davide Giri, Maico Cassel Dos Santos, Tianyu Jia, David Brooks, Gu-Yeon Wei, Luca P Carloni.
In *IEEE Design & Test 2023 - NOCS'23 Special Issue* - **Best Paper Award**

DECADES: A 67mm2, 1.46TOPS, 55 Giga Cache-Coherent 64-bit RISC-V Instructions per second, Heterogeneous Manycore SoC with 109 Tiles including Accelerators, Intelligent Storage, and eFPGA in 12nm FinFET
Fei Gao, Ting-Jung Chang, Ang Li, Marcelo Orenes-Vera, Davide Giri, Paul J Jackson, August Ning, Georgios Tziantzioulis, Joseph Zuckerman, Jinzheng Tu, Kaifeng Xu, Grigory Chirkov, **Gabriele Tombesi**, Jonathan Balkind, Margaret Martonosi, Luca Carloni, David Wentzlaff.
In *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), 2023*

A 12nm Agile-Designed SoC for Swarm-Based Perception with Heterogeneous IP Blocks, a Reconfigurable Memory Hierarchy, and an 800MHz Multi-Plane NoC
Tianyu Jia, Paolo Mantovani, Maico Cassel Dos Santos, Davide Giri,Joseph Zuckerman,Erik Jens Loscalzo, Martin Cochet, Karthik Swaminathan, **Gabriele Tombesi**, Jeff Jun Zhang, Nandhini Cahndromoorthy, John-David Wellman, Kevin Tien, and Luca P. Carloni
In *Proceedings of the European Conference on Solid-State Circuits (ESSCIRC), 2022.*

A Scalable Methodology for Agile Chip Development with Open-Source Hardware Components.
Maico Cassel Dos Santos, Tianyu Jia, Martin Cochet, Karthik Swaminathan, Joseph Zuckerman, Paolo Mantovani, Davide Giri, Jeff Jun Zhang, Erik Jens Loscalzo, **Gabriele Tombesi**, Kevin Tien, Nandhini Chandramoorthy, John-David Wellman, David Brooks, Gu-Yeon Wei, Kenneth Shepard, Luca Carloni, and Pradip Bose.
In *Proceedings of the IEEE International Conference on Computer-Aided Design (ICCAD), 2022.*

TUTORIALS

Design, Programming, and Partial Reconfiguration of Heterogeneous SoCs with ESP
L.P. Carloni, B. Seyoum, **G. Tombesi**, J.Zuckerman
Design, Automation and Test in Europe Conference (DATE), 2023

Design of Heterogeneous SoCs for ASIC and FPGA Targets with ESP
L.P. Carloni, M. Cassel dos Santos, K.L. Chiu, B. Seyoum, **G. Tombesi**, J.Zuckerman
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2023.