# Giuseppe Di Guglielmo

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Research scientist and hardware engineer with 10+ years of experience in system-level design, HLS, FPGA-based acceleration, and functional verification, as well as a Ph.D. in hardware verification. Active contributor to the open-source hardware community for SoC design and machine learning acceleration.

## Experience

**Associate Research Scientist** Oct. 2013 — Present
*Columbia University, Department of Computer Science* *New York, NY*

- Columbia lead for the hls4ml project (`fastmachinelearning.org/hls4ml`), an open-source framework for the co-design, optimization, and automatic deployment of ML models on FPGAs. Collaborating with physicists and computer scientists at MIT, Fermilab, and CERN to deploy ML systems for applications like low-latency computational particle physics and low-power medical devices.
- Principal system-level designer for the Embedded Scalable Platforms project (`esp.cs.columbia.edu`), an open-source SoC platform adopted by institutions such as IBM Research and Harvard. ESP combines a system-level-design methodology with a heterogeneous computing architecture. My contributions include accelerator design for image processing and ML, design-space exploration with HLS, and heterogeneous SoC security and verification.
- Lead engineer for neural-network-based data compression on ASIC for the CERN Large Hadron Collider. The system will be deployed for the next 20 years, and must perform with ultra-low latency in a high-radiation environment. The design leverages HLS and relies on redundancy techniques against single-event effects.
- Architect for dynamic information flow tracking to secure RISC-V cores for the ETH Zurich PULP Platform.
- Instructor for graduate-level SoC design and verification courses at Columbia University.

**Postdoctoral Research Scientist** Nov. 2012 — Sept. 2013
*Columbia University, Department of Computer Science* *New York, NY*

- Used HLS to expedite the design of accelerators, improve design-space exploration, and promote the reuse of accelerators across different target SoCs.
- Designed a configurable set of accelerators using SystemC and Cadence C-to-Silicon, device drivers, and multi-threaded software for a DARPA-sponsored wide-area motion imagery (WAMI) system, an image processing application used for aerial surveillance.

**Postdoctoral Fellow** March 2010 — March 2011
*University of Tokyo, VLSI Design and Education Center* *Tokyo, Japan*

- Defined the first dynamic mining approach that assist developers in the formal verification of embedded software by automatically inferring linear temporal logic (LTL) properties. Best paper finalist at the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, 2012.

**Postdoctoral Fellow** April 2009 — Feb. 2010, April 2011 — Oct. 2012
*University of Verona, Department of Computer Science* *Verona, Italy*

- Collaborated with an industrial partner, STM Products S.r.l., to develop a suite of tools to integrate assertion-based verification in the model-driven design flow for embedded software.

**Verification Engineering Intern.** Sept. 2007 — Dec. 2007
*Certess Inc. (now Synopsys)* *Grenoble, France*

- Developed mutation-analysis techniques and a parallel simulator for functional-fault models at the register-transfer level for Certitude, the first tool for functional qualification, which identifies verification weaknesses that allow bugs to go undetected.

**Visiting Scholar** Oct. 2006 — Feb. 2007
*Tallinn University of Technology* *Tallinn, Estonia*

- Developed new techniques for the modeling and manipulation of embedded-system design.

## Language and Tools

- Hardware: SystemC, Verilog, VHDL
- Software: C/C++, Python, Bash, TCL, Git, Make
- Machine learning: Keras, TensorFlow
- Simulators: Mentor Graphics Modelsim and Questa Formal, Cadence Incisive
- EDA tools: Cadence C-to-Silicon, Cadence Stratus HLS, Mentor Catapult HLS, Mentor CCOV, Xilinx Vivado, Vivado HLS, Vidado SDK

## Education

**Ph.D. in Computer Science** Jan. 2006 — April 2009

*University of Verona, Department of Computer Science* *Verona, Italy*

- Thesis: "On the validation of embedded systems through functional ATPG"
- Primary topics: functional validation of embedded systems; automatic test pattern generation; system-level design; formal and simulation-based methods; computational and fault models.

**Laurea Degree *Summa cum Laude* in Computer Science** Sept. 1999 — Sept. 2005

*University of Verona, Department of Computer Science* *Verona, Italy*

## Research Activity

- Published 70+ scientific papers (Google Scholar) for peer-reviewed conference proceedings and journals on computer-aided design, verification, and security of heterogeneous SoC.
- Served in technical program committees and as a reviewer for 20+ international journals and conferences.

## Selected Publications

- *A reconfigurable neural network ASIC for detector front-end data compression at the HL-LHC*, G. Di Guglielmo et al., IEEE Transactions on Nuclear Science (TNS), 2021
- *Agile SoC development with open ESP*, P. Mantovani et al., in the Proc. of IEEE/ACM International Conference On Computer Aided Design (ICCAD), 2020
- *Leveraging prior knowledge for effective design-space exploration in high-level synthesis*, L. Ferretti et al., IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), 2020
- *Fast inference of Boosted Decision Trees in FPGAs for particle physics*, S. Summers et al., Journal of Instrumentation (JINST), 2020
- *PAGURUS: Low-overhead dynamic information flow tracking on loosely-coupled accelerators*, L. Piccolboni et al., IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), 2018
- *COSMOS: Coordination of high-level synthesis and memory optimization for hardware accelerators*, L. Piccolboni et al., ACM Transactions on Embedded Computing Systems (TECS), 2017
- *An analysis of accelerator coupling in heterogeneous architectures*, E. Cota et al., in the Proc. of ACM/EDAC/IEEE Design Automation Conference (DAC), 2015
- *On the integration of model-driven design and dynamic assertion-based verification for embedded software*, G. Di Guglielmo et al., Journal of Systems and Software (JSS), 2013
- *Dynamic property mining for embedded software*, M. Bonato et al., in the Proc. of IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2012