Giuseppe Di Guglielmo

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Research Interests

Giuseppe Di Guglielmo holds a Ph.D. in Computer Science with focus on the verification, validation, and testing of hardware at the system level. His areas of research are computer-aided design and verification of heterogeneous Systems-on-Chip. Current research topics are the design, optimization, and validation of hardware accelerators with emphasis on high-level synthesis and FPGA. He is interested in various application domains, such as physics, biology, image processing, and machine learning. He is recently investigating architectural solutions for hardware and software security.

Education

Ph.D. in Computer Science, University of Verona, Italy, 2009

TH2. *On the Validation of Embedded Systems through Functional ATPG*, Advisor: Prof. Franco Fummi

Laurea degree in Computer Science, *Summa Cum Laude*, University of Verona, Italy, 2005

TH1. *Verifica funzionale dei dispositivi digitali mediante manipolazione di Macchine a Stati Finiti Estese*, Advisor: Prof. Franco Fummi

Classical Studies Diploma, Liceo Ginnasio di Stato Scipione Maffei, Italy, 1998

Appointments

Research Scientist in Computer Science, October 2021 - *till now*

Affiliation: Columbia University in the City of New York, USA

Associate Research Scientist in Computer Science, October 2013 - September 2021

Affiliation: Columbia University in the City of New York, USA

Postdoctoral Research Scientist in Computer Science, November 2012 - September 2013

Affiliation: Columbia University in the City of New York, USA

Postdoctoral Fellow, March 2010 - March 2011

Affiliation: VLSI Design and Education Center (VDEC), University of Tokyo, Japan

Postdoctoral Fellow, April 2009 - February 2010

Affiliation: University of Verona, Department of Computer Science, Italy

Visiting Experiences

Visiting Scholar, August 2009 - February 2010

Affiliation: Purdue University, School of Electrical and Computer Engineering, USA

Student Internship, September 2007 - December 2007

Affiliation: Certess Inc. (now Synopsys), France

Visiting Student, October 2006 - February 2007

Affiliation: Tallinn University of Technology, Department of Computer Engineering, Estonia

Professional Activities

Research Projects

A Realtime HPC Platform with Inmemory NonVonNeumann Processing and Optical Networking (ARION), January 2020 – *till now*

Program: Digital RF Battlespace Emulator (DRBE)

Sponsor: Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Abstract: The Digital RF Battlespace Emulator (DRBE) program aims to create the world's first, large-scale, virtual radio frequency (RF) environment for developing, training, and testing advanced RF systems, such as radar and electronic warfare (EW) systems. The target DRBE environment will enable numerous RF systems to interact with each other in a fully closed-loop RF arena, replicating dense, responsive, real-world RF environments. RF systems increasingly use artificial intelligence (AI) to help automate and augment capabilities for defense use. DRBE is exploring novel computing architectures to enable the creation of a new breed of High Performance Computing (HPC) – dubbed "Real Time HPC". The goal of the RT-HPC is to generate computational performance in the double-digit petaFLOPs class while maintaining single-digit microsecond scale end-to-end latency.

Efficient Programmability of Cognitive Heterogeneous Systems (EPOCHS), January 2018 – *till now*

Program: Domain-Specific System on Chip (DSSOC)

Sponsor: Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Abstract: The project goal is to develop a heterogeneous system-on-chip comprised of many cores that mix general purpose processors, special purpose processors, hardware accelerators, memory, and input/output (I/O) devices to significantly improve performance of domain-specific applications of interest for the Department of Defense (DoD). The project explores architectures that improve the efficiency of computing through specialized processing while maintaining programmability. Dr. Di Guglielmo's research focuses on the development of automation methods for the sytem-level design and optimization of accelerators that are specialized for machine learning applications.

Embedded Computing for Embodied Learning, July 2019 – *till now*

Sponsor: SEAS Interdisciplinary Research Seed (SIRS) at Columbia University

Position: Researcher

Abstract: The project aims to embed computational power in a highly distributed fashion, inside a robot's body. The traditional paradigm calls for any data from the robot's sensors to be centralized to one powerful computer, often sitting outside the robot's body, in order to run learning algorithms that require high computing power. By distributing powerful, energy-efficient embedded computer platforms throughout the robot's body, the robot can process sensor data right where it is harvested, and use it to develop new motor skills. The robots designed in this project move through debris and clutter, in disaster response or search-and-rescue operations. Dr. Di Guglielmo focuses his research on robotic motor learning by leveraging embedded computing under power and computation constraints.

Acceleration of Deep Neural Networks via Heterogeneous Computing for Real-Time Processing of Neutrino and Particle Imagery, March 2018 – *till now*

Sponsor: Research Initiatives in Science & Engineering (RISE) at Columbia University

Position: Researcher

Abstract: The project aims to develop a system to facilitate real-time classification of images streamed at a massive scale, with the ultimate goal of leveraging recent advancements in computer science to accelerate particle physics discovery. The main application of the system is the upcoming Deep Underground Neutrino Experiment (DUNE). DUNE is a major international particle physics experiment aimed at continuously streaming high-resolution 3D images at over 5 terabytes per second. It will commence in 2024 and be operational for over a decade. Dr. Di Guglielmo's research focuses on the design of a scalable computing system that employs machine learning and field-programmable gate arrays (FPGAs) to identify and classify interesting activity in the data. The ability to process this data in real time could enable the discovery of rare particle interactions which have never before been observed.

Rethinking CAD for System-Level Design via Interactivity, Learning, and Collaboration, June 2015 – *till now*

Sponsor: National Science Foundation, Software and Hardware Foundations (SHF)

Position: Researcher

Abstract: The core part of this project was the development of a new senior-level undergraduate course unique in its use of a collaborative Computer-Aided Design (CAD) environment. Dr. Di Guglielmo developed a highly-interactive CAD environment for System-Level Design to promote continuous collaboration across teams of students and inspire creative engineering solutions. The proposed approach leverages his work on compositional design-space exploration and machine learning to assist designers in the use of advanced synthesis tools.

Hardware-Up Security Antifragility and Automation January 2018 – April 2019

Program: System Security Integrated Through Hardware and Firmware (SSITH)

Sponsor: Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Abstract: The SSITH program involved eight research institutes: Columbia University, MIT, Cornell, University of Michigan, University of California San Diego, Charles Draper Laboratories, Lockheed Martin, and SRI International. The overall goal of SSITH was to develop "hardware design tools that provide security against hardware vulnerabilities that are exploited through software in Department of Defense and commercial electronic systems". Dr. Di Guglielmo's research focused on the definition of security mechanisms between the hardware and software interfaces of modern Systems on Chip and hardware accelerators. The approach systematically strengthens each layer in the system stack from the low-level hardware up to the user-application software.

ESP: Embedded Scalable Platforms for Terascale Energy Efficient Computing February 2012 – August 2017

Program: Power Efficiency Revolution for Embedded Computing Technologies (PERFECT)

Sponsor: Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Dr. Di Guglielmo was a lead designer in this project, which was part of the DARPA multi-year program Power Efficiency Revolution for Embedded Computing Technologies (PERFECT) that started in February 2012 and completed its goals in August 2017. The aim of the PERFECT program was to research and develop the technologies to provide the power efficiency required by future military systems. The goal of ESP was to create a novel design methodology for digital integrated circuits which improves the amount of computation that can be performed per watt.

Center for Future Architectures Research (C-FAR) January 2013 – December 2017

Sponsor: Semiconductor Research Corporation (SRC) & Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Abstract: Semiconductor Research Corporation (SRC) & Defense Advanced Research Projects Agency (DARPA) founded the C-FAR project. The research center was focused on creating the future generation of scalable computing systems and completed its goals in December 2017. It accomplished its goals through a highly collaborative research agenda that brought together researchers from many top-tier universities, including Columbia, Duke, Harvard, MIT, Princeton, Stanford, UC Berkeley, and University of Michigan. Dr. Di Guglielmo's research efforts focused on improving the speed, throughput, and efficiency of the computation of heterogeneous, customized, and application-specific architectures.

A COrrect-by-CONstrUcTion Workbench for Design and Verification of Embedded Systems (COCONUT) January 2008 – June 2010

Sponsor: European Union Project FP7-IC

Position: Research Student

Abstract: The aim of the COCONUT project was the definition of a formal framework based on tight integration of design and verification through all the refinement steps of an embedded platform design flow, from the specifications to the logic synthesis and software compilation. The project proposed a modeling and verification flow to enhance and speed up the embedded platform design and configuration. The project also designed mixed continuous and discrete models for the management of multimedia and sensor networks.

Verification and Validation of Embedded System Design Workbench (VERTIGO) June 2006 – November 2008

Sponsor: European Union Project FP6-IST

Position: Research student

Abstract: The aim of the VERTIGO project was the development of technologies and tools to integrate the verification of embedded systems in configurable platforms, within economical and technical constraints. VERTIGO leveraged the results and tools coming from the previous IST-FP5 SYMBAD project and widened the spectrum of formal techniques applied at the verification of embedded systems.

Technical Program Commitee

1. IEEE International Conference on Computer Design (ICCD), 2019
2. IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2014
3. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2014
4. IEEE/CAS International Conference on VLSI Design (VLSID), 2014
5. Haifa Verification Conference (HVC), 2013

Services to the Technical Community

Over the years, Giuseppe Di Guglielmo has been a reviewer for many international journals and conferences. This is a partial list: IEEE Transactions on Very Large Scale Integration Systems, International Journal of Parallel Programming, IEEE Embedded System Letters (ESL), Journal of Systems and Software (JSS), IEEE/ACM Design Automation Conference (DAC), ACM/IEEE Design, Automation and Test in Europe (DATE), International Confererence on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), International Conference on Embedded Software (EMSOFT), ACM/IEEE International

Conference on Formal Methods and Models for System Design (MEMOCODE), International Conference on Computer Aided Design (ICCAD), IEEE High Performance Extreme Computing Conference (HPEC), IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), International Test Conference (ITC), ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), International Workshop on Logic & Synthesis (IWLS), ACM International Conference on Computing Frontiers (CF), IEEE International Parallel and Distributed Processing Symposium (IPDPS), IEEE International Conference on Computer Design (ICDD), Haifa Verification Conference, International Symposium on Games, Automata, Logics, and Formal Verification (GandALF), and many others.

Research Activities

Giuseppe Di Guglielmo has co-authored more than seventy papers with a h-index of 21 (Google Scholar). Publications are here listed together with Scimago h-index per journal publications and sponsor per conference publications. Sponsors, as the Institute of Electrical and Electronics Engineers (IEEE) and Association for Computing Machinery (ACM), have a long-standing commitment to sponsoring the highest quality peer-reviewed scientific contributions.

Journal Publications

J17. Naif Tarafdar, Giuseppe Di Guglielmo, Philip C. Harris, Jeffrey D. Krupa, Vladimir Loncar, Dylan Rankin, Nhan Tran, Zhenbin Wu, Qianfeng Shen, Paul Chow, *AIgean: An open framework for machine learning on heterogeneous clusers*, ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol. 15, No. 3, 2021, h-index 28

J16. Marco Ricci, Bernardita Štitić, Luca Urbinati, Giuseppe Di Guglielmo, Jorge A Tobon Vasquez, Luca P Carloni, Francesca Vipiana, Mario R Casu, *Machine-Learning Based Microwave Sensing: A Case Study for the Food Industry*, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, h-index 50

J15. Giuseppe Di Guglielmo, Farah Fahim, Christian Herwig, Manuel Blanco Valentin, Javier Duarte, Cristian Gingu,Philip Harris, James Hirschauer, Martin Kwok, Vladimir Loncar, Yingyi Luo, Llovizna Miranda, JenniferNgadiuba, Daniel Noonan, Seda Ogrenci-Memik, Maurizio Pierini, Sioni Summers, Nhan Tran, *A reconfigurable neural network ASIC for detector front-end data compression at the HL-LHC*, IEEE Transaction Nuclear Science, Vol. 68, No. 8, 2021, h-index 116

J14. Lorenzo Ferretti, Jihye Kwon, Giovanni Ansaloni, Giuseppe Di Guglielmo, Luca Carloni, and Laura Pozzi, *DB4HLS: A database of high-level synthesis design space explorations*, IEEE Embedded Systems Letters, 2021, h-index 23

J13. Jennifer Ngadiuba, Vladimir Loncar, Maurizio Pierini, Sioni Summers, Giuseppe Di Guglielmo, Javier Duarte, Philip Harris, Dylan Rankin Sergo Jindariani, Mia Liu, Kevin Pedro, Nhan Tran, Edward Kreinar, Sheila Sagear, Zhenbin Wu, and Duc Hoang, *Compressing deep neural networks on FPGAs to binary and ternary precision with hls4ml*, Machine Learning: Science and Technology, Vol. 2, No. 1, 2020, 015001

J12. Lorenzo Ferretti, Jihye Kwon, Giovanni Ansaloni, Giuseppe Di Guglielmo, Luca P. Carloni, and Laura Pozzi, *Leveraging prior knowledge for effective design-space exploration in high-level synthesis*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), Vol. 39, No. 11, 2020, pp. 3736-3747, h-index 113

J11. Sioni Summers, Giuseppe Di Guglielmo, Javier Duarte, Philip Harris, Duc Hoang, Sergo Jindariani, Edward Kreinar, Vladimir Loncar, Jennifer Ngadiuba, Maurizio Pierini, Dylan Rankin, Nhan Tran, and Zhenbin Wu, *Fast inference of Boosted Decision Trees in FPGAs for particle physics*, Journal of Instrumentation (JINST), Vol. 15, No. 5, 2020, P05026, h-index 69

J10. Ziyu Zhu, Giuseppe Di Guglielmo, Qixiang Cheng, Madeleine Glick, Jihye Kwon, Hang Guan, Luca P. Carloni, and Keren Bergman, *Photonic switched optically connected memory: an approach to address memory challenges in deep learning*, Journal of Lightwave Technology (JLT), Vol. 38, No. 10, 2020, pp. 2815-2825, h-index 191

J9. Luca Piccolboni, Giuseppe Di Guglielmo, Luca P. Carloni, *PAGURUS: Low-overhead dynamic information flow tracking on loosely-coupled accelerators*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), Vol. 37, No. 11, 2018, pp. 2685-2696, h-index 113

J8. Luca Piccolboni, Paolo Mantovani, Giuseppe Di Guglielmo, Luca P. Carloni, *COSMOS: Coordination of high-level synthesis and memory optimization for hardware accelerators*, ACM Transactions on Embedded Computing Systems (TECS), Vol. 16, No. 5, 2017, pp. 1-22, h-index 53

J7. Christian Pilato, Paolo Mantovani, Giuseppe Di Guglielmo, and Luca P. Carloni, *System-level optimization of accelerator local memory for heterogeneous systems-on-chip*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), Volume 36, Issue 3, 2017, pp. 435-448, h-index 113

J6. Giuseppe Di Guglielmo, Luigi Di Guglielmo, Andreas Foltinek, Masahiro Fujita, Franco Fummi, Cristina Marconcini, Graziano Pravadelli, *On the integration of model-driven design and dynamic assertion-based verification for embedded software*, Journal of Systems and Software (JSS), Volume 86, Issue 8, 2013, pp. 2013-2033, h-index 101

J5. Valerio Guarnieri, Giuseppe Di Guglielmo, Nicola Bombieri, Graziano Pravadelli, Franco Fummi, Hanno Hantson, Jaan Raik, Maksim Jenihhin, and Raimund Ubar, *On the reuse of TLM mutation analysis at RTL*, Journal of Electronic Testing: Theory and Applications (JETTA), Volume 28, Issue 4, 2012, pp. 435-448, h-index 33

J4. Viacheslav Izosimov, Giuseppe Di Guglielmo, Michele Lora, Graziano Pravadelli, Franco Fummi, Zebo Peng, and Masahiro Fujita, *Time-constraint-aware optimization of assertions in embedded software*, Journal of Electronic Testing: Theory and Applications (JETTA), Volume 28, Issue 4, 2012, pp. 469-486, h-index 33

J3. Giuseppe Di Guglielmo, Luigi Di Guglielmo, Franco Fummi, and Graziano Pravadelli, *Efficient generation of stimuli for functional verification by backjumping across extended FSMs*, Journal of Electronic Testing: Theory and Applications (JETTA), Volume 27, Issue 2, 2011, pp. 137-162, h-index 33

J2. Nicola Bombieri, Michele Ferrari, Giuseppe Di Guglielmo, Graziano Pravadelli, Francesco Stefanni, and Alessandro Venturelli, *HIFSuite: tools for HDL code conversion and manipulation*, EURASIP Journal on Advances in Signal Processing, Volume 2010, Issue 10.1155/2010/436328, 2010, pp. 1-20, h-index 83

J1. Giuseppe Di Guglielmo, Franco Fummi, Cristina Marconcini, and Graziano Pravadelli, *Improving high-level and gate-level testing with FATE: A functional automatic test pattern generator traversing unstabilised extended FSM*, Computers & Digital Techniques, IET, Volume 1, Issue 3, 2007, pp. 187-196, h-index 42

Chapter in Books

CB1. Giuseppe Di Guglielmo, Franco Fummi, Cristina Marconcini, and Graziano Pravadelli, *Books Test Generation based on CLP*, Micro Electronic and Mechanical Systems IN-TECH

Conference Publications

C48. Colby Banbury, Vijay Janapa Reddi, Peter Torelli, Jeremy Holleman, Nat Jeffries, Csaba Kiraly, Pietro Montino, David Kanter, Sebastian Ahmed, Danilo Pau, Urmish Thakker, Antonio Torrini, Peter Warden, Jay Cordaro, Giuseppe Di Guglielmo, Javier Duarte, Stephen Gibellini, Videet Parekh, Honson

Tran, Nhan Tran, Niu Wenxu, Xu Xuesong, *MLPerf Tiny Benchmark*, in the Prof. of Conference on Neural Information Processing Systems (NeurIPS), December 6-14, 2021

C47. Luca Piccolboni, Giuseppe Di Guglielmo, Simha Sethumadhavan, and Luca Carloni, *HARDROID: Transparent Integration of Crypto Accelerators in Android*, in the Proc. of IEEE High Performance Extreme Computing Virtual Conference (HPEC), September 20-24, 2021

C46. Luca Piccolboni, Giuseppe Di Guglielmo, Luca P Carloni, and Simha Sethumadhavan, *CRYLOGGER: Detecting crypto misuses dynamically*, in the Proc. of IEEE Symposium on Security and Privacy (S&P), May 24-27, 2021

C45. Farah Fahim, Benjamin Hawks, Christian Herwig, James Hirschauer, Sergo Jindariani, Nhan Tran, Luca Carloni, Giuseppe Di Guglielmo, Philip Harris, Jeffrey Krupa, Dylan Rankin, Manuel Blanco Valentin, Josiah Hester, Yingyi Luo, John Mamish, Seda Memik, Thea Aarrestad, Hamza Javed, Vladimir Loncar, Maurizio Pierini, Adrian Alan Pol, Sioni Summers, Javier Duarte, Scott Hauck, Shih-Chieh Hsu, Jennifer Ngadiuba, Mia Liu, Duc Hoang, Edward Kreinar, Zhenbin Wu, *hls4ml: An Open-Source Co-Design Workflow to Empower Scientific Low-Power Machine Learning Devices*, in the Proc. of TinyML Research Symposium, Virtual, March 26 2021, pp. 1-8

C44. Mantovani, Paolo, Davide Giri, Giuseppe Di Guglielmo, Luca Piccolboni, Joseph Zuckerman, Emilio G. Cota, Michele Petracca, Christian Pilato, and Luca P. Carloni, *Agile SoC development with open ESP*, in the Proc. of IEEE/ACM International Conference On Computer Aided Design (ICCAD), Virtual, November 2-5, 2020, pp. 1-9

C43. Maarten Hattink, Giuseppe Di Guglielmo, Luca P Carloni, Keren Bergman, *A scalable architecture for CNN accelerators leveraging high-performance memories*, in the Proc. of IEEE High Performance Extreme Computing Conference (HPEC), Virtual, September 21-25, 2020, pp. 1-6

C42. Naif Tarafdar, Giuseppe Di Guglielmo, Philip C. Harris, Jeffrey D. Krupa, Vladimir Loncar, Dylan S. Rankin, Nhan Tran, Zhenbin Wu, Qianfeng Shen, and Paul Chow, *AIgean: An open framework for machine learning on heterogeneous clusters*, in the Proc. of IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), Fayetteville, AK, USA, May 3-6, pp. 239-239

C41. Davide Giri, Kuan-Lin Chiu, Giuseppe Di Guglielmo, Paolo Mantovani, and Luca P. Carloni, *ESP4ML: Platform-based design of systems-on-chip for embedded machine learning*, in the Proc. of ACM/IEEE Conference on Design, Automation and Test in Europe (DATE), Grenoble, France, March 9-13, 2020, pp. 1049-1054

C40. Georgios Zacharopoulos, Lorenzo Ferretti, Giovanni Ansaloni, Giuseppe Di Guglielmo, Luca Carloni and Laura Pozzi, *Compiler-assisted selection of hardware acceleration candidates from application source code*, in the Proc. of IEEE International Conference on Computer Design (ICCD), 2019, pp. 129-137

C39. Luca Piccolboni, Giuseppe Di Guglielmo, and Luca P. Carloni, *KAIROS: Incremental verification in high-level synthesis through latency-insensitive design*, in the Proc. of Formal Methods in Computer-Aided Design (FMCAD), San Jose, CA, USA, October 22-25, 2019, pp. 105-109

C38. Luca P. Carloni, Emilio Cota, Giuseppe Di Guglielmo, Davide Giri, Jihye Kwon, Paolo Mantovani, Luca Piccolboni, and Michele Petracca, *Teaching heterogeneous computing with system-level design methods*, in the Proc. of Workshop on Computer Architecture Education (WCAE), Phoenix, AZ, USA, June 22, 2019, pp. 1-8

C37. Yeon-Jae Jwa, Giuseppe Di Guglielmo, Luca P. Carloni and Georgia Karagiorgi, *Accelerating deep neural networks for real-time data selection for high-resolution imaging particle detectors*, in the Proc. of New York Scientific Data Summit (NYSDS), New York, NY, USA, June 12-14, 2019, pp. 1-10

C36. Christian Palmiero, Giuseppe Di Guglielmo, Luciano Lavagno, and Luca P. Carloni, *Design and implementation of a dynamic information flow tracking architecture to secure a RISC-V core for IoT applications*, in the Proc. of IEEE High Performance Extreme Computing Conference (HPEC), Waltham, MA, USA, September 25-27, 2018, pp. 1-7

C35. Luca Piccolboni, Paolo Mantovani, Giuseppe Di Guglielmo, and Luca P. Carloni, *Broadening the exploration of the accelerator design space in embedded scalable platforms*, in the Proc. of Twenty-First Annual Conference on High Performance Extreme Computing (HPEC), Waltham, MA, USA, September 12-14, 2017, pp. 1-7

C34. Paolo Mantovani, Emilio Cota, Christian Pilato, Giuseppe Di Guglielmo, and L. P. Carloni, *Handling large data sets for high-performance embedded applications in heterogeneous systems-on-chip*, in the Proc. of ACM/IEEE International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES), Pittsburgh, PA, USA, October 2-7, 2016, pp. 1-10

C33. Paolo Mantovani, Emilio Cota, Kevin Tien, Christian Pilato, Giuseppe Di Guglielmo, Ken Shepard, and Luca P. Carloni, *An FPGA-based infrastructure for fine-grained DVFS analysis in high-performance embedded systems*, in the Proc. of ACM/IEEE Design Automation Conference (DAC), Austin, TX, USA, June 5-9, 2016, pp. 1-6

C32. Christian Pilato, Qirui Xu, Paolo Mantovani, Giuseppe Di Guglielmo, and Luca P. Carloni, *On the design of scalable and reusable accelerators for big data applications*, in the Proc. of ACM International Conference on Computing Frontiers (CF), Como, Italy, May 16-18, 2016, pp. 406-411

C31. Paolo Mantovani, Giuseppe Di Guglielmo, and Luca P. Carloni, *High-level synthesis of accelerators in embedded scalable platforms*, in the Proc. of ACM/IEEE/IEICE Asia and South Pacific Design Automation Conference (ASP-DAC), Macao, January 25-28, 2016, pp. 204-211

C30. Emilio Cota, Paolo Mantovani, Giuseppe Di Guglielmo, Luca Carloni, *An analysis of accelerator coupling in heterogeneous architectures*, in the Proc. of ACM/EDAC/IEEE Design Automation Conference (DAC), San Francisco, USA, June 7-11, 2015, pp. 1-6

C29. Christian Pilato, Paolo Mantovani, Giuseppe Di Guglielmo, Luca Carloni, *System-level memory optimization for high-level synthesis of component-based SoCs*, in the Proc. of ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New Delhi, India, October 12-17, 2014, pp. 1-10

C28. Giuseppe Di Guglielmo, Christian Pilato, Luca Carloni, *A design methodology for compositional high-level synthesis of communication-centric SoCs*, in the Proc. of ACM/EDAC/IEEE Design Automation Conference (DAC), San Francisco, USA, June 1-5, 2014, pp. 1-6

C27. Michele Bertasi, Giuseppe Di Guglielmo, and Graziano Pravadelli, *Automatic generation of compact formal properties for effective error detection*, in the Proc. of IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Montreal, Canada, September 29 - October 4, 2013, pp. 1-1

C26. Giuseppe Di Guglielmo, Davide Ferraretto, Franco Fummi, Graziano Pravadelli, *Efficient fault simulation through dynamic binary translation for dependability analysis of embedded software*, in the Proc. of IEEE European Test Symposium (ETS), Avignon, France, May 27-31, 2013, pp. 21-26

C25. Simone Bronuzzi, Giuseppe Di Guglielmo, Franco Fummi, and Graziano Pravadelli, *Accurate profiling of oracles for self-checking time-constrained embedded software*, in the Proc. of IEEE International High Level Design Validation and Test Workshop (HLDVT), Huntington Beach, CA, USA, November 9-10, 2012, pp. 96-99

C24. Giuseppe Di Guglielmo and Graziano Pravadelli, *A testbench specification language for SystemC verification*, in the Proc. of IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Tampere, Finland, October 7-12, 2012, pp. 333-342

C23. Marco Bonato, Giuseppe Di Guglielmo, Masahiro Fujita, Franco Fummi, and Graziano Pravadelli, *Dynamic property mining for embedded software*, in the Proc. of IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Tampere, Finland, October 7-12, 2012, pp. 187-196

C22. Urmas Repinski, Hanno Hantson, Maksim Jenihhin, Jaan Raik, Raimund Ubar, Giuseppe Di Guglielmo, Graziano Pravadelli, and Franco Fummi, *Combining Dynamic Slicing and Mutation Operators for System-Level Repair*, in the Proc. of European Test Symposium (ETS), Annecy, France, May 28 - June 1, 2012, pp. 116-121

C21. Giuseppe Di Guglielmo, Luigi Di Guglielmo, Graziano Pravadelli, Franco Fummi, *On the use of assertions for embedded-software dynamic verification*, in the Proc. of IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), Tallinn, Estonia, April 18-20, 2012, pp. 330-335

C20. Giuseppe Di Guglielmo, Luigi Di Guglielmo, Franco Fummi, and Graziano Pravadelli, *Enabling Dynamic Assertion-based Verification of Embedded Software through Model-driven Design*, in the Proc. of ACM/IEEE Design, Automation and Test in Europe (DATE), Dresden, Germany, March 12-16, 2012, pp. 212-217

C19. Giuseppe Di Guglielmo, Luigi Di Guglielmo, Franco Fummi, and Graziano Pravadelli, *IPA: Assertion-based verification in embedded-software design*, in the Proc. of IEEE International High Level Design Validation and Test Workshop (HLDVT), Napa Valley, CA, USA, November 9-11, 2011, pp. 80-80

C18. Giuseppe Di Guglielmo, Masahiro Fujita, Franco Fummi, Graziano Pravadelli, and Stefano Soffia, *EFSM-based model-driven approach to concolic testing of system-level design*, in the Proc. of ACM/IEEE Ninth International Conference on Formal Methods and Models for Codesign (MEMOCODE), Cambridge, UK, July 11-13, 2011, pp. 201-209

C17. Viacheslav Izosimov, Zebo Peng, Michele Lora, Graziano Pravadelli, Franco Fummi, Giuseppe Di Guglielmo, and Masahiro Fujita, *Optimization of assertion placement in time-constrained embedded systems*, in the Proc. of IEEE European Test Symposium (ETS), Trondheim, Norway, May 23-27, 2011, pp. 171-176

C16. Giuseppe Di Guglielmo, Luigi Di Guglielmo, Masahiro Fujita, Cristina Marconcini, Andreas Foltinek, Franco Fummi, and Graziano Pravadelli, *Model-driven design and validation of embedded software*, in the Proc. of IEEE/ACM International Workshop on Automation of Software Testing (ICSE Workshop), Waikiki, Honoulu, Hawaii, May 23-24, 2011, pp. 98-104

C15. Nicola Bombieri, Michele Ferrari, Giuseppe Di Guglielmo, Graziano Pravadelli, Francesco Stefanni, and Alessandro Venturelli, *HIFSuite: Tools for HDL Code Conversion and Manipulation*, in the Proc. of IEEE International High Level Design Validation and Test Workshop (HLDVT), Anaheim, CA, USA, 2010, pp. 40-41

C14. Michele Bertasi, Giuseppe Di Guglielmo, Franco Fummi, Graziano Pravadelli, *Effective EFSM generation for HW/SW-design verification*, in the Proc. of IEEE International Biennal Baltic Electronics Conference (BEC), Tallinn, Estonia, October 4-6, 2010, pp. 209-212

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Pre-print or Non-Peer Reviewed Publications

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U6. Allison McCarn Deiana, Nhan Tran, Joshua Agar, Michaela Blott, Giuseppe Di Guglielmo, Javier Duarte, Philip Harris, Scott Hauck, Mia Liu, Mark S Neubauer, Jennifer Ngadiuba, Seda Ogrenci-Memik, Maurizio Pierini, Thea Aarrestad, Steffen Bahr, Jurgen Becker, Anne-Sophie Berthold, Richard

J Bonventre, Tomas E Muller Bravo, Markus Diefenthaler, Zhen Dong, Nick Fritzsche, Amir Gholami, Ekaterina Govorkova, Kyle J Hazelwood, Christian Herwig, Babar Khan, Sehoon Kim, Thomas Klijnsma, Yaling Liu, Kin Ho Lo, Tri Nguyen, Gianantonio Pezzullo, Seyedramin Rasoulinezhad, Ryan A Rivera, Kate Scholberg, Justin Selig, Sougata Sen, Dmitri Strukov, William Tang, Savannah Thais, Kai Lukas Unger, Ricardo Vilalta, Belinavon Krosigk, Thomas K Warburton, Maria Acosta Flechas, Anthony Aportela, Thomas Calvet, Leonardo Cristella, Daniel Diaz, Caterina Doglioni, Maria Domenica Galati, Elham E Khoda, Farah Fahim, Davide Giri, Benjamin Hawks, Duc Hoang, Burt Holzman, Shih-Chieh Hsu, Sergo Jindariani, Iris Johnson, Raghav Kansal, Ryan Kastner, Erik Katsavounidis, Jeffrey Krupa, Pan Li, Sandeep Madireddy, Ethan Marx, Patrick McCormack, Andres Meza, Jovan Mitrevski, Mohammed Attia Mohammed, Farouk Mokhtar, Eric Moreno, Srishti Nagu, Rohin Narayan, Noah Palladino, Zhiqiang Que, Sang Eon Park, Subramanian Ramamoorthy, Dylan Rankin, Simon Rothman, Ashish Sharma, Sioni Summers, Pietro Vischia, Jean-Roch Vlimant, Olivia Weng, *Applications and Techniques for Fast Machine Learning in Science*, October 2021, arXiv:2110.13041

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U3. Luca Piccolboni, Giuseppe Di Guglielmo, and Luca P. Carloni, *Securing accelerators with dynamic information flow tracking*, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), Washington DC, VA, USA May 6-10, 2019, pp. 1-2

U2. Paolo Mantovani, Emilio G. Cota, Seongjong Kim, Kevin Tien, Johnnie Chan, Giuseppe Di Guglielmo, Christian Pilato, Martha A. Kim, Mingoo Seok, Kenneth Shepard, and Luca P. Carloni, *Benchmarking methodology for embedded scalable platforms*, SEAK Workshop, San Francisco, CA, USA, June 1, 2014

U1. Giuseppe Di Guglielmo, Masahiro Fujita, Franco Fummi, Graziano Pravadelli, Stefano Soffia, *EFSM-based Weight-oriented Concolic Testing for Embedded Software*, IEICE Technical Report, Vol. 110, No. 316, pp. 19-24, November 11, 2010

Tutorials

T8. *ESP: the Open-Source Research Platform for Agile SoC Design and Programming*, ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2021

T7. *ESP: an Open-Source Platform for Agile SoC Development*, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2021

T6. *ESP: an Open-Source Platform for Agile SoC Development*, IEEE/ACM International Symposium on Microarchitecture (MICRO), 2020

T5. *ESP: an Open-Source Platform for Interdisciplinary Research on SoC Design and Programming*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2020

T4. *Open-Source Hardware: Heterogeneous System Integration with Embedded Scalable Platforms*, Embedded Systems Week (ESWEEK), October 13-18, 2019

T3. *Assertion based verification: a common verification infrastructure for SoC and embedded software at Design*, ACM/IEEE Design, Automation and Test in Europe (DATE), March 18-22, 2013

T2. *Assertion-based verification for SoC and embedded software at Asia and South Pacific Design Automation Conference*, ACM/IEEE/IEICE Asia and South Pacific Design Automation Conference (ASP-DAC), January 30 - February 2, 2012

T1. *Verifying reliability* at Dagstuhl Seminar 12341, Germany, August 18-24, 2012

Awards

A5. Best paper finalist for "ESP4ML: Platform-Based Design of Systems-on-Chip for Embedded Machine Learning"

ACM/IEEE Conference on Design, Automation and Test in Europe (DATE), 2020

A4. Best Session Presentation Award for "Automatic Revisioning of Communication Interfaces for Compositional High-Level Synthesis of SoCs"

Semiconductor Research Corporation TECHON, 2014

A3. Best paper finalist for "Dynamic property mining for embedded software"

IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, 2012

A2. Best paper finalist for "FATE: A Functional ATPG to Traverse Unstabilized EFSMs"

IEEE European Test Symposium, 2006

A1. First prize winner of competition "Applicazioni per Terminali Mobili", 2004

Telecom Italia Lab (TiLab), Torino, Italy

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