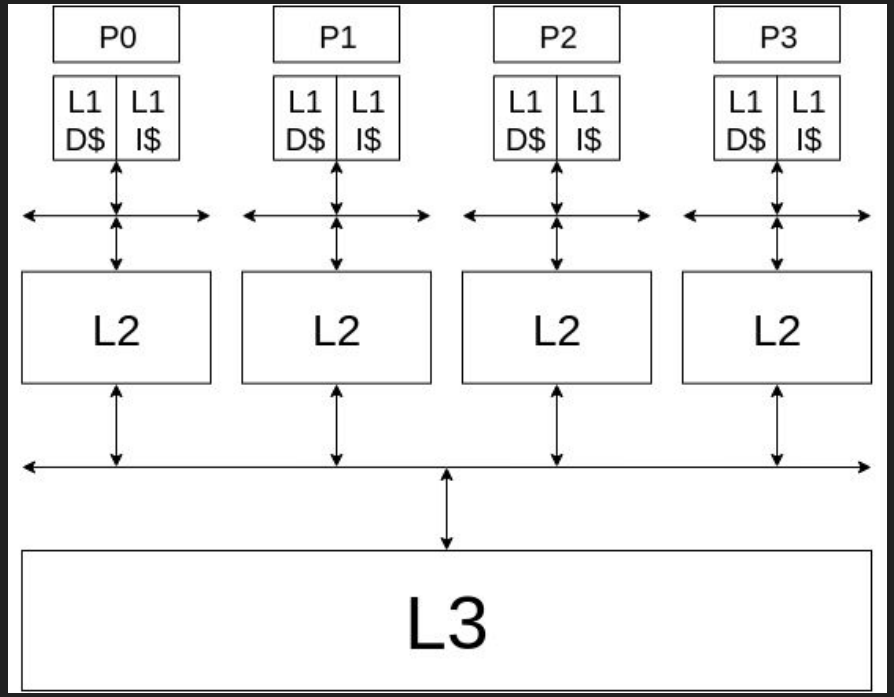
Verifying an L2 Cache

Chae Jubb

Background on Cache

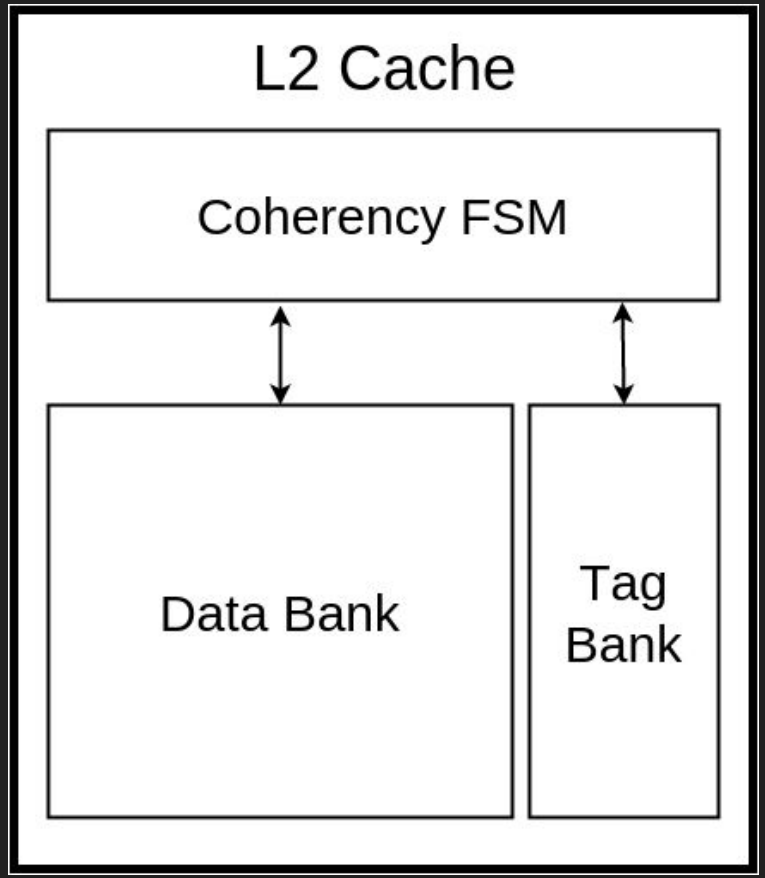
- Coherent (MESI protocol)
- L2
  - Private
  - Unified
  - 8-way associative
  - 128 sets
- L3
  - Shared
  - Unified
  - 32-way associative
  - 128 sets



Cache Architecture

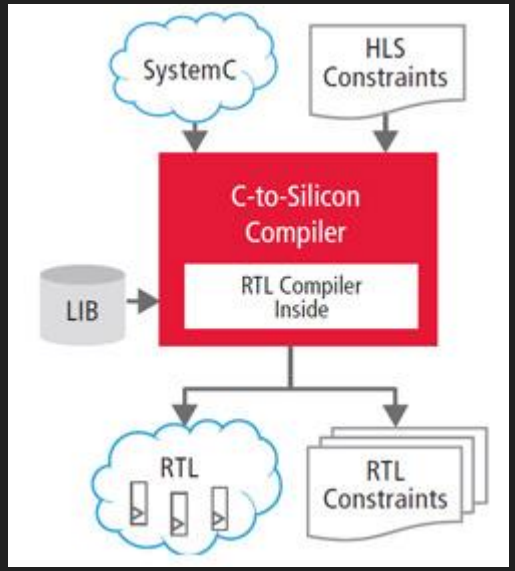
Main Components

- Data Bank
  - Store and Fetch Data
- Tag Bank
  - Store and Fetch Metadata
- Coherency FSM
  - Maintain Coherent System
  - Process incoming messages
  - Send outgoing messages
  - Read / Write from data and tag banks



General Tools

- Toolbox
  - HLS Specification of DUT
  - HLS Directed Test Bench
  - RTL Implementation of DUT
- Validation and Verification
  - HLS DUT / HLS TB
  - RTL DUT / HLS TB
  - **FV on RTL DUT**



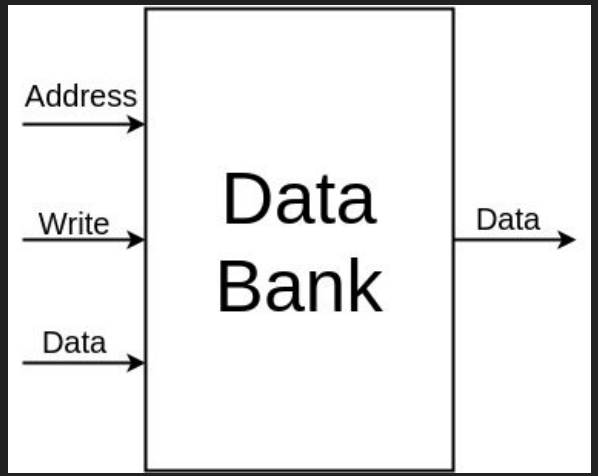
SYSTEMC™

Questa

Data Bank Validation & Verification

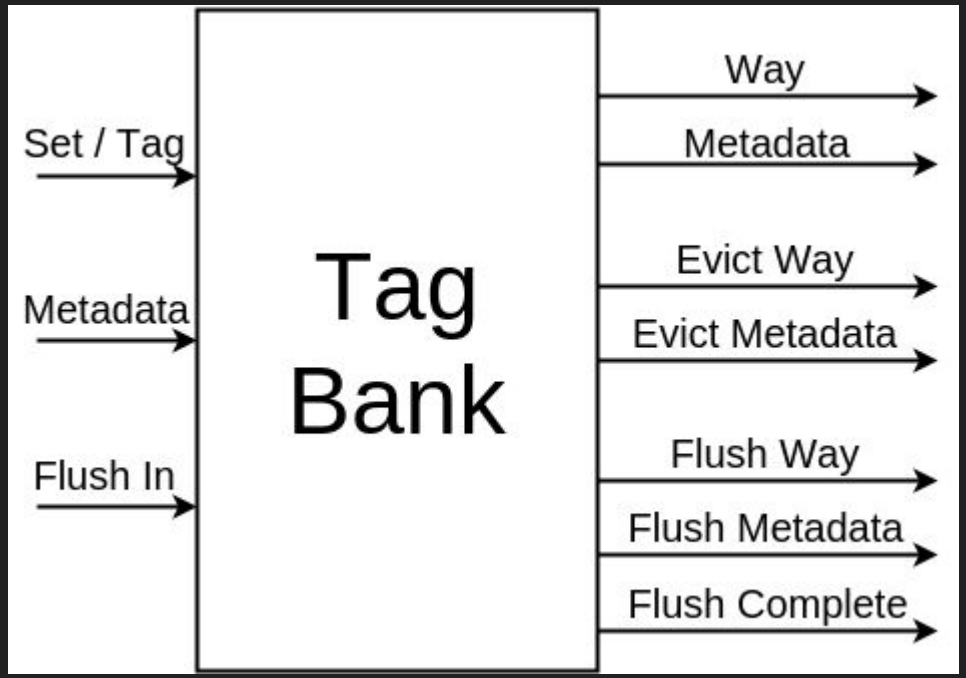
- Simple Interface
  - Address / Data In
  - Data Out
- Formal Assumptions
  - Latency-Insensitive Interface
  - Readiness for Response
  - Validity of Input
- Properties Tested
  - Latency Bound
- Properties Not Tested
  - Data Correctness
- Simulation / Directed Testing
  - Control Correctness Common Cases
  - Data Correctness

- Two-pronged Approach
  - Simulation first
  - Formal Verification second
  - Types of properties for each



Tag Bank Validation & Verification

- More complex than data bank
- Additional Assumptions
  - Flush Protocol
  - Optional Inputs
- Uncovered Branches
  - Cover with FV!
- Latency Bounds
  - General request
  - Non-flushing request
  - Read hit (bound / cover)
- Simulation Coverage
  - Line: 100%
  - Branch: 88% (excluding `assert`)
- Simulation During Development
- Verification at Milestones



Limits of FV

- State Space Explosion
  - Flushing Properties
  - Multiple “Levels” of Properties
- Language of Properties
  - Extended Reset
  - Formal Constraints
  - Formal Assumptions

Coherency FSM Validation & Verification

- Purely Simulation
- High Coverage
  - 94% Line
  - 64% Branch (including `assert`)
- No Latency Bound
- Meaningful FV Impractical
  - Complex FSM
  - Many (control message, coherency state) pairs
  - State Space Explosion

	Hit	Total	Coverage
Lines:	558	590	94.6 %
Functions:	8	8	100.0 %
Branches:	291	456	63.8 %

Future Work

- Model Checking of Entire L2 Cache (RTL)
- Model Checking of Coherency Protocol (RTL)
- Equivalence Checking of HLS specification and RTL implementation
- Model Checking of L2 Cache (HLS level)
- Checking L2 Cache for undefined behavior
  - Use before initialization
  - Array out-of-bounds accesses

Summary

- Formal Verification
  - State-Space explosion is real
  - Generating formal assumptions is hard
  - *Provable* bounds and other properties
  - Uncommon case
  - Limited language for properties
- Simulation
  - Quick feedback
  - Common case
  - Difficult / impossible to prove or bound properties