Davide **Giri**

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Education

Columbia University — *New York, USA*
PH.D. IN COMPUTER SCIENCE (GPA: 4.0/4.0) — *(expected) May 2021*

University of Illinois at Chicago — *Chicago, USA*
M.S. IN ELECTRICAL AND COMPUTER ENGINEERING (GPA @ UIC: 4.0/4.0), TOP-UIC DOUBLE DEGREE — *May 2015*

Tongji University — *Shanghai, China*
B.S. IN ELECTRONIC AND INFORMATION ENGINEERING, POLITONG DOUBLE DEGREE — *Jan. 2015*

Polytechnic University of Turin — *Turin, Italy*
M.S. IN ELECTRONIC ENGINEERING (110/110 WITH HONORS), TOP-UIC DOUBLE DEGREE — *Dec. 2014*

Polytechnic University of Turin — *Turin, Italy*
B.S. IN INFORMATION TECHNOLOGY ENGINEERING (110/110 WITH HONORS), POLITONG DOUBLE DEGREE — *Jul. 2012*

Experience

Columbia University, Computer Science Department — *New York, USA*
GRADUATE RESEARCH ASSISTANT, SYSTEM LEVEL DESIGN GROUP (ADVISOR: PROF. LUCA CARLONI) — *Jan. 2016 - present*

- Research on heterogeneous SoCs: accelerator integration and programmability, memory hierarchy, data orchestration.
- Contributing since Jan. 2016 to the development and release of ESP, an open-source platform for heterogeneous SoC design.
- Contributing since July 2018 to the DECADES and EPOCHS projects, funded by the SDH and DSSoC DARPA ERI programs.

NVIDIA — *Santa Clara, CA, USA*
RESEARCH INTERN, ASIC/VLSI RESEARCH GROUP — *May 2018 - Aug. 2018*

- Project: *"Optimization of Latency-Insensitive Channels for High-Productivity SoC Design."*. Contributed to MatchLib.

Fiat Chrysler Automobiles (FCA) — *Turin, Italy*
TEST ENGINEER IN THE ELECTRICAL/ELECTRONIC VALIDATION DEPARTMENT — *May 2015 - Dec. 2015*

- Designed semi-automatic tests for software validation of ECUs after integration on the vehicle (e.g. emergency brake, alarm).

Polytechnic University of Turin, Department of Electronics and Telecommunications — *Turin, Italy*
GRADUATE RESEARCHER, VLSI LABORATORY (ADVISORS: PROF. M. GRAZIANO, PROF. M. ZAMBONI) — *Jan. 2014 - Dec. 2014*

- M.S. Thesis: *"MagnetoElastic NanoMagnet Logic circuits"*. Designed the first ME NML circuits.

EnviSens Technologies — *Chivasso, Italy*
FIRMWARE DESIGN INTERN, PROJECT ON A WIRELESS SENSORS NETWORK — *Mar. 2012 - Jul. 2012*

- B.S. Thesis: *"Firmware Debug and Software Interface Creation for a Wireless Sensors Network"*.

Technical Skills

Languages Assembly, Bash, **C**/C++, HTML, **LaTeX**, Matlab, Python, **SystemC**, TCL, Verilog, **VHDL**.

Tools Altera Quartus II, Cadence SimVision and **Stratus HLS**, **Git**, Intel Pin, Mentor **Modelsim** and Catapult HLS, Synopsys Design Compiler, Xilinx **Vivado** and Vivado HLS.

Publications

[1] O. Matthews, J. L. Aragon, T. J. Ham, **D. Giri**, A. Manocha, T. Sorensen, M. O. Vera, E. Tureci, L. P. Carloni, M. Martonosi
(in press) "MosaicSim: A Lightweight, Modular Simulator for Heterogeneous Systems", ISPASS, 2020.

[2] P. Mantovani, R. Margelli, **D. Giri**, L. P. Carloni
(in press) "HL5: A 32-bit RISC-V Processor Designed with High-Level Synthesis", (invited) CICC, 2020.

[3] **D. Giri**, K. Chiu, G. Di Guglielmo, P. Mantovani, and L. P. Carloni
(in press) "ESP4ML: Platform-Based Design of Systems-on-Chip for Embedded Machine Learning", DATE, 2020.

[4] L. P. Carloni, E. Cota, G. Di Guglielmo, **D. Giri**, J. Kwon, P. Mantovani, L. Piccolboni, M. Petracca
"Teaching Heterogeneous Computing with System-Level Design Methods", WCAE, 2019.

[5] **D. Giri**, P. Mantovani, L. P. Carloni
"Runtime Reconfigurable Memory Hierarchy in Embedded Scalable Platforms", (invited) ASPDAC, 2019.

[6] **D. Giri**, P. Mantovani, L. P. Carloni
"Accelerators and Coherence: An SoC Perspective", IEEE Micro (Special Issue: Hardware Acceleration), 2018.

[7] **D. Giri**, P. Mantovani, L. P. Carloni
"NoC-Based Support of Heterogeneous Cache-Coherence Models for Accelerators", NOCS, 2018.
[8] **D. Giri**, G. Causapruno, F. Riente
"Parallel and Serial Computation in Nanomagnet Logic: an Overview", IEEE Transactions on VLSI Systems, 2018.
[9] **D. Giri**, M. Vacca, G. Causapruno, M. Graziano, M. Zamboni
"Modeling, Design and Analysis of MagnetoElastic NML Circuits", IEEE Transactions on Nanotechnology, 2016.
[10] **D. Giri**, M. Vacca, G. Causapruno, W. Rao, M. Graziano, M. Zamboni
"A Standard Cell Approach for MagnetoElastic NML Circuits", NANOARCH, 2014.

Tutorials

[1] L. P. Carloni, G. Di Guglielmo, **D. Giri**, P. Mantovani
"ESP: An Open-Source Platform for Interdisciplinary Research on SoC Design and Programming", ASPLOS, 2020.
[2] L. P. Carloni, G. Di Guglielmo, **D. Giri**, P. Mantovani
"Open-Source Hardware: Heterogeneous System Integration with Embedded Scalable Platforms", ES Week, 2019.

Talks

[1] L. P. Carloni, G. Di Guglielmo, **D. Giri**, P. Mantovani
"ESP: An Open-Source Platform for Interdisciplinary Research on SoC Design and Programming", ASPLOS, 2020.
[2] L. P. Carloni, **D. Giri**
"Open ESP: The Heterogeneous Open-Source Platform for Developing RISC-V Systems", FOSDEM, 2020.
[2] **D. Giri**
"Accelerator Integration in Heterogeneous Architectures", PhD Candidacy Exam, 2020.
[3] L. P. Carloni, G. Di Guglielmo, **D. Giri**, P. Mantovani
"Open-Source Hardware: Heterogeneous System Integration with Embedded Scalable Platforms", ES Week, 2019.
[4] **D. Giri**, P. Mantovani, L. P. Carloni
"NoC-Based Support of Heterogeneous Cache-Coherence Models for Accelerators", NOCS, 2018.

Teaching

Computer Architecture: Teaching Assistant.	*Columbia University*	Summer '19
System-on-Chip Platforms: Teaching Assistant.	*Columbia University*	Fall '17 '18
Embedded Scalable Platforms: Teaching Assistant ('19, '20) and Project Mentor.	*Columbia University*	Spring '18 '19 '20
Projects in Computer Science: Project Mentor.	*Columbia University*	Fall '17 '18 '19

Awards

Columbia University: Kosoresow Memorial Award for Excellence in Teaching and Service.	*New York, USA*	Fall 2018
Polytechnic University of Turin: Scholarship for the Top-UIC M.S. double degree program.	*Turin, Italy*	2013
Polytechnic University of Turin: Scholarship for the PoliTong B.S. double degree program.	*Turin, Italy*	2010
EDISU Piemonte: Full scholarship and tuition exemption for B.S and M.S programs.	*Turin, Italy*	2009-2014

Relevant Coursework

Advanced Programming, Analog Electronics, Analysis of Algorithms, Artifical Intelligence, CAD of Digital Systems, Circuits Theory, Computer Architecture, Digital Electronics, Electronic Devices, Electronic Systems, Embedded Scalable Platforms, Multimedia Systems, Neural Networks, Operating Systems, Signal Theory, System-on-Chip Platforms.

Class Projects

CAD of Digital Systems	CAD tool for re-timing of sequential circuits and multi-cube extraction for multi-level logic.
Neural Networks	Counter Propagation neural network for American Sign Language classification.
Operating Systems	Modify Linux kernel of a Huawei phone. Main topics: scheduler, synchronization, virtual memory.

Extracurricular Activity

Classical piano education (1998 - 2009) — **Competitive level soccer** (1996 - present) — **Volunteering as activity leader in summer camps** (2005 - 2009) — **Business Foundations Specialization:** 4 courses on Coursera by The Wharton School (2015).