CSEE W3827 - Fundamentals of Computer Systems
Course Information

Course Call #: 96898
Professor Dan Rubenstein Fall 2010

Course Resources

Contact Information					
Staff	**Office**	**Phone**	**e-mail**	**Mailbox**	**Office Hours**
Dan Rubenstein (Instructor)	CEPSR 816	(212) 854-0050	danr@cs.columbia.edu	CS Main Office	M,W 2-3pm or by appt.
Qi Ding (TA)	CS TA Room	(212) 854-4916	qd2110@columbia.edu	TBD	Th 3-5pm
Vinay Sharma (TA)	CS TA Room	(212) 854-4916	vs2330@columbia.edu	EE Office (Mudd 1310)	Tu 2-4pm
Cathy Chen (TA)	CEPSR 803	(212) 854-2900	cache@ee.columbia.edu	EE Office (Mudd 1310)	F 10am-12pm (in CEPSR 8th fl Lounge)
Yipeng Huang (TA)	CS TA Room	(212) 854-4916	yh2315@columbia.edu	TBD	MW 4:30-5:30pm

Course URL: http://www.cs.columbia.edu/∼danr/3827

Course meeting time / location: 11:00 am - 12:15 pm on Tu,Th in 627 Mudd

Pre-Requisites

An introductory programming course (e.g., COMS 1004 or 1007)

Description

This course explains, from a logic perspective, how computers work, i.e., how 0's and 1's are manipulated to do all the advanced calculations, computations, and services that computers can perform. The first major topic is digital logic, which concerns the design of circuits to implement logic functions using standard components such as AND-gates, OR-gates, and inverters. The circuits might be used to control the flow of data within a computer, or the processing of the data (e.g., arithmetic operations), or to control the overall action of a computer. We will cover how to specify logic functions precisely, to manipulate formal expressions, and to implement them efficiently. We will then cover the design of basic building blocks, including the control, of modern digital computers. Both combinational and sequential circuits will be covered.

The second part of the course involves the structure and software interface of digital computers. Focusing our attention on modern RISC architecture. We will discuss the functional blocks such as the arithmetic unit, register files, and memory. Single-cycle and multiple-cycle implementations will be presented, followed by the concept of pipelining. We will cover the basics of caches and virtual memory. Machine and assembly language programming is a feature of the course. Main memory systems, currently DRAM, will be discussed as well as the operation of magnetic disk drives. Some aspects of I/O will also be introduced.

Grading

Your grade consists of:

40% **Homework:** Homework is **due by the end of class at 12:15** on the date that it is due, unless otherwise specified. **The TAs**, Qi, Vinay and Cathy, will accept assignments until the end of the day, provided you can find them. **Professor Rubenstein will not accept assignments once they have been handed to Qi, Vinay, or Cathy for grading.** E-mailed/faxed homework and late assignments will not be accepted unless approved in advance. Approval will only be given under extreme circumstances. You are expected to produce your work in a timely manner. You may discuss and work on questions with other students in the class. However, you should write your solutions on your own, i.e., not copy someone else's solution.

35% **Mid-term:** October 21, in-class, open book, open note, no calculators.

45% **Final:** Probably 12/21 at 9am (determined by the registrar), open book, open note, no calculators.

Note that the total adds to 120%. The lowest score's contribution is reduced by 20%. For instance, if your homework average is 90, your midterm score is a 35, and your final exam score is 70, the midterm's contribution is reduced to 15%, making your average score equal to $0.4 \times 90 + 0.15 \times 35 + 0.45 \times 70 = 72.75$.

A note on effort: The final grade is based on my interpretation of how well you know the material. If all I know about you is your scores on homeworks, midterm and final, then those will directly determine your grade. If, however, you speak up in class and/or attend office hours, this gives me another way to evaluate how much you know and can only help your grade.

Reading / Texts

Two texts are **required**:

- *Logic and Computer Design Fundamentals (4th edition)*, M. Morris Mano and Charles R. Kime, Prentice Hall. ISBN 0-13-198926-X, ISBN-13: 978-0-13-198926-9
- *Computer Organization and Design, The Hardware/Software Interface, 4th edition*, David A. Patterson and John L. Hennessy, Morgan Kaufmann, ISBN 978-0-12-374493-7

A text used back in 2007 that can be used as a reference text:

- *Fundamentals of Digital Logic with VHDL Design, 3rd edition*, Stephen Brown and Zvonko Vranesic, ISBN 0-07-352953-2, ISBN-13: 978-0-07-352953-0

Computing Accounts

The course does not require computing facilities or computing accounts.

Syllabus and Schedule

Note schedule subject to change...

Date	#	Topics/chapters covered	Reading	Assigned	Due
9/7	1	Intro; Overview of Computer Architecture; Definitions (bit,byte,word)	M&K Ch 1		
9/9	2	Binary number representations: 1's complement; 2's complement, adding and subtracting and overflow; floating point representations: overflow and underflow	M&K 4.3-4.4, 10.7, P&H 3.5 skip FP in MIPS	HW #1	
9/14	3	Logic gates; XOR; Boolean Algebra; NAND and NOR gates; Taking complements; DeMorgan's Theorem; Duals	M&K 2.1-2.2, 2.8 2.9		
9/16	4	Standard Forms: minterms, maxterms, sum-of-products, product-of-sums	M&K 2.3	HW #2	HW #1
9/21	5	K-maps: simplification with implicants, Don't-care conditions	M&K 2.4-2.5		
9/23	6	***** Catchup *****		HW #3	HW #2
9/28	7	Combinatorial Circuit Design: Multi-bit output functions; standard combinatorial circuits (enabler decoder, encoder, priority encoder, mux	M&K 3.1, 3.3, 3, 3.6-3.9		
9/30	8	Arithmetic funcs: Adder (half, full, ripple-carry, adder-subtractor); Contraction; Shifter	M&K 4.1-4.2, 4.5 9.4	HW #4	HW #3
10/5	9	Sequential Circuitry: Latch, Flip-Flops, timing issues	M&K 5.1-5.3, 5.6		
10/7	10	Sequential Circuit Analysis & Design: State machines	M&K 5.4-5.5	HW #5	HW #4
10/12	11	PLAs; ROM; Register Design: Load and Transfer	M&K 6.8, 7.1-7.3		
10/14	12	Register Design cont'd: MicroOps and Counters, mux and serial transfer	M&K 7.5-7.6, 7.8-7.9		HW #5
10/19	13	***** Catchup and/or Midterm review *****			
10/21	14	**MIDTERM** (in class)			
10/26	15	Memory Design	M&K 8.1-8.7		
10/28	16	Processor Design: Datapath, ALU	M&K 9.1-9.5	HW #6	
11/2	–	**ELECTION DAY - NO CLASS!**			
11/4	17	Control Word; Simple Arch; Instruction Decoder	M&K 9.6-9.8	HW #7	HW #6
11/9	18	Instruction Types and Formats	P&H 2.1-2.6		
11/11	19	Branches, stacks, heaps, immediate addressing	P&H 2.7-2.8, 2.10	HW #8	HW #7
11/16	20	Single Cycle Datapath	P&H 4.1-4.4		
11/18	21	Single Cycle Datapath cont'd		HW #9	HW #8
11/23	22	Pipelining	P&H 4.5-4.6		
11/25	–	**THANKSGIVING - NO CLASS!**			
11/30	23	Hazards	P&H 4.7-4.8		
12/2	24	Cache & Cache Replacement Policies	P&H 5.1-5.2		
12/7	25	***** Catchup and/or review *****			HW #9
12/9	26	***** Catchup and/or review *****			
Tentative 12/21 9am-12pm		**FINAL EXAM**:	Location TBD		