WEEK #1: September 8-10

Introduction.
Course overview, recent trends, modern digital design and systems.

Combinational Logic: Quick Review.
Boolean representations, two-level/multi-level logic, structured blocks. Finite bases.

Sequential Logic: Latches/Flipflops (Quick Overview).

WEEK #2: September 15-17

Sequential Logic: Registers and Shift-Register Counters.
Johnson counters, linear feedback shift-registers (LFSR’s) for pseudo-random number generation.

Sequential Logic: Clocked State Machine Design.
Controller design procedure: Moore and Moore machines. Timing issues.
Sequential optimization: optimal state encoding, state minimization.

WEEK #3: September 22-24

Sequential Logic: Clocked State Machine Design.
Complex modeling case studies, deriving a specification.

Sequential Logic: Iterative Circuits.
Unrolling FSM’s: designing fast combinational pattern detectors, comparators.

Introduction to VHDL. Combinational Modeling.
Basic combinational modeling examples. Formal syntax. Entities and architectures.

WEEK #4: September 29-October 1

Introduction to VHDL. Combinational Modeling (cont.).
Libraries and packages. Structural, dataflow and behavioral modeling.
Selected and conditional signal assignment statements, for-generate statements.
Multi-bit operations; delta delays, simulation semantics.
Advanced Topics (1): FPGA Internals.
Actel and Xilinx case studies. Gate-level industrial structures.

WEEK #5: October 6-8

Arithmetic Circuits (1): Basic Combinational Adders.
Ripple-carry adder review. Von Neumann’s average worst-case carry-chain analysis.

Arithmetic Circuits (2): Advanced Combinational Adders.
High-Speed Adders: carry-select, conditional sum, carry-skip, carry-lookahead.
Tradeoffs between delay, area and power. Strategies: parallelism vs. speculation.
Introduction to ternary/higher-radix arithmetic.

WEEK #6: October 13-15

Arithmetic Circuits (2): Advanced Combinational Adders (cont.).
Parallel-prefix (tree) adders: Kogge-Store, Brent-Kung. Hybrid structures, saturating arithmetic.

Arithmetic Circuits (3): Combinational Array Multipliers.
Basic version. Performance optimization using carry-save addition.

Sequential VHDL.
Modeling flip-flops, registers, state machines: templates and practical strategies.
WEEK #7: October 20-22
Low-Power Digital Techniques (1).
Recent approaches: sequential precomputation architectures.
Low-Power Digital Techniques (2).
Recent approaches: low-power bus encoding.

WEEK #8: October 27-29
Fault-Tolerance and Reliability: Error Detection and Correction.
Basic principles; parity, Hamming and extended Hamming codes.

MIDTERM: THURSDAY, OCTOBER 29 (in class).

WEEK #9: November 3-5 [NO CLASS 11/3: Election Day]
Fault-Tolerance and Reliability: Error Detection and Correction (cont.).
Two-dimensional (product) codes, cyclic redundancy check (CRC) codes.
Introduction to Asynchronous Design: Overview.
Motivation and recent industrial advances. Handshaking protocols, data encoding, completion detection.

WEEK #10: November 10-12
Digression: Floating Point Arithmetic.
Single- and double-precision representation. FP-integer conversion, FP multiplication.
Special cases: overflow, zero, infinity, rounding issues, advanced modes.
Algorithmic State Machine charts (ASM’s).

WEEK #11: November 17-19
Architectural Synthesis: Register-Transfer Level (RTL) Design (cont.).
Specification and design procedure for large complex digital systems. Detailed case study.
Control vs. datapath extraction. Timing issues.
Optimizations: resource sharing, scheduling, inner loop acceleration.

WEEK #12: November 24-26 [NO CLASS 11/26: Thanksgiving]
Architectural Synthesis: Register-Transfer Level (RTL) Design (cont.).
System-level performance tuning, parallel vs. serial operation, area/delay/power tradeoffs.

WEEK #13: December 1-3
Asynchronous Design: Controllers.
Clockless controller synthesis: “burst-mode” specifications.
The Columbia “MINIMALIST” CAD tool, case studies and tutorial.
Asynchronous Design: High-Speed Pipelines.
MOUSERTRAP pipelines. Handling non-linear topologies, applications.

WEEK #14: December 8-10
Crossing clock domains: synchronizers, metastability, synchronization failure, practical solutions.
Advanced Topics (2): Soft Error Mitigation.
Recent techniques for robustness to transient failures (due to cosmic rays).

FINAL EXAM (TENTATIVE). Thursday, December 17, 1:10-4:00 p.m. (Room: TBA)