WEEK #1: September 6-8

Introduction.

Course overview, recent trends, modern digital design and systems.

Combinational Logic: Quick Review.

Boolean representations, two-level/multi-level logic, structured blocks. Finite bases.

Sequential Logic: Latches/Flipflops (Quick Overview).

WEEK #2: September 13-15

Sequential Logic: Registers and Shift-Register Counters.

Johnson counters, linear feedback shift-registers (LFSR's) for pseudo-random number generation.

Sequential Logic: Clocked State Machine Design.

General counter design procedure. State machine structures: Moore vs. Mealy.
Controller design procedure: Moore and Moore machines. Timing issues.
Sequential optimization: optimal state encoding, state minimization.

WEEK #3: September 20-22

Sequential Logic: Clocked State Machine Design.

Complex modeling case studies, deriving a specification.

Sequential Logic: Iterative Circuits.

Unrolling FSM's: designing fast combinational pattern detectors, comparators.

Introduction to VHDL. Combinational Modeling.

Basic combinational modeling examples. Formal syntax. Entities and architectures.

WEEK #4: September 27-29

Introduction to VHDL. Combinational Modeling (cont.).

Libraries and packages. Structural, dataflow and behavioral modeling.
Selected and conditional signal assignment statements, for-generate statements.
Multi-bit operations; delta delays, simulation semantics.

Advanced Topics (1): FPGA Internals.

Actel and Xilinx case studies. Gate-level industrial structures.

WEEK #5: October 4-6

Arithmetic Circuits (1): Basic Combinational Adders.

Ripple-carry adder review. Von Neumann's average worst-case carry-chain analysis.

Arithmetic Circuits (2): Advanced Combinational Adders.

High-Speed Adders: carry-select, conditional sum, carry-skip, carry-lookahead.
Tradeoffs between delay, area and power. Hybrid structures, saturating arithmetic.
Strategies: parallelism vs. speculation. Introduction to ternary/higher-radix arithmetic.

WEEK #6: October 11-13

Arithmetic Circuits (3): Combinational Array Multipliers.

Basic version. Performance optimization using carry-save addition.

Sequential VHDL.

Modeling flip-flops, registers, state machines: templates and practical strategies.

WEEK #7: October 18-20

Low-Power Digital Techniques (1).

Recent approaches: sequential precomputation architectures using clock gating.

Low-Power Digital Techniques (2).

Recent approaches: low-power bus encoding.

WEEK #8: October 25-27

Fault-Tolerance and Reliability: Error Detection and Correction.

Basic principles; parity, Hamming and extended Hamming codes.

MIDTERM: THURSDAY, OCTOBER 27 (in class).

WEEK #9: November 1-3

Fault-Tolerance and Reliability: Error Detection and Correction (cont.).

Two-dimensional (product) codes, cyclic redundancy check (CRC) codes.

Introduction to Asynchronous Design: Overview.

Motivation and recent industrial advances. Handshaking protocols, data encoding, completion detection.

Digression: Floating Point Arithmetic.

Single- and double-precision representation. FP-integer conversion, FP multiplication.
Special cases: overflow, zero, infinity, rounding issues, advanced modes.

WEEK #10: November 8-10 [NO CLASS 11/8: Election Day]

Architectural Synthesis: Register-Transfer Level (RTL) Design.

Algorithmic State Machine charts (ASM's).

WEEK #11: November 15-17

Architectural Synthesis: Register-Transfer Level (RTL) Design (cont.).

Specification and design procedure for large complex digital systems. Detailed case study.
Control vs. datapath extraction. Timing issues.
Optimizations: resource sharing, scheduling, inner loop acceleration.

WEEK #12: November 22-24 [NO CLASS 11/24: Thanksgiving]

Architectural Synthesis: Register-Transfer Level (RTL) Design (cont.).

System-level performance tuning, parallel vs. serial operation, area/delay/power tradeoffs.

WEEK #13: November 29-December 1

Advanced Topics (1): Synchronous Timing Issues and Challenges.

Crossing clock domains: synchronizers, metastability, synchronization failure, practical solutions.

Asynchronous Design: High-Speed Pipelines.

MOUSETRAP pipelines. Handling non-linear topologies, applications.

Asynchronous Design: Controllers.

Clockless controller synthesis: "burst-mode" specifications.
The Columbia "MINIMALIST" CAD tool, case studies and tutorial.

WEEK #14: December 6-8

Asynchronous Design: Hazard-Free Logic Minimization.

Hazards and combinational logic. Exact hazard-free 2-level logic minimization.
Safe multi-level "hazard-non-increasing" transformations.

Advanced Topics (2): Approximate Computing.

Recent approaches using approximate arithmetic with limited error rates for low power.

Advanced Topics (3): Soft Error Mitigation.

Recent techniques for robustness to transient failures (due to cosmic rays).

FINAL EXAM (TENTATIVE). Thursday, December 22, 1:10-4:00 p.m. (Room: TBA)