Characterization of Soft Errors Caused by Single Event Upsets in CMOS Processes

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Abstract—Radiation-induced single event upsets (SEUs) pose a major challenge for the design of memories and logic circuits in high-performance microprocessors in technologies beyond 90nm. Historically, we have considered power-performance-area trade offs. There is a need to include the soft error rate (SER) as another design parameter. In this paper, we present radiation particle interactions with silicon, charge collection effects, soft errors, and their effect on VLSI circuits. We also discuss the impact of SEUs on system reliability. We describe an accelerated measurement of SERs using a high-intensity neutron beam, the characterization of SERs in sequential logic cells, and technology scaling trends. Finally, some directions for future research are given.

Index Terms—High performance, error tolerance, reliability, soft error, single event upset.

1 Introduction

Electronic circuits encode information in the form of a charge stored on a circuit node or as a current flowing between two circuit nodes. For example, one bit of static memory contains two nodes that store two complementary charges corresponding to logic "1" and logic "0." The bit values "1" and "0" can be stored as node charges "10" and "01," respectively. A static memory makes use of feedback to continuously replenish the charge on both nodes. The stored bit value can be preserved indefinitely as long as noise originating from the interconnect coupling or other sources does not overwhelm the stored charge. During the write operation, the state is intentionally modified by coupling the charge via bitlines.

With the development of CMOS technology, the area per bit scales down and is about $1\mu m^2$ in a 90nm technology [1]. To prevent excessive material wear or even breakdown caused by high electric fields, the supply voltage has to scale down with the decreasing transistor dimensions to about 1.2V. The net effect is that the node charge reduces at least linearly with the channel length. Already in 1962 [2], it was pointed out that, if the channel length scales below $1\mu m$, a single cosmic ray particle strike would short-circuit the source, drain the terminals of a transistor in the off state, and potentially disrupt the circuit. The first reports of failures attributed to cosmic rays emerged in 1975 when space-borne electronics malfunctioned during a magnetically quiet time, when it was unlikely that the failures were due to spacecraft charging [3]. In 1978, similar problems were observed in dynamic memories at ground level [4]. After the memory had been written, the values of some of the bits had randomly changed. They appeared as errors after reading out and comparing the state of the memory array with the original data. The memory was not damaged and, if the same data were stored again, after some time the errors would reappear at different locations. Due to their nonpermanent, nonrecurring nature, these errors were called *soft errors*.

The failures were traced to alpha particles emitted from a small number of impurities found in the plastic packages. At the time, materials such as sealing glasses, fillers, alumina, and plastic contained several parts-per-million of radioactive isotopes uranium-238 and thorium-232 and their daughter products. Even such small quantities were sufficient to produce a flux of several alpha particles per cm^2 per hour, leading to one soft error per day in a 4 kbit DRAM chip. The *soft error rate* (SER) due to alpha particles can be greatly reduced by improving the purity of the materials and, to some extent, by shielding the die from the package. In 1979, it was predicted that the secondary particles created in interactions of cosmic rays with the atmosphere could cause soft errors in ground-based electronics [5]. In the same year, errors due to neutrons and protons were observed in laboratory conditions [6]. An error due to a hit of a single particle was termed a *single event upset* (SEU).

The first measurements of cosmic ray SERs at ground level were conducted by O'Gorman in 1983 [7]. After three years of measurements underground, at sea level, and at elevated altitudes, the two leading causes of soft errors were confirmed to be alpha particles and cosmic rays. The former, originating from the chip itself, do not depend on altitude; as impurities decay over time, the alpha-particle-SER will change. The latter, originating from space, decrease exponentially with the amount of shielding. The atmosphere acts as a natural shield, decreasing the SER by nearly three orders of magnitude.

After the discovery of soft errors, semiconductor companies (Intel, IBM, Fujitsu, etc.), aerospace companies (Boeing, Ericsson-Saab Avionics), government organizations (Sandia National Labs, Jet Propulsion Laboratory, NASA), and universities initiated independent research programs addressing various aspects of the problem. In

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1993, neutron-induced soft errors were found in a computer on board a commercial aircraft [8]. A 256 kbit SRAM showed failures at a rate of one error per chip in 80 days. In the same year, Alan Taber from IBM and Eugene Normand from Boeing demonstrated a strong correlation of the in-flight error rates with 1-10 MeV atmospheric neutron flux [9].

In 1995, a new mechanism, namely, errors due to boron-10 activated by low energy atmospheric neutrons, was observed in DRAMs [10]. After this discovery, borophospho-silicate glass (BPSG) that contained natural boron and the isotope boron-10 was removed from the manufacturing processes. In 1996, a survey of computer log files showed that a supercomputer with 156 Gbit of DRAM could fail several times per day [11] and the incidence of soft errors in implanted pacemakers was about the same as if the errors were caused by background neutron radiation [12]. Currently, the main effort is focused on improving the accuracy of SER models and finding cost-effective methods of reducing failure rates.

In this paper, we review the current status of SER modeling methodology. Starting from the basic interactions of particles with silicon, we cover the charge-collection mechanisms on diodes, the effects on simple circuits, and various manifestations of SEUs in large circuits, e.g., microprocessors. We review measurement techniques suitable for SER model development in 90nm and future technologies. We compare the conclusions of several neutron and alpha-particle SER scaling studies (most of them published in the last five years) and give suggestions for future research.

2 Particle Generation and Interactions

The terrestrial radiation environment consists of >92 percent neutrons, ~4 percent pions, ~2 percent protons, and sea-level muons generated by cosmic ray interactions in the Earth's atmosphere. Charged particles create a direct ionization in semiconductor devices, causing a current surge that is responsible for errors in the memory and processing elements of a computing system. Highly abundant neutrons do not have electrical charges; their effects occur through nuclear collisions that give rise to charged particles, which in turn cause ionization. The amount of ionization and the current surge in a given semiconductor device are directly proportional to the energy lost by radiation particles. In silicon, an average energy of 3.6 eV is required to create one electron-hole pair. This value depends on the energy gap between the valence and conduction bands of a given semiconductor.

Primary cosmic ray protons interact with the Earth's magnetosphere upon approach. The intensity of these cosmic rays varies by about 20 percent during an 11-year solar cycle [13]. The Earth's magnetic field bends the particles' trajectories. It also deflects low energy particles away into the space. Only those protons entering vertically into the poles are not affected by the Earth's magnetic field. The effect of the magnetic field on protons determines the minimum energy required of a charged particle to enter the atmosphere at a given location. This energy defines the *geomagnetic rigidity* of a primary proton to cause cosmic ray showers at a given location on the Earth's surface. Thus, we see the latitude-dependence of the secondary radiation on the Earth, which increases by a factor of 1.6 from the equator to the poles [14]. In addition, alpha particles originating from some of the metals used in integrated circuit (IC) fabrication also cause SEUs.

2.1 High-Energy Neutrons

Neutrons are generated in the atmosphere by high-energy cosmic ray particles through direct nuclear spallation reactions and the creation and decay of radioactive nuclei. The energy of neutrons generated in spallation reactions tends to be high, in the range of 20-300 MeV, whereas neutrons evaporating from radioactive nuclei are much lower in energy (a fraction of an eV to a few MeVs).

2.1.1 Altitude Dependence

Neutrons exhibit strong altitude dependence due to the wide variations in air pressure (from 700 to $1,033\mathrm{g/cm^2}$) over the surface of the Earth. Air pressure plays a significant role in causing neutron-generating reactions and in transporting neutrons to ground level. An intense neutron environment exists at higher altitudes in the atmosphere, 10-40km and more above the surface. The maximum intensity occurs at the Pfotzer point at 15km. Below the Pfotzer point, absorption of secondary particles prevails, leading to a much lower neutron intensity at the sea level, where the typical flux is only 20 neutrons per $\mathrm{cm^2}$ per hour (>10 MeV, New York City, see [13]).

2.1.2 Nuclear Interaction in Silicon

Neutrons interact with matter through inelastic nuclear collisions with the nuclei in the host lattice. During these collisions, a primary knock on atom (PKA) gets kicked out of a lattice site in the semiconductor materials. PKA has a very high linear energy transfer (LET). It causes ionization and displacement damage in semiconductor devices, thereby causing SEUs and the degradation of electrical properties. The cross-section that represents the probability of occurrence for nuclear collisions is extremely low. Hence, one out of 40,000 neutrons hits a silicon nucleus in the first 10μm of thickness of a device [13].

2.2 Alpha Particles

Alpha particles are emitted by various radioisotopes undergoing radioactive decay. Metals such as lead, which is a daughter product of the naturally radioactive decay chain of uranium-238, emit alpha particles with kinetic energy in the range of 3-6 MeV. Such low-energy alpha particles have a range of 15 to 30μm in silicon and are very effective in causing single even upsets in memory. Alpha particles are also generated by (n,α) nuclear reactions induced by slow neutrons (energy range of 0.0253 to 100s of eV) in various nuclei. Elements such as natural boron used in the doping of semiconductors contain the isotope boron-10 (~20 percent), which has a very high cross-section (~5,000 barns) for (n,α) reactions [15]. Upon absorbing a slow neutron, boron-10 splits into an alpha particle with ~1.5 MeV energy and a lithium nucleus, both capable of causing ionization with high LET. Boron-10-related SEUs have been demonstrated in DRAMs [10] and SRAMs [16]. In fact, due to the large number of thermal neutrons in natural

radiation and a large reaction cross-section, boron can result in as many as 81 percent of the SEUs in a 0.25μm SRAM [17]. Most subquarter-micron manufacturing processes do not use boron-10 anymore. Alpha particles from radioactive impurities remain an important source of errors in SRAMs and other sensitive circuits.

2.2.1 Alpha Particle Interactions in Silicon

Alpha particles, despite their lower LET and kinetic energy, are capable of causing SEUs. Even extremely pure materials such as semiconductor wafers contain the radioactive impurities of uranium-238 and thorium-232 and their daughter products in part-per-billion (ppb) concentrations. Uranium-238 decays to lead-206 with a half-life of $4.51^{*}10^{9}$ years by emitting 8 alpha particles with energies of 4.1 to 7.7 MeV. Thorium-232 decays to lead-208 with a half-life of $1.41^{*}10^{10}$ years via the emission of six alphas with energies of 0.6 to 6.8 MeV. In silicon, 1 MeV of energy corresponds to 44.5fC of charge, which is more than enough to flip the state of a logic circuit. Most alpha particles are emitted from solder balls and materials used in IC packaging.

To avoid alpha particles emitted from metals (such as lead), one must make a clever selection of older and aged metals. The older metals, smelted hundreds of years ago, have gone through many half-lives of decay, hence they are relatively free of the alpha particle emission in comparison with newer metals. Current methods can resolve impurity concentrations of about 1ppb, corresponding to a flux of about $0.001\alpha/\mathrm{cm}^2/\mathrm{hr}$ [18]. This is not sufficient for the requirements of the semiconductor industry. There is a need to advance metrology methods to about $0.0001\alpha/\mathrm{cm}^2/\mathrm{hr}$ [19]. As the electronic industry moves toward a lead-free technology, there should be some decrease in alphas emitted from solder joints. However, the contribution from the package, on-chip interconnects, and wafers will remain largely unchanged.

2.3 Radiation in Space

There is an ever-increasing interest in using commercial off-the-shelf (COTS) electronics in space missions, both in the aerospace industry and NASA. It is worth mentioning here the radiation environments that would be encountered by electronics in space. Space near the Earth has cosmic rays in addition to the protons and electrons trapped in the magnetic field. These cosmic rays consist of >93 percent protons, ~6 percent alpha particles, and a remainder of heavy nuclei (up to uranium) with very high energies. Trapped proton energy varies from a few MeV to 500 MeV, whereas trapped electron energies vary from 10s of keV to several MeVs. Away from the Earth in interplanetary space, during quiescent solar periods, the radiation environment takes the form of a cosmic radiation background. During intense solar activity and flares, there is a several orders of magnitude increase in proton and electron flux both near and far from the Earth. Such storms also affect the near-Earth and terrestrial radiation environments. Unlike the terrestrial radiation environment, which is primarily dominated by secondary neutrons, the space radiation environment is made up of radiations with a wide range of energies, from tens of KeV/nucleon to hundreds of MeV per nucleon.

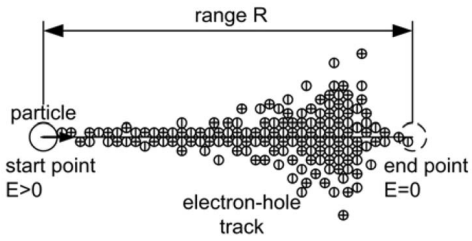

Fig. 1. Electron-hole track created by charged particle.

2.4 Particle Tracks in Silicon

SEUs or soft errors are caused by concentrated bursts of excess charge generated at random locations in a semiconductor substrate and subsequently collected by the drain diodes of the MOS transistors. These bursts of free electrons and holes appear to be due to ionizing radiation in much the same way as the photodiode forward current appears to be due to absorbed photons. A single photon of visible light carries energy of 1-2 eV and can generate about one electron-hole pair in silicon, corresponding to 0.00016fC of charge. In comparison, a circuit node in a 90nm CMOS technology stores 1-10fC of charge. Therefore, single photons do not cause SEUs. Other particles, such as alpha particles emanating from decaying impurities, carry energy of the order of 3-10 MeV, corresponding to more than 100fC of charge. This charge is sufficient to alter the logic state of a circuit node. However, not all of the charge produced in the substrate is collected by the diodes. In fact, most of the electron-hole pairs either recombine or are collected on reverse-biased PN junctions that are shorted to a power supply rail without disturbing the normal operation of the circuit. A PN junction connected to a vulnerable circuit node can only collect charges from its immediate vicinity. The collection volume is approximately defined by the diode area and the collection depth. For a 90nm process, the collection depth and collection volume are about 1μm and $1\mu\mathrm{m}^3$, respectively. The fraction of the total charge within the collection volume depends strongly on the ionizing particle, its energy, and its path of travel through silicon. Next, we will describe the spatial and temporal distribution of charge generated by various ionizing particles.

An ionizing particle can originate from the outside of a chip (e.g., an alpha particle emitted by a package impurity) or from within the chip (e.g., a secondary particle of a neutron collision with silicon). These particles possess kinetic energy and move rapidly through the substrate. As they move, they encounter the negatively charged electrons and the positively charged nuclei of the surrounding atoms. Gradually, the particle loses all of its kinetic energy to ionizations and displacement damage.

Fig. 1 shows a diagram of a particle track. The distance from the starting point of a particle track to the point where the particle stops is called range. A particle generally moves along a straight path perturbed by collisions. The rate at which a particle loses its energy, dE/dR, is called stopping power or linear energy transfer (LET) and depends on the mass, energy, and charge of the particle, and the host material. The lost energy is converted into charge at a rate of 3.6 eV per e-h pair in silicon and 4.8 eV per e-h pair in

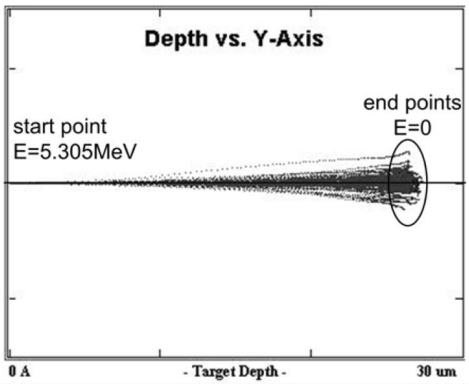

Fig. 2. Distribution of range of 100 alpha particles with energy $\mathrm{E_R} = 5.305\mathrm{MeV}$ in silicon target.

gallium arsenide. The trajectory of a stopping particle is not unique for identical initial conditions due to the randomness of the collisions with the atoms of the host material.

Fig. 2 shows 100 trajectories of alpha particles with an initial energy of 5.305 MeV obtained from simulation code SRIM [20]. The projected range is 28μm. There is uncertainty in the value of the projected range and in the deviation of the particle track from the straight path. For purposes of SEU calculations, approximating the trajectory by a straight path is acceptable. Note that Fig. 2 does not show any lateral dimensions of a track, i.e., the initial distribution of charge in the direction perpendicular to the motion of the particle. The initial charge density decreases rapidly within 10-100nm in the direction perpendicular to the particle trajectory.

Fig. 3 shows the calculated range for various secondary particles that emerge from the collisions of atmospheric neutrons with silicon nuclei. At an energy of several MeV, light particles have smaller stopping power, shown in Fig. 4, and longer range. The maximum stopping power is called the Bragg peak. SEUs occur when sufficient energy (or charge) is deposited within the collection volume. The particle has to exceed a certain minimum LET as it crosses the collection volume and the portion of the track around the Bragg peak is the most *effective* in causing upsets. However, the portion of the track that is most *probable* to cause upsets depends on the energy spectrum of the particles as well as the minimum LET requirement. The stopping powers have been verified experimentally by measuring the energy difference of a particle passing

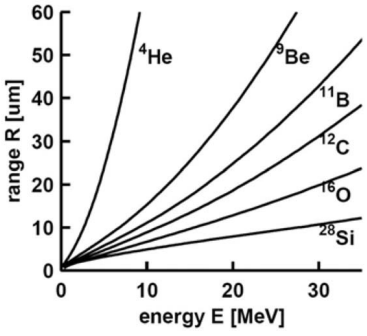

Fig. 3. Range in silicon as a function of energy.

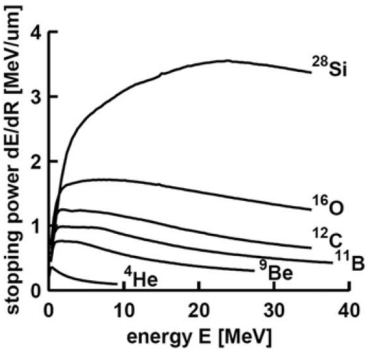

Fig. 4. Stopping power in silicon.

through a thin foil. Also, stopping powers can be converted from one material to another based on the material's density. The lateral dependency of the initial distribution of charge has been studied by Monte Carlo simulations [21] and theoretical models have been developed [22]. Experimental verification is very difficult and limited mostly to qualitative measurements of the track width in nuclear emulsion [23]. For the particles in Fig. 3 with energy of 10 MeV, it takes less than 6 picoseconds to stop in silicon and about 1ps to create a track within the collection volume. This time is comparable to the dielectric relaxation time of silicon and the time it takes for the energy to be converted to a free charge. The track-generation time is becoming comparable to the gate delay of CMOS circuits in advanced technologies (~10ps).

Once the initial electron-hole distribution is established in the substrate, the carriers are subject to drift, diffusion, and recombination. Charge-collection effects have been extensively studied both analytically [24], [25], [26], [27], [28] and using device simulators [29], [30], [31], e.g., DESSIS from ISE [32]. Identical tracks produced at different locations will have different effects on the circuit.

Fig. 5 shows a simplified diagram of N- and P-type MOSFETs. Three identical particle tracks are shown at locations below the N+ drain, crossing the N+ drain, and crossing the P+ drain and N-well. Charge collection was simulated for a 0.6μm process and drain diodes were approximated by cylinders to reduce the problem to quasi two dimensions and shorten the simulation time. The track of an 8.29 MeV magnesium-25 ion with a 5μm range and a total charge of 368fC was used.

Fig. 6 shows the resulting current transients observed at the N+ drain due to Tracks I and II (simulated separately) and at the P+ drain due to Track III. Note that the collected charge (138-225fC) is significantly less than the generated charge. The ratio of the collected to the generated charge is

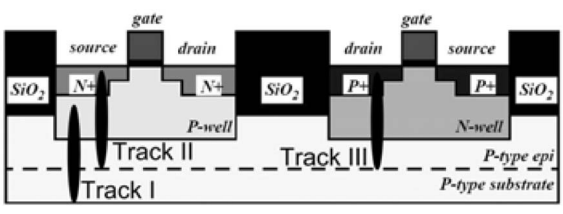

Fig. 5. Three examples of particle tracks.

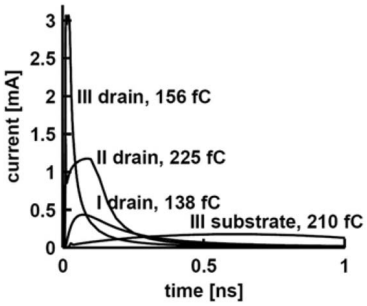

Fig. 6. Collected charge for tracks outside (I) and through N+ drain (II) and through P+ drain (III).

called the *collection efficiency*. The current due to Track II is larger in amplitude than for Track I. This is because Track I is closer to the drain diode and has a larger overlap with the collection volume. Tracks II and III are produced at the same location, only the type of the drain is different, and the P+ drain diode resides inside N-well. Track III results in a much smaller collected charge than does Track I because some portion of the charge is inside the collection volumes of both the P+ drain diode and the N-well diode. This charge is divided between the two PN junctions, which results in a smaller charge being collected on a P+ drain than on an N+ drain. A much lower upset rate of P+ drains compared to N+ drains in an N-well process has been confirmed experimentally [33].

The time dependency and the total amount of collected charge depend on the applied voltage across the diode, as shown in Fig. 7.

With a larger applied voltage, the depletion region width, collection depth, and volume increase, which results in a larger collected charge. A higher voltage and a larger electric field in the depletion region result in a faster charge collection transient. The distribution of charge in a particle track depends on the particle type and energy. Fig. 8 shows the collected charge for seven particles with a range of 5μm. The initial energies can be found from Fig. 3. Heavier particles have much larger LET for the same range, which results in about a factor-of-10 difference in the collected charge. The variation in the time constant is much smaller. The collected charge and the time constant are both important in determining whether a specific circuit fails. The collection waveforms obtained from a device simulator

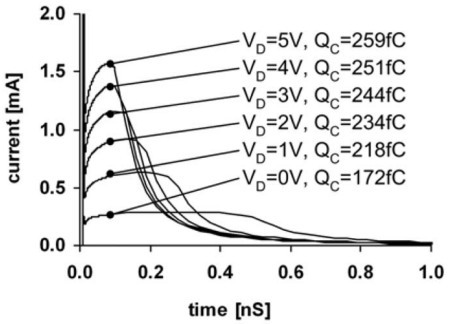

Fig. 7. Variation of collected charge and current waveform shapes with applied drain voltage.

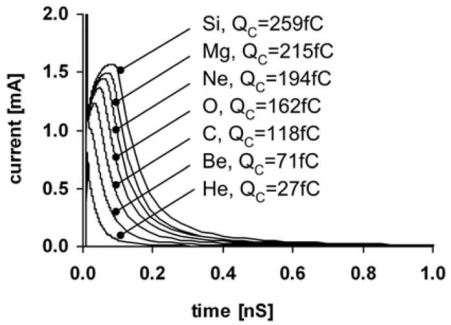

Fig. 8. Collected charge for various secondary particles with track length of 5μm.

are scaled in magnitude and injected on circuit nodes to perturb the normal operation of a circuit and determine the SER. At the cost of a longer simulation time, a better accuracy can be obtained with mixed device-circuit simulations [34], [35] or 3D simulations of a simple circuit, e.g., SRAM cell [36].

3 Impact on Circuits and Systems

An SEU is a transient event that lasts about 100ps (Figs. 6, 7, and 8). If a charge disturbance on a circuit node is smaller than the noise margin, the circuit will continue to operate properly. Otherwise, the disturbed voltage may be interpreted as the opposite logic state and the circuit will malfunction. There is a difference in the response of dynamic circuits and static circuits with and without regenerative feedback. A dynamic node is affected by the total collected charge and the change in voltage is inversely proportional to node capacitance. A static node that has a glitch will eventually recover to its original state unless there is regenerative feedback that adds to the glitch and reverses the logic state of the node. Sequential circuits that use regenerative feedback is described in Section 3.1. In an actively clocked circuit, an SEU on any node has a finite probability of causing a glitch that may propagate to an input of a sequential cell, get latched as a wrong value, and affect the machine operation. We describe such events and their impact in Section 3.2. This section concludes with a discussion of the block-level impact of SEUs.

3.1 Memory and Sequential Circuits

Fig. 9 shows a typical static RAM (SRAM) cell in an on-die memory. The word line (WL) is low, and the cell is holding its stored data using the back-to-back inverter configuration. The bitlines BL and BL# are decoupled from the memory cell by NMOS transistors. If a particle strike causes one of the nodes to transition, the disturbance may

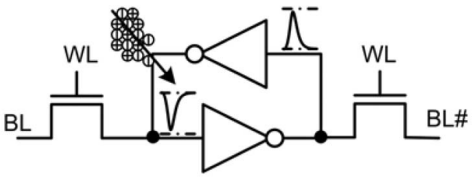

Fig. 9. SRAM cell.

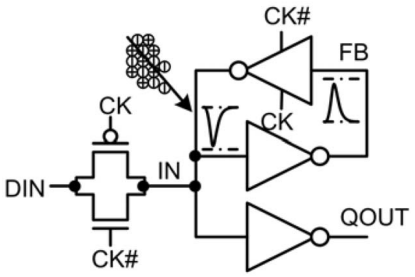

Fig. 10. Static latch cell.

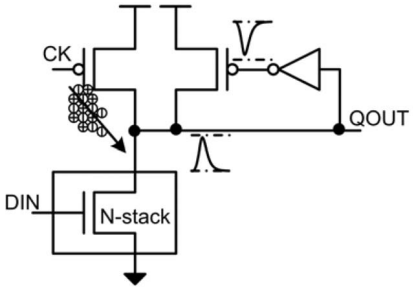

Fig. 12. Domino circuit.

propagate forward through the inverter and cause a transient on the second node. Since the second node, in turn, drives the first node toward a wrong value, this regenerative action will cause both nodes to flip. Hence, the memory cell will reverse its state and store a wrong data value. Once the cell flips, there is no mechanism for its recovery other than explicitly rewriting the state via the bitlines. Soft errors can also be caused by particle strikes on bitlines [37]. During the read operation, a bitline is discharged by a small current from a memory cell. The data bit is read as a "0" or "1" based on the voltage differential developed on the bitline during the cell access period. This voltage differential is disturbed if a particle strikes close to a diode of an access transistor of any of the cells on that bitline. Error correction codes (ECC) [38] with redundant storage of data can be implemented to correct both types of errors when the data is read out.

Similar state changes can occur in the core logic. The typical sequential elements in the core logic are a latch (Fig. 10), a register file cell (Fig. 11), or a domino cell (Fig. 12). Unlike a memory, the core logic often is not designed as a regular array and does not lend itself to ECC protection. In some implementations of the latch in Fig. 10, the FB and Q_{OUT} node may be merged, i.e., there is only one forward inverter. The impact of an SEU is similar to that in an SRAM cell, except that the transistors in the latch are larger and the inverters have varying strengths. For example, the inverter driving the output is stronger than the one driving node IN. The backward inverter is clocked to prevent contention during a latch write operation. The Q_{OUT} node in the domino cell in Fig. 12 is strongly driven by a precharge PMOS transistor during the precharge phase. When the N-stack evaluates and pulls Q_{OUT} strongly toward ground, the cell is quite resilient to SEUs. So, the domino cell is vulnerable to a particle strike mostly when it is in the evaluation phase and the N-stack does not evaluate [39].

3.2 Combinational Logic

SEUs can cause a voltage transient on any node in a circuit. The transient may propagate through the combinational stages and eventually be latched by a sequential element, as shown in Fig. 13. Many transients will not be latched. Some of the latched data may not be relevant to machine operation and there will be no perceivable error in the program operation. Hence, the effective SER of a large combinational circuit needs to be derated. Three types of derating are applied to a typical circuit for calculating its SER [40].

- **Logical masking**. Fig. 14 explains logical masking [41]. If the strike happens on an input to a NAND (NOR) gate, but one of the other inputs is in the controlling state (e.g., $0(1)$ for a NAND (NOR) gate), the strike will be completely masked and the output will be unchanged, i.e., this particle strike will not cause a soft error. In order for an error to propagate, there must be a sensitized path from the input to the output.
- **Temporal masking**. As the transient propagates towards a sequential element, e.g., a latch shown in Fig. 15, the noise on node *DIN* may be outside the latching window of all the latches in the subsequent combinatorial paths [40]. Hence, the error will not be latched, and there will be no soft error. This is called temporal masking.
- **Electrical masking**. Finally, as all CMOS circuits have limited bandwidth, transients with bandwidths higher than the cutoff frequency will be attenuated [42]. The pulse amplitude may reduce, the rise and fall times increase, and, eventually, the pulse may evaporate (Fig. 16). This phenomenon is called

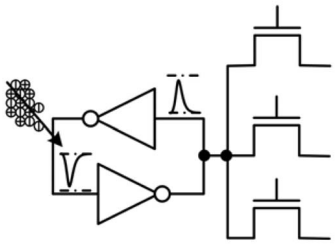

Fig. 11. Multiport register file cell.

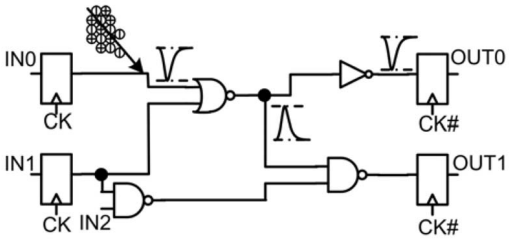

Fig. 13. Random logic block.

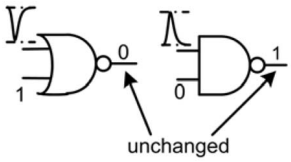

Fig. 14. Logical masking.

electrical masking. On the other hand, since most logic gates are nonlinear circuits with substantial voltage gain, low-frequency pulses with sufficient initial amplitude will be amplified.

3.3 Block-Level Impact

Computing the SER of a larger block is a two-step process. In the first step, raw error probabilities are calculated from device-level models for each circuit node. In the second step, the raw probabilities are derated and combined [43], [44]. From a user's perspective, we have to differentiate between the detected and corrected errors, the detected and uncorrected errors, and the undetected errors [45]. Corrected errors do not cause any harm and can be ignored. Detected uncorrectable errors (DUEs), such as parity errors, usually cause an exception or system crash and are included in the block-level SER estimation. Undetected errors may cause silent data corruption (SDC) in the sense that wrong computations may go on undetected, corrupt a significant portion of data, and, eventually, cause the system to hang or crash. SDCs are the most catastrophic type of error; therefore, the requirement on the maximum SDC rate is usually stricter than the requirement on DUEs. SDCs must be separately accounted for in SER estimations. Consider a memory bit corrupted by a particle strike. If the memory is rewritten by new data before it is read, the error will be erased and will never propagate to the machine state. In this case, there is no need to consider the error in SER calculations. If the erroneous bit is read and the memory is ECC protected, then the error will be repaired and need not be included in SER calculations. If the memory only has parity protection on a word, then the word containing the erroneous bit will be detected, but the error cannot be repaired because parity protection cannot identify which bit within the word is corrupted. This error must be included in SER as a DUE. If the memory does not have any ECC or parity protection and the wrong bit is read and used in a computation, it will likely affect the program outcome and should be counted as an SDC.

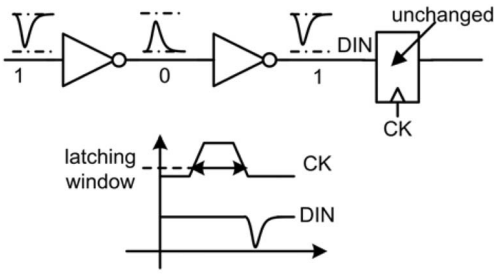

Fig. 15. Temporal masking.

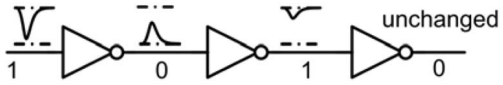

Fig. 16. Electrical masking.

ECC and parity are effective against single-bit errors within a logic word. ECC with double-error detection can be implemented by appending an additional bit to a single-error-correcting ECC, e.g., a Hamming code [37]. More effective ECC requires more redundancy and is seldom used in mainstream commercial circuits. Only about 2 percent of all SEUs result in the simultaneous upset of two physically adjacent bits in a 90nm cache SRAM [46]. The percentage of multibit errors remains about the same as memory density increases [46], [47]. Intelligent memory organization with physical interleaving makes the physically adjacent, multibit errors appear as single-bit errors in multiple logic words, which can be detected by a parity checker and corrected by single-error-correcting ECC. In a combinational circuit, a single particle strike can affect multiple outputs because the induced transient can propagate through multiple combinational logic paths and get latched at multiple locations. Various studies have been performed to quantify the effect of one strike that affects multiple bits [43], [44].

4 Measurement of SER

In the normal operation of a product, many environmental factors can cause errors: power supply noise, charge sharing, crosstalk, SEUs, etc. It is not easy to separate the sources of errors and identify a particle-induced soft error. One exception is measurement at high altitudes or on-board airplanes since the neutron flux increases by nearly three orders of magnitude at flight altitudes (Section 2). In-flight measurements have been instrumental in validating the accuracy of accelerated measurements using human-made, high-intensity particle sources [8], [9], [48] and for measurements of the atmospheric neutron flux [14], [49]. Since a typical device SER is very low under normal conditions [50], it is more practical to measure the SER under accelerated conditions and then scale the measurements back to natural conditions. In this section, we describe methods of obtaining alpha and neutron-induced SERs. Major portions of this and the following sections will focus on the neutron-induced SER, which dominates in most circuits. Although advances in packaging and fabrication have gradually reduced the effect of the alpha-particle-induced SER, it remains important in SRAMs and DRAMs. Hence, we briefly comment on measurements of the alpha SER. Detailed guidelines for performing both field and accelerated alpha and neutron SER measurements can be found in the dedicated JEDEC standard [51].

4.1 Neutron-Induced SER

Two mechanisms lead to neutron-induced SEUs (Section 2). Since boron-10 is not used in most new technologies, a reader interested in methods of measuring the boron-induced SER can find more information in the following papers [10], [16], [17], [52], [53]. It should be noted that the

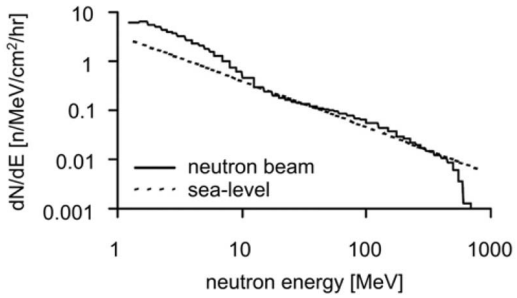

Fig. 17. Neutron energy spectrum.

boron-induced SER may dominate in technologies that use BPSG. In technologies that do not contain boron-10 in large concentrations, the main SEU mechanism is the collision of a high-energy neutron (1-1,000 MeV) with a nucleus of, e.g., silicon. Accelerated measurement of the neutron-induced SER is complicated because high-energy neutron beams are not widely available.

To cover the range of energies, three approaches have been used.

1. The preferred method [51] is to use a "white" neutron beam with an energy spectrum similar to the atmospheric neutron spectrum, e.g., the neutron beam at Weapon Neutron Research (WNR) in Los Alamos National Laboratory (Fig. 17) [54]. At WNR, neutrons are produced in spallation reactions of 800 MeV protons incident on a tungsten target. This beam has been widely used for SEU testing [55], [56], [57], [58], [33].
2. The second approach is to deconvolve the energy dependency of the SER from measurements with quasi-monoenergetic neutron sources at several peak energies and then calculate the SER for the atmospheric energy spectrum [59], [60].
3. The third approach is to use a proton beam as an approximation of neutrons at energies 50-100 MeV and above [61], [62].

The advantage of a proton beam is its wide availability. It is much easier to produce a monoenergetic proton beam with high intensity since the protons can be accelerated to a specific energy. Neutrons, however, have to be produced by accelerating charged particles, e.g., protons, which collide with a target and then produce the neutrons as secondary particles. A target that is thinner than the absorption length ($\sim$ 100-200g/cm^2) will result in a low neutron intensity and quasi-monoenergetic spectrum, while a thick target will result in a higher intensity and "white" spectrum. Because the median neutron energy for an SEU appears to decrease with technology scaling [63], proton beams may produce less accurate results. Another disadvantage of proton beams is the total dose damage to the tested parts, which is a concern if the supply of the parts is limited (test chips or prototypes).

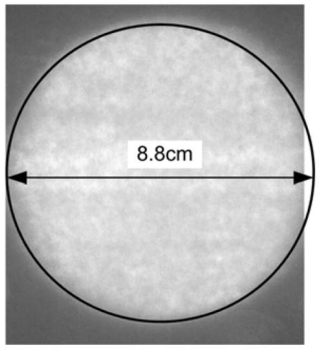

Fig. 19. Measurement of beam cross-section by exposed Polaroid film.

Fig. 18 shows a typical experimental setup at WNR. The neutron beam enters from the left, passes through a uranium fission detector chamber, and continues toward the circuit boards with the devices under test (DUT) [64]. The detector produces a number of pulses proportional to the neutron flux. The pulses are accumulated by a counter set up outside the beam area. The beam can be turned on and off by blocking the beam entrance with a massive concrete shutter. The test chips are loaded with a known data pattern. The beam is turned on for several minutes to several hours, after which the shutter is closed and the data patterns are read out along with the pulse count. The permanently installed LANSCE detector tracks the neutrons energy spectrum and the number of pulses at the location of the detector chamber. With the increasing distance from the detector, the diameter and intensity of the beam changes.

Fig. 19 shows the diameter of the beam immediately after the detector. This picture was obtained by placing a Polaroid film in the beam path for 10-20 minutes. It is important that the beam covers the entire DUT. From measurements of the beam diameter at several locations along the beam path, we calculated a correction factor for beam intensity at the location of the DUT (Fig. 20).

The beam cross-sectional area increases with the distance from the detector. Since the total number of neutrons in the beam is constant, the beam intensity drops inversely

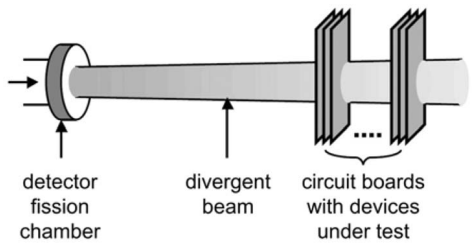

Fig. 18. Measurement of neutron SER.

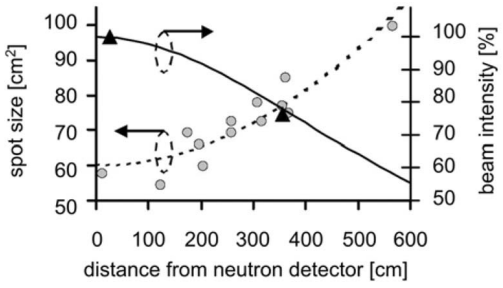

Fig. 20. Correction for distance from the source.

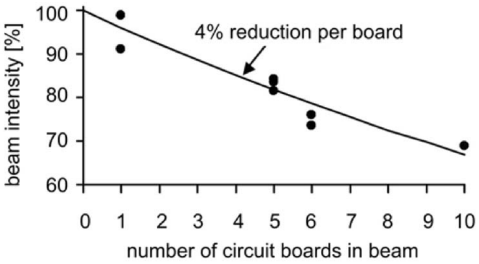

Fig. 21. Correction for beam attenuation due to multiple boards simultaneously placed in beam.

proportional to the beam area. The net effect is a 9.5 percent reduction in beam intensity for each 100cm increase in distance. Two calibration SER measurements (shown by triangles) at two locations confirmed the relative decrease in the beam intensity obtained from the film exposures. As shown in Fig. 18, multiple boards and experiments were arranged in the beam path. We observed a significant reduction in the beam intensity due to absorption and scattering effects in the circuit boards. By placing various numbers of boards in front of one of the experiments, the intensity was calculated to decrease by 4 percent for each additional board (Fig. 21). The boards were populated by packaged parts on both sides, resulting in a total board thickness of 1.5cm. The neutron flux measured by the detector was corrected for the distance and absorption effects.

4.2 Alpha-Particle SER

Alpha particles are produced by radioactive impurities with low concentrations. Accelerated measurements can be performed by exposing a DUT to a material with a much higher concentration of radioactive alpha-emitting isotopes, such as americium-241, uranium-238, or thorium-232. Such radioactive sources are commercially available in the form of a thin foil, or a disk. However, they should be handled only by trained personnel and stored properly to prevent health hazards. Alpha particles are absorbed within 5-8cm in air and several 10μm in silicon. The top of the circuit die has to be directly exposed, which makes it difficult to test circuits in flip-chip packages. The packages suitable for alpha testing are, for example, dual-in-line (DIL) and similar wirebond type packages with pads around the perimeter of the die. The package lid needs to be removed. A typical experimental setup is shown in Fig. 22. A radioactive foil was mounted in close proximity to and parallel to the die. The foil was calibrated

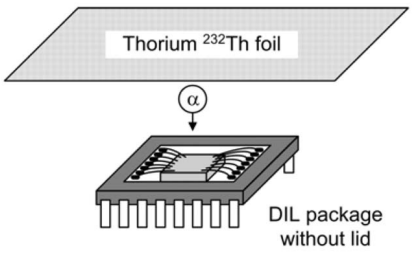

Fig. 22. Measurement of alpha-particle SER.

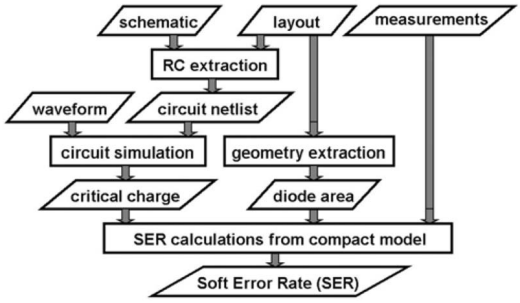

Fig. 23. Process characterization flow.

by a counter to gauge its alpha emission. After the die had been exposed for a predetermined time, the foil was removed. The data pattern was read out to determine the count and location of the errors. As the chip is not exposed during data read/write, the error location is captured accurately. From the alpha activity of the foil, exposure time, and error count, it is possible to calculate the SER under natural conditions.

5 Process Characterization

5.1 Methodology

The goal of process characterization with respect to an SEU is to quantify the impact of various parameters, e.g., supply voltage, transistor size, circuit topology, doping, and well structure, on the SER of a product. Process characterization consists of modeling and experimental validation. The experimental part should provide an accurate SER for a few types of circuits under several operating conditions. The modeling part should provide a model that calculates the SER for the conditions in which measured data is not available. Physical models capturing the underlying mechanisms leading to SEUs are especially useful because they allow the results to be extrapolated to future technologies [65], [66], [67], [68], [69], [70].

Fig. 23 shows a typical process characterization and modeling flow. The schematic and layout databases are used to generate an annotated netlist of the circuit, describing the connectivity of transistors and various, mainly capacitive, parasitic components. A device simulator is used to estimate a charge collection waveform for the specific manufacturing process and supply voltage (Section 3.4). The current waveform is used to perturb the normal operation of the circuit and to determine the minimum critical charge, Q_{CRIT}, leading to an SEU. The layout database also provides the physical sizes of the drain diodes, which, together with Q_{CRIT}, are fed into a compact model to determine the SER of the circuit. Measurements provide the SER for a limited number of critical charges and diode areas. These experimental data are used to improve the accuracy of the compact model. Careful selection of a test circuit is important in order to decouple the effects of critical charge, transistor type, and diode area, and also to cover a sufficient range of values of these parameters [71], [72]. Static memory requires fine spacing and a large die size, making it a preferred reliability test vehicle in developing a logic manufacturing process. Static memories

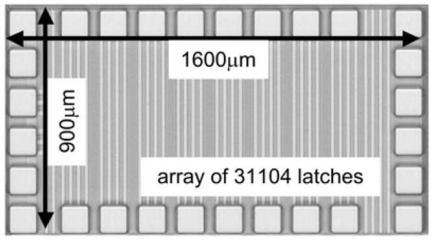

Fig. 24. Testchip photograph.

are often used for SER measurements. Unfortunately, the number of data points is limited, and the cell symmetry makes it difficult to separate the upsets on P+ and N+ drain diodes.

A latch-based test circuit in Fig. 24 solves this problem by making one of the nodes more sensitive to upsets than the others. In Fig. 25, collection node *cnode2* has low capacitance and is driven by a weak inverter. The SER of the latch is due mostly to an SEU on *cnode2*. The critical charge can be varied within a factor of two by varying the supply voltage. To measure the dependency on the diode area, explicit P+ and N+ diodes were added. By adding diodes, the capacitance of *cnode2* increases, and the Q_{CRIT} of the circuit changes. Due to the process variations and uncertainty in the collection waveform, it may be difficult to precisely determine Q_{CRIT}. To decouple the SER's dependency on the diode area from its dependency on Q_{CRIT}, it is desirable for Q_{CRIT} to remain constant over a range of diode area. This can be accomplished by keeping the total diode area constant and varying only the ratio between the N+ and P+ diode area.

5.2 Application to a 90nm CMOS Process

The test chip was fabricated in a 90nm process and the neutron-induced SER was measured at Los Alamos National Laboratory (Section 4.1) [64]. The SERs of N+ and P+ diodes were measured independently by programming the collection node to high and low voltage, respectively. The correlation of the errors measured at various supply voltages is shown in Fig. 26.

On the X-axis, we plotted the number of errors for the nominal process voltage of 1.2V. The Y-axis shows the equivalent measurements, i.e., for the same circuit, diode type, and size, at voltages other than 1.2V. The gray and black symbols represent N+ and P+ diodes, respectively. The SER increases by 2x when the voltage is reduced from 1.2V to 0.8V. Over the range of measurements, the SER

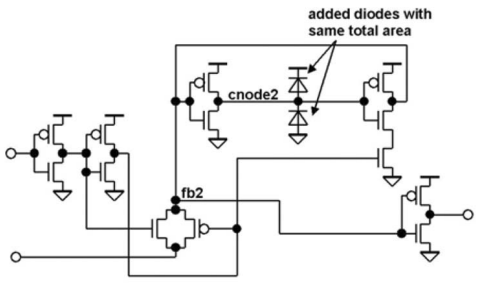

Fig. 25. Latch description with explicit diodes.

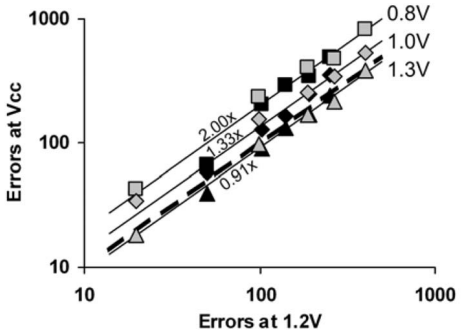

Fig. 26. SER dependency on supply voltage.

increases by 18 percent for every 10 percent reduction in the supply voltage. SER dependency on the N+ diode area is shown in Fig. 27. All the diodes had a square shape and identical Q_{CRIT}. Fig. 27 shows that the SER increases linearly with the N+ diode area. In the same way, we measured dependency on the P+ diode area. The relative sensitivity of N+ and P+ diodes was determined by calculating the ratio of the measured error rates (Fig. 28). The N+ drain diode exhibited 2.2x higher sensitivity than the P+ drain diode. This means that, for the same transistor width and Q_{CRIT}, the N-type MOSFET is 2.2x more prone to an SEU than the P-type MOSFET. This effect is caused by the lower collection efficiency of the P+ drain inside the N-well, as explained in Section 2.4 in connection with Fig. 6.

A similar difference in the sensitivity of N+ and P+ diodes was measured for a 0.6μm process [33]. The measurements were used to calibrate an SER model that was later validated by independent SER measurements on SRAM [64]. The model is now used to estimate the SER of products and to optimize designs for reduced SER [39], [73].

6 Technology Scaling Trends

6.1 Cell-Level Trends

The scaling of process technology results in a simultaneous change of several parameters that affect the SER. Assume that the length and the supply voltage scale by a factor of K per generation, where $K = 0.7$. The scaling of the supply voltage actually slowed down beyond 130nm, but, for simplicity, this fact will be ignored. Then, the node capacitance scales as K, the node charge as K^2, and the collection area as K^2. For unhardened circuits, the critical charge Q_{CRIT} is comparable to the node charge and scales as

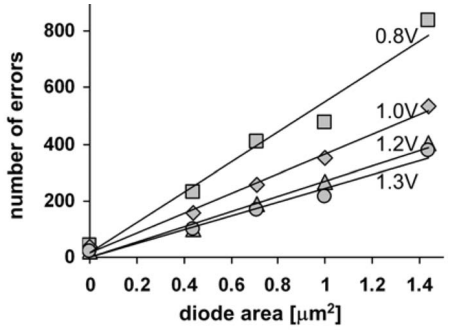

Fig. 27. SER dependency on diode area.

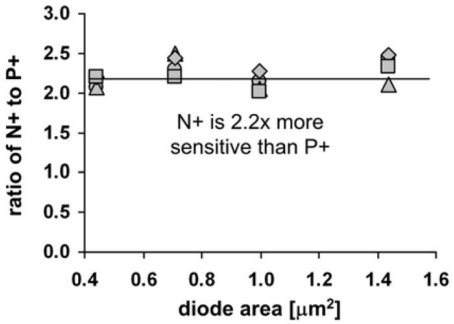

Fig. 28. Relative error rate of N+ and P+ drains.

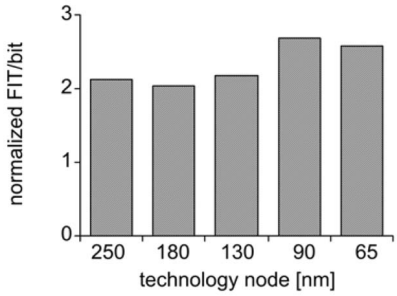

Fig. 29. Scaling of neutron SER in SRAM.

K^2. As Q_{CRIT} decreases, the SER becomes worse. As the collection area decreases, the SER improves. In addition, the collection efficiency (or collection depth, for collection-volume-based models) decreases with increased substrate doping and reduced bias voltage, which tends to reduce the SER. The net result of these compensating effects can be either an increasing or decreasing SER per cell.

The first scaling studies for the space environment, published in 1982 by Pickel [74] and Petersen et al. [75], concluded that the SER per bit in SRAM should remain approximately constant. Depending on the assumptions of charge collection mechanism, called funneling, the SER per bit might increase approximately linearly [74]. The scaling of the SER at ground level is complicated due to the aggregate effect of the alpha particles, high-energy neutrons, and, possibly, thermal neutrons.

6.1.1 Contributions of Various Mechanisms

Alpha particles have a lower stopping power than secondary particles of neutron collisions. The dependence of the SER on Q_{CRIT} has a much steeper slope for alpha particles than for neutrons. At a lower Q_{CRIT}, e.g., for SRAM cell, alphas contribute about as much as neutrons to the total SER [76]. In latches and combinational logics that have Q_{CRIT} several times larger than SRAM, neutrons usually dominate. The SER due to thermal neutron interactions with boron-10, if present in raw materials used in the fabrication process, exhibits a less steep trend with Q_{CRIT} compared to alphas due to the additional contribution from lithium. The thermal neutron SER may dominate in circuits with a lower Q_{CRIT} [17]. With technology scaling, the relative contribution of alphas increases compared to that of neutrons. In the past, this trend has been counteracted by using materials with a lower concentration of alpha-emitting impurities [77].

6.1.2 Neutron SER Scaling

A scaling study on SRAM published in 2000 was based on an extrapolation of the measurements in a 0.6μm technology [33]. The study concluded that the neutron-induced SER per bit decreases approximately as K, i.e., by a factor of 0.7 per generation [78]. Recent measurements on commercial SRAM vary in their conclusions about scaling. In [79], the neutron SER in 6T cells increased by 2x per generation from 0.25μm to 0.14μm. Granlund et al. [80] found that the SER decreased by 2x from 0.5μm to 0.25μm node and then increased by 4x from 0.25μm to 0.14μm. This nonmonotonic trend was explained by a disproportionate scaling of Q_{CRIT} with respect to collection efficiency. A 2004 study from IBM [81] showed a decreasing trend of several 10 percent per generation. Intel reported an increase of only 8 percent per generation, from 0.25μm to 90nm [64]. This trend is shown in Fig. 29. The measurements were extrapolated to a 65nm node.

6.1.3 Alpha SER Scaling

It should be noted that most of the studies based on calculated or extrapolated projections assume that the alpha-particle flux due to impurities does not scale. However, semiconductor manufacturers estimate the product-level alpha-SER during the process development. If an unacceptable increase is discovered, measures are taken to lower the SER. Therefore, the actual trends measured on products often show a different trend than the projections.

A 1995 study of the alpha-SER in a multiplier found a 10x increase from 0.6μm to 0.12μm, which translates to an increase of 1.8x per generation [82]. Cohen et al. projected a dramatic three-orders-of-magnitude increase, from 0.25μm to 50nm, corresponding to a 4x increase per generation [83]. In contrast, Dai et al. [84] found that, as Q_{CRIT} gets smaller, the alpha particle SER/bit will saturate; this agrees with some earlier projections [85] and was subsequently confirmed by measurements [86]. Roche et al. measured an approximately constant alpha SER in 0.25μm and 130nm SRAM [87].

6.1.4 Scaling of Total SER in Memories

Although the SER was initially discovered in DRAM, the rapid scaling in size of a cell and the much slower scaling of storage capacitance improved the SER/bit in DRAM by three orders of magnitude, from 1Mb to 16Mb generation [55]. Some of this reduction was accomplished by modifying the processing technology [62]. There were no significant modifications to the SRAM cell design, which resulted in a slow increase in the SER/bit and a rapid increase in the chip-level SER due to a rising number of bits per chip [88]. The system-level SER can be reduced by ECC, although some SRAM manufacturers began implementing capacitor structures such as those used in DRAM [89], [90], [91].

6.1.5 Scaling in Latches

The neutron SER dominates in latches due to a higher Q_{CRIT} than SRAM [76]. Karnik et al. projected that the SER per latch would increase by 10 percent per generation if voltage

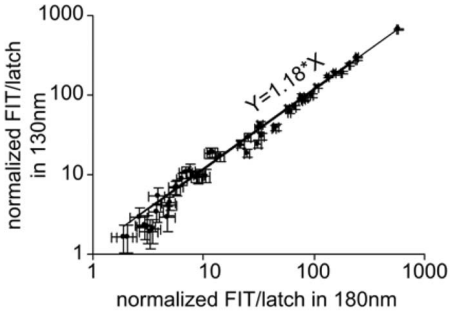

Fig. 30. Neutron SER scaling for latches in two process generations (optical shrink, same voltage).

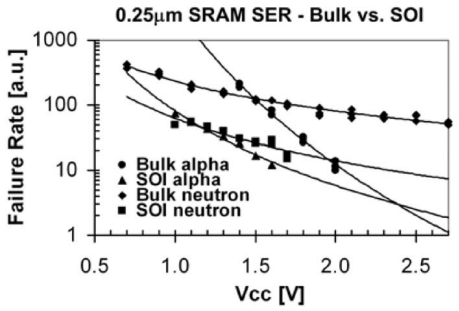

Fig. 31. Comparison of alpha and neutron SERs for bulk and SOI technologies.

were scaled by 0.8x [72]. The actual measurements showed an 18 percent higher SER for various 130nm latches compared to 180nm latches at the same voltage (Fig. 30). The 130nm test chip was a direct optical shrink of the 180nm test chip.

6.1.6 SOI Improvement over Bulk

A partially depleted SOI technology has advantages over a bulk technology because of a lower junction capacitance, better noise isolation, and a somewhat higher packing density due to the absence of substrate taps. A smaller substrate thickness results in a lower collection volume, which improves the SER. However, forward bias of the substrate during a charge collection transient results in an opening of a parasitic bipolar transistor. Amplification of the collected charge diminishes the benefit of SOI over bulk at a point when they become equally sensitive to SEU [85]. The reduced substrate thickness in SOI results in a profound reduction of the SER [92]. Fig. 31 shows the measured SRAM SER for neutrons and alphas for 0.25μm bulk and SOI technologies [86]. The SER for SOI is 5x lower than for bulk and this difference is about the same for neutrons and alphas. A similar ratio of 6-7x was reported for SRAM in 130nm and 90nm technologies [81], [87]. The SEU benefit of SOI is enhanced by retrograde substrate doping [93]. Hardened SOI technologies that use substrate taps can reduce SER close to 100x compared to bulk [94], [95].

6.2 Chip and System-Level Trends

Due to the increasing packing density, the uncorrected, chip-level SER increases rapidly for SRAM. The rising SER in DRAM (due to the increasing number of bits) has been compensated for by decreasing the SER/bit. Microprocessors and similar chips are a mixture of memory and logic cores that contain sequential and combinational logic. It has been argued that, with an increasing clock frequency and a higher level of pipelining, the contribution of the logic will dominate the chip-level SER [96]. Today, virtually all of the high-performance microprocessors use ECC protection on the major memory arrays and a large part of the residual SER can be attributed to the logic cores. The measurements on Alpha processors from 0.35μm to 0.18μm have not indicated a dramatic increase in the total SER [77]. Similarly, 120 MeV proton tests of IA-32 microprocessors did not show a significant increase in SEU cross-sections [97]. However, a rapidly increasing number of bits and growing complexity pose some unique challenges to the design of reliable memories, microprocessors, and other integrated circuits in the future.

7 Future Challenges

7.1 New Materials

With clock speeds surpassing 1GHz, on-chip global interconnects have become a bottleneck in increasing microprocessor performance. To reduce intrinsic wire delay, aluminum interconnects were replaced by copper interconnects around the 130nm node. To further lower wire delay, the 90nm node saw an introduction of a low-K carbon-doped oxide interlayer dielectric (ILD) in the metal stack. The conventional scaling of MOS transistors results in a prohibitively large gate and subthreshold leakage. This forced the process engineers to look for performance elsewhere. Strained silicon, such as SiGe with 10-20 percent of germanium, offers higher channel mobility without increasing leakage. Extrinsic source and drain resistance was reduced by using cobalt or nickel silicide. In the near future, we can expect high-K materials to replace SiO_2 as the MOS gate oxide and, eventually, the geometry of the transistor may change.

With the new materials and structures being introduced, SER modeling is having a hard time keeping up-to-date. In fact, most SER models assume that the only material contributing to SERs is silicon. First-order calculations suggest that the neutron-induced SER should increase with the mass density of a material. Heavy materials, e.g., copper, tantalum, tungsten, and cobalt, are abundant in the immediate vicinity of the MOS transistors and could actually contribute to an increase in the SER by a factor of two or more [98]. It is desirable to address the SER impact of these new materials in a timely manner in order to prevent future reliability hazards similar to boron-10. Accurate nuclear models take a long time to develop, mainly because they must cover a wide range of neutron energies. For silicon, the energy range of 10 MeV to 1,000 MeV is usually sufficient, but a wider range may be required for other materials. Another difficulty comes from the lack of experimental neutron cross-sections at high energies (>100 MeV).

7.2 Modeling and CAD Tools

SER modeling proceeds in several steps covering the radiation environment, nuclear physics, particle track generation, charge collection, circuit response, and the manifestation of errors in the system. Several of the steps involve statistical events with many degrees of freedom. For example, a particle strike can occur at various locations in the circuit and, at any given time, the circuit can be in various states. The complexity of the phenomenon requires decoupling of the parameters so that only a small number of parameters are considered simultaneously. The raw SER is usually calculated by averaging the effects of particle strikes over the angles of incidence and locations, then binning them by the collected charge. Next, the impact on the circuit is found by assuming that the circuit is in a steady state with a well-defined critical charge that determines the probability of a node upset. The contributions of the SER of various nodes are summed up to arrive at the total SER of the circuit.

On the system level, the SER of each circuit is derated according to the usage scenario. A derating factor gives the probability that a circuit actually produces an output or stores data that is vital to the correct operation of the circuit. How to efficiently estimate the derating factors for complex circuits is one of the difficult issues of high-level SER modeling. Given that a particular node in a circuit flips into the opposite state for a certain amount time, what is the probability that it results in an erroneous output? The problem lies in the large number of possible circuit states compounded by the large number of circuit nodes that can be upset. An innovative approach is needed that does not result in an exponential explosion of simulation time due to the size of the circuit, an approach that could potentially handle circuits as large as a whole microprocessor.

Gradually, some of the assumptions used by the models become invalid. For example, in the modeling of particle tracks, the lateral charge distribution is often not well known. With the channel length scaling below 90nm, the transistor size actually approaches the diameter of a typical particle track. In the device simulations, it is assumed that a particle track is generated almost instantly or much faster then the response time of the circuit. With the inverter gate delay as low as 10ps, this assumption may no longer hold. In the modeling of a circuit response, only one node is upset at a time. It has been shown in the example of an SRAM cell, that simultaneous charge collection by several nodes may lower the apparent critical charge for upset. Considering collection of charge by even two nodes at a time adds significant complexity and it is not clear how to efficiently handle it for more complex circuits. Another challenge comes from the fact that many circuits are not in a steady state. Depending on when a strike occurs, the critical charge of a node may vary. Currently, the only way to account for this variation is to run multiple simulations of particle strikes at various times and perform a statistical summation.

A more efficient method is clearly needed to shorten simulation times. In the past, a lot of effort was focused on memories. With the memory protected by ECC, the residual SER comes from the sequential elements (latches, register files) and the combinational logic. Some work has been done on the modeling of propagated transients in the combinational logic, but more focus is needed in developing efficient simulation methods that can be applied to a large variety of circuits without excessive intervention or expertise from the user. Such tools demand comprehensive validation by fault injection experiments and measurements.

7.3 SER Mitigation

A technical challenge of building reliable systems out of unreliable components is nothing new. If anything, the reliability of a single MOS transistor inside an IC is much higher than that of a vacuum tube or a discrete transistor. However, for a system without redundancy, the probability of error-free operation decreases rapidly with increases in component count. For example, consider an advanced microprocessor with about 1 billion transistors and an application that requires a mean time to failure (MTTF) of 100 years. To meet this requirement, a single transistor would have to reach an MTTF of 100 billion years. Apparently, this may be hard to achieve. Fortunately, many fault-tolerant techniques have been developed, especially for memories. The difficulty is not in improving the reliability, but in doing it cost effectively and without degrading the speed or increasing the power consumption. What is the most efficient way of protecting a complex system like a microprocessor? Should we try to identify and solve the reliability bottlenecks, such as latches and register files? At some point, there may be so many bottlenecks that the overhead of protecting each circuit separately just would not be acceptable. Is it better to add redundancy in software? Protecting a larger and more complex system increases the error detection latency and may make system recovery more complicated. There is a need for application-specific, fault-tolerant techniques that offer a trade off between the reliability improvement and amount of overhead.

8 Conclusion

We presented an overview of the current status of soft error rate (SER) methodology. Technology scaling trends indicate a moderate increase in the SER/bit or SER/latch. Due to routine SEU modeling, measurements, product validation, and hardening by semiconductor manufacturers, this trend has not been reflected in product SERs. It is important to continue these efforts in order to deliver reliable products at affordable prices.

Appendix

Definitions of Acronyms

DIL	dual-in-line, package type
DUT	device under test
SEU	single event upset, an error caused by a single particle hit
MBU	multiple-bit upset
SER	soft error rate, number of errors in time
FIT	failure in time, number of errors in 10^9 hours
MTTF	mean time to failure

SDC	silent data corruption
LET	linear energy transfer, energy loss divided by distance of a particle propagating through target material
PKA	primary knock on atom
RAS	reliability, availability, serviceability
ECC	error-correction code
SRAM	static random access memory
DRAM	dynamic random access memory
IC	integrated circuit
ppb	parts per billion, concentration of 10^{-9}
COTS	commercial off-the-shelf
NASA	National Aeronautics and Space Administration
MOS	metal-oxide-semiconductor
e-h pair	electron-hole pair
SRIM	stopping and range of ions in matter (simulation code)
BPSG	boro-phospho-silicate glass, used as dielectric in some semiconductors

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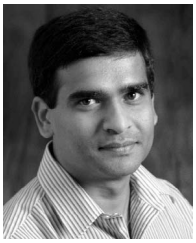

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