

Conditional Sum Adders: Detailed Implementation

In this handout, we illustrate the functionality of an 8-bit conditional sum adder. The block diagram of 8 bit Conditional Sum Adder is drawn on next page.

The basic idea in the conditional sum adder is to generate two sets of outputs for a given group of operand bits, say, k bits. Each set includes k sum bits and an outgoing carry. One set assumes that the eventual incoming carry will be zero, while the other assumes that it will be one. Once the incoming carry is known, we need only to select the correct set of outputs (out of the two sets) without waiting for the carry to further propagate through the k positions.

In this 8-bit Conditional Sum Adder, the first FA (with x_0 and y_0 input) takes c_{in} as carry in and generates carry-out. For x_1 and y_1 , we have two sets of adders with carry-in as 0 and 1 respectively. The final sum s_1 is the result of multiplex operation between the two sum generated with the select lines as carry-out generated by previous FA. The carryout of second addition is also multiplexed and sent as a select signal for higher bit additions as shown in figure. The concatenator simply groups the incoming bit lines to a wider sum-bus: it is not an actual hardware component, but rather indicates that two fields of input wires will be treated as a combined larger field of output wires.

Advantage: The addition is much faster as higher bit addition operation doesn't rely on carry propagation. However, the selection of correct result waits for the previous carry-out to be set.

Disadvantage: This is a relatively expensive design, as for $N=2^n$ -bit addition, it requires $2N-1$ full-adders and $2^{n+1} - n - 2$ multiplexers, which are not present in traditional ripple-carry adders.

