

CSEE 4823 Advanced Logic Design
Handout: Lecture #25
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Introduction to Approximate Computing
(follows Handout #42 paper)

Full Adder Designs: Mirror Adder (MA)

Conventional Mirror Adder = efficient transistor-level design

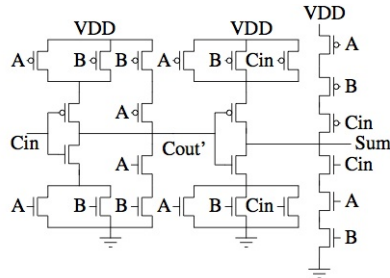


Fig. 1: Conventional MA

Figures courtesy of: V. Gupta, D. Mohapatra, S.P. Park, A. Raghunathan and K. Roy, "IMPACT: IMPrecise adders for low-power Approximate ComputIng," Proceedings of the IEEE Int. Symp. on Low-Power Electronics and Design (2011)

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Full Adder Designs: Mirror Adder (MA)

Simplified + Approximate Mirror Adders

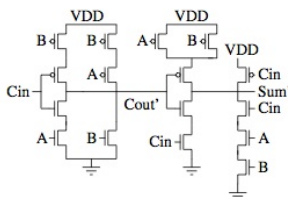


Fig. 2: Simplified MA

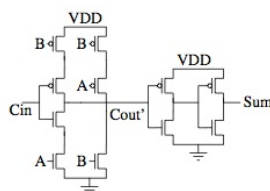


Fig. 3: MA approximation 1

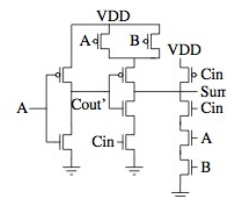


Fig. 4: MA approximation 2

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Full Adder Designs: Mirror Adder (MA)

Simplified + Approximate Mirror Adders: Layouts

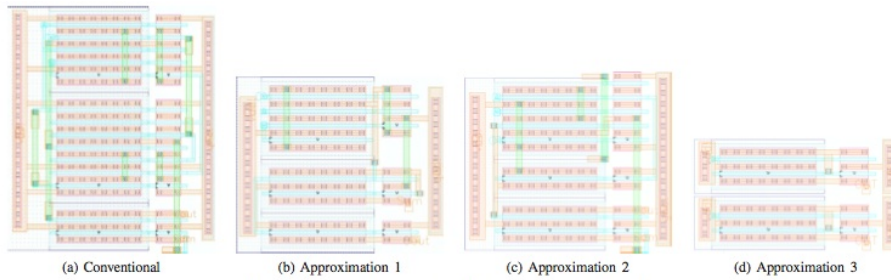


Fig. 5: Layouts of conventional and approximate MA cells

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Full Adder Designs: Mirror Adder (MA)

Accurate + Approximate Mirror Adders: Truth Table

TABLE I: Truth table for conventional full adder and approximations 1, 2 and 3

Inputs			Accurate outputs		Approximate outputs					
A	B	C_{in}	Sum	C_{out}	Sum_1	C_{out1}	Sum_2	C_{out2}	Sum_3	C_{out3}
0	0	0	0	0	1×	0✓	0✓	0✓	0✓	0✓
0	0	1	1	0	1✓	0✓	1✓	0✓	0×	0✓
0	1	0	1	0	0×	1×	0×	0✓	1✓	0✓
0	1	1	0	1	0✓	1✓	1×	0×	1×	0×
1	0	0	1	0	1✓	0✓	0×	1×	0×	1×
1	0	1	0	1	0✓	1✓	0✓	1✓	0✓	1✓
1	1	0	0	1	0✓	1✓	0✓	1✓	1×	1✓
1	1	1	1	1	0×	1✓	1✓	1✓	1✓	1✓

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Full Adder Designs: Mirror Adder (MA)

DSP Application areas: Discrete Cosine Transform (DCT) and Inverse DCT (IDCT)

- Approximate Mirror Adders: Output quality

(for 7-9 LSB bits using approximation)

- peak signal to noise ratio (PSNR)
- accurate 20-bit adder: PSNR = 31.16dB

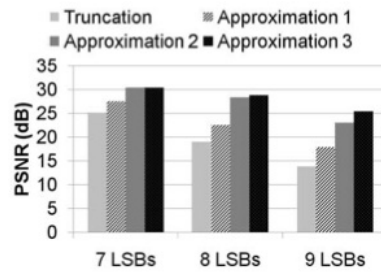


Fig. 8: Output quality for different techniques

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Full Adder Designs: Mirror Adder (MA)

DSP Application areas: DCT and IDCT

- Goal: use improved performance to reduce Vdd
 → for power savings

TABLE III: Operating voltages for different techniques

Technique	V_{DD} (V) for the 3 cases					
	7 LSBs		8 LSBs		9 LSBs	
	DCT	IDCT	DCT	IDCT	DCT	IDCT
Truncation	1.13	1.03	1.10	1.03	1.1	1
Approx. 1	1.18	1.05	1.1	1.03	1.1	1.03
Approx. 2	1.15	1.1	1.13	1.1	1.1	1.1
Approx. 3	1.14	1.02	1.11	1.01	1.1	1

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Full Adder Designs: Mirror Adder (MA)

DSP Application areas: **DCT and IDCT**

-power and area savings

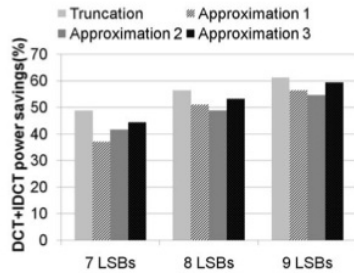


Fig. 9: Power savings for DCT+IDCT over the base case

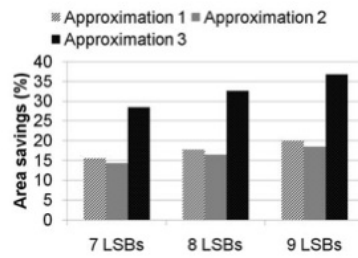


Fig. 10: Area savings for DCT+IDCT over the base case

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Full Adder Designs: Mirror Adder (MA)

DSP Application areas: **DCT and IDCT**

-overall quality metric for approximate designs

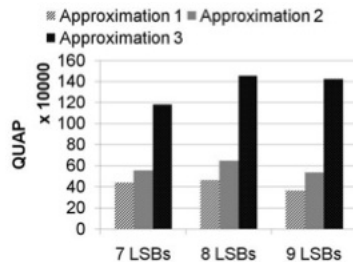


Fig. 14: Comparison of different approximations

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