Carry-Lookahead Adders (CLA’s) (hierarchical)
16-Bit Hierarchical CLA: Overall Architecture

Bitwise P/G Generation (level-0)

- $A_{0-15}$
- $B_{0-15}$
- $g_{0-15}$
- $p_{0-15}$

4-bit CLA

- $g_{12-15}$
- $p_{12-15}$
- $c_{15}c_{14}c_{13}$
- $G_{12/15}$ (4-bit group generate/propagate)

- $g_{8-11}$
- $p_{8-11}$
- $c_{11}c_{10}c_{9}$
- $G_{8/11}$ (4-bit group generate/propagate)

- $g_{4-7}$
- $p_{4-7}$
- $c_{7}c_{6}c_{5}$
- $G_{4/7}$ (4-bit group generate/propagate)

- $g_{0-3}$
- $p_{0-3}$
- $c_{3}c_{2}c_{1}$
- $G_{0/3}$ (4-bit group generate/propagate)

Sum Generation (level-n)

- $c_{16} = cout$ (optional)
- $G_{0/15}p_{0/15}$ (16-bit group generate/propagate for building larger adders)

- $G_{11/15}G_{8/11}G_{4/7}G_{0/3}p_{11/15}p_{8/11}p_{4/7}p_{0/3}$

- $S_{0-15}$

$16-Bit$ $Hierarchical$ $CLA$: $Overall$ $Architecture$
16-Bit Hierarchical CLA: Details of Cell Design

Level-0: Bitwise P/G Generation ➔ logic equations for bit i
\[ p_i = a_i \text{XOR} b_i \]
\[ g_i = a_i b_i \]

4-Bit CLA Cell: one example = bits 0-3 ➔ logic equations

**Carry Bits:**
\[ c_1 = g_0 + p_0 c_0 \]
\[ c_2 = g_1 + p_1 g_0 + p_1 p_0 c_0 \]
\[ c_3 = g_2 + p_2 g_1 + p_2 p_1 g_0 + p_2 p_1 p_0 c_0 \]

**Group P & G Bits:**
\[ G_{0/3} = g_3 + p_3 g_2 + p_3 p_2 g_1 + p_3 p_2 p_1 g_0 \]
\[ P_{0/3} = p_3 p_2 p_1 p_0 \]

Level-N: Sum Generation ➔ logic equations for bit i
\[ s_i = p_i \text{XOR} c_i \]