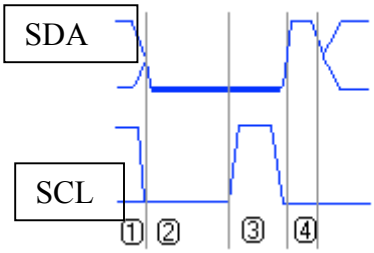
Handout #27c
CSEE 4823x
Professor Steven Nowick
"I^{2}C Ack"

This text is a modification of it original form. Modifications were made by Melinda Agyekum and Steven Nowick. The original text can be found at:
http://www.esacademy.com/en/library/technical-articles-and-documents/miscellaneous/i2c-bus.html

I2C Bus Events: Getting Acknowledge from a slave (as a receiver)

When an address or data byte has been transmitted onto the bus then this must be ACKNOWLEDGED by the slave(s). In case of an address: If the address matches its own then that slave and only that slave will respond to the address with an ACK. In case of a byte transmitted to an already addressed slave, then that slave will respond with an ACK as well.



The slave that is going to send an ACK holds the SDA line low immediately after reception of the 8th bit transmitted, or, in case of an address byte, immediately after evaluation of its address. In practical applications this will not be noticeable.

This means that as soon as the master pulls SCL low to complete the transmission of the bit(1), SDA will be pulled low by the slave (2). When SDA is pulled low by the slave, all data transfers on SDA is prevented until SDA is released.

Next, the master will issue a clock pulse on the SCL line (3), which signals an ACK transmission. The slave will release the SDA line upon completion of this clock pulse (4), allowing for the master to regain control.

In case of data being written to a slave, this cycle must be completed before a stop condition can be generated. The slave will be blocking the bus (SDA kept low by slave) until a clock pulse is generated on the SCL line.