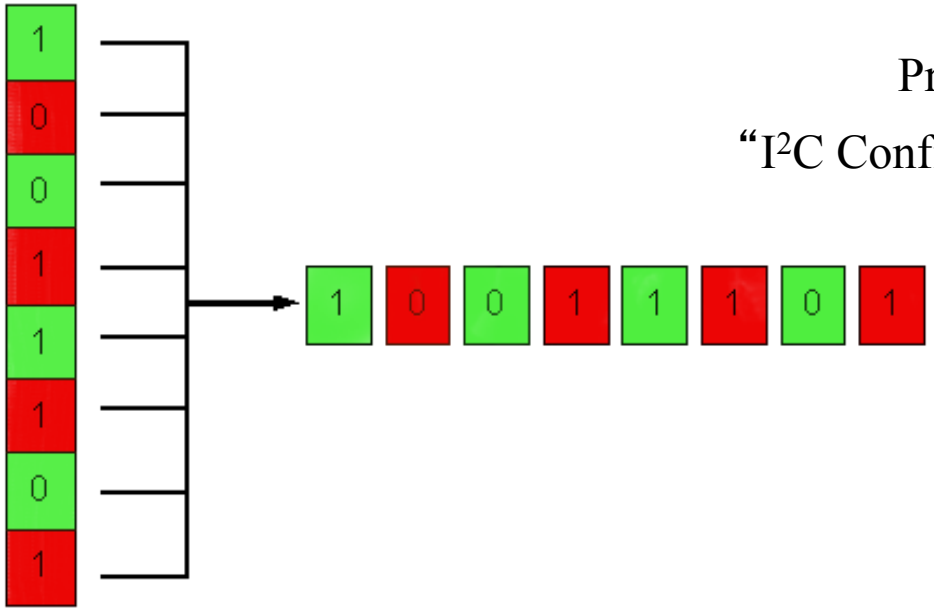
Handout #27a

CSEE4823x 10/27/16

Professor Steven Nowick

"I²C Configuration and Protocol"



I²C Configuration and Protocol

(With modifications by Melinda Agyekum and Steven Nowick)

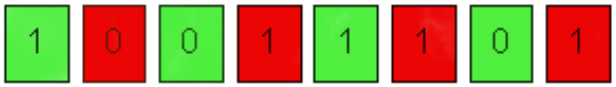
Presenter: Eugene Ho

Title: "Serial Interfaces, Part Deux- I²C and SPI"

Date: December 4, 2002

Website:

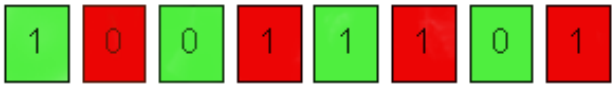
http://www.stanford.edu/class/ee281/presentations/aut2002/eugeneho-serialcomm.ppt



What is I²C?

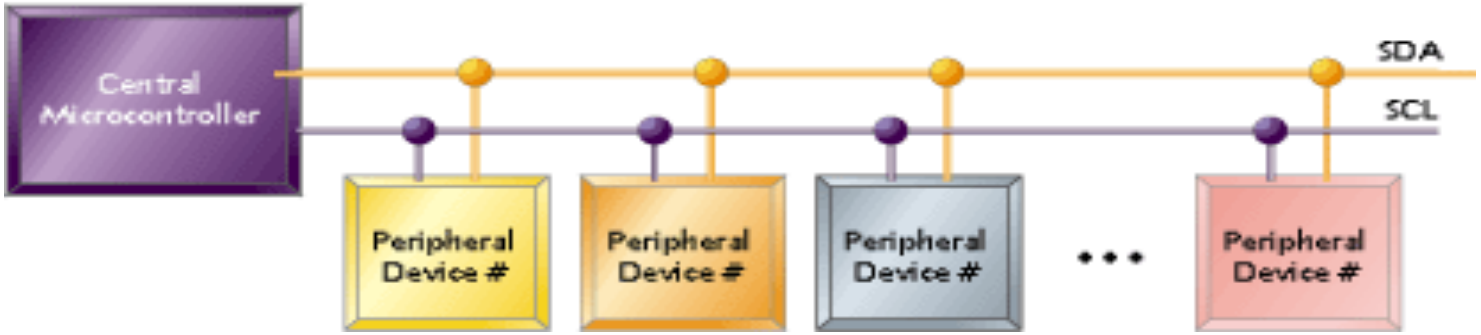
Serial Interfaces, part two

- Shorthand for an "Inter-integrated circuit" bus
- Developed by Philips Semiconductor for TV sets in the 1980's
- I²C devices include EEPROMs, thermal sensors, and real-time clocks
- Used as a control interface to signal processing devices that have separate data interfaces, e.g. RF tuners, video decoders and encoders, and audio processors.
- I²C bus has three speeds:
  - Slow (under 100 Kbps)
  - Fast (400 Kbps)
  - High-speed (3.4 Mbps) – I²C v.2.0
- Limited to about 10 feet for moderate speeds

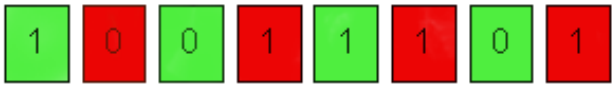


I^2C Bus Configuration

Serial Interfaces, part two



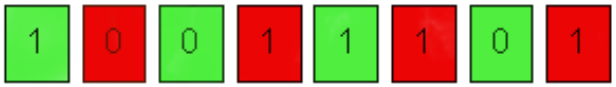
- 2-wire serial bus – Serial data (SDA) and Serial clock (SCL)
- Half-duplex, synchronous, multi-master bus
- No chip select or arbitration logic required
- Lines pulled high via resistors, pulled down via open-drain drivers (wired-AND)



I^2C Protocol

Serial Interfaces, part two

1. Master sends start condition (S) and controls the clock signal
2. Master sends a unique 7-bit slave device address
3. Master sends read/write bit (R/W) – 0 - slave receive, 1 - slave transmit
4. Slave with matching 7-bit device address always sends acknowledge bit (ACK)
5. Transmitter (slave or master) transmits 1 byte of data

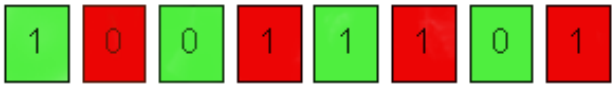


I^2C Protocol (cont.)

6. Receiver issues an ACK bit for the byte received
7. Repeat 5 and 6 if more bytes need to be transmitted
8. Master always sends stop condition (P)

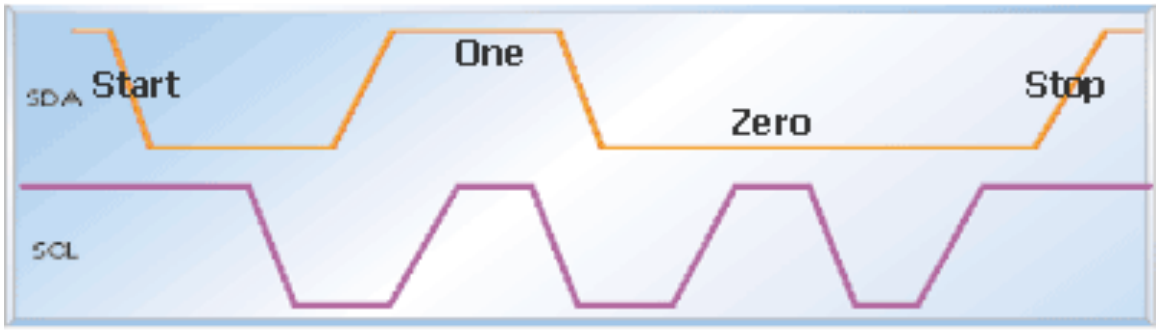
   a. For write transaction (master transmitting), master issues stop condition (P) after last byte of data.

   b. For read transaction (master receiving), master does not acknowledge final byte, just issues stop condition (P) to tell the slave the transmission is done



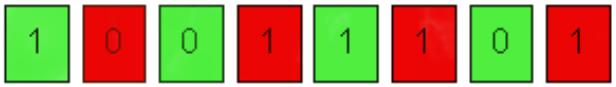
I^2C Signals

Serial Interfaces, part two



Sample Signals

- Start – high-to-low transition of the SDA line while SCL line is high
- Stop – low-to-high transition of the SDA line while SCL line is high
- Ack – While transmitter allows SDA to float, the receiver pulls SDA low throughout the entire next clock pulse on SCL.
- Data – transition takes place while SCL is low and is valid while SCL is high

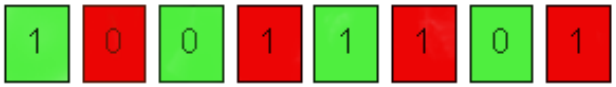


I²C Features

- "Clock stretching" – when the receiver needs more time to process a bit, it can pull SCL low to keep it from going high a bit longer. This technique is called clock stretching . On SDL low, the transmitter can send its next data value, but this value will not be interpreted as a valid data symbol by the receiver until after the slave is ready to release SCL to go high.

- "General call" broadcast – addresses every device on the bus

- 10-bit extended addressing for new designs. 7-bit addresses all exhausted



References

I^2C:

- http://www-us2.semiconductors.philips.com/acrobat/various/I2C_BUS_SPECIFICATION_1995.pdf
- http://www.esacademy.com/faq/i2c/index.htm
- http://www.embedded.com/story/OEG20020528S0057