

\*NOTE: "CSEE" refers to a course cross-listed between CS and EE Departments.

**Course:** CSEE W4823x, Advanced Logic Design  
**Time:** Tuesday and Thursday, 2:40–3:55 p.m.  
**Location:** 614 Schemerhorn  
**Credits:** 3 units

**Instructor:** Steven M. Nowick  
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**Email:** nowick@cs.columbia.edu  
**Office Hours:** Monday\* 4:30-5:30 p.m., Thursday 4:00-5:00 p.m.  
*\*Note:* CS Building doors close at 5pm, call after 5pm to be let in.  
**Phone:** (212) 939-7056

Extra individual appointments can be made if necessary; send me email or call.

**TA:** Yichun Deng  
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CSEE 4823 is an advanced course in modern digital design. The course is suitable for both graduate and upper-level undergraduate students. It serves as a technical elective for MS/PhD degrees in Computer Science and Electrical Engineering, and for the MS in Computer Engineering. It is also required for Computer Engineering undergraduates (in the digital systems track), and is a technical elective for Computer Science and Electrical Engineering undergraduates.

It provides a strong foundation for upper-level courses in digital and embedded systems, computer architecture, parallel systems, digital signal processing, digital signal processing, system-on-chip, VLSI and networking. It also provides a good background for a variety of industrial positions and for graduate research. The course also provides strong background in digital design and VHDL to prepare for courses such as CSEE 4840 Embedded System Design, CSEE 4868 System-on-Chip Platforms, and EECS 4321 Digital VLSI Circuits.

### **Course Description:**

*Overview.* The course covers advanced topics in digital design, with a special emphasis on how to model, simulate, synthesize and optimize large and complex subsystems — also known as register-transfer level (RTL) design. It also seamlessly covers some of the practical industrial aspects of modern design, including use of hardware description languages (e.g. VHDL) for structured modelling and simulation. Other topics include: controller synthesis and optimization, iterative circuits, high-speed combinational arithmetic circuits, fault-tolerance and soft error mitigation, power optimization strategies, asynchronous design, FPGA structures, and floating-point arithmetic. Students will also gain hands-on experience in designing and simulating a number of real digital systems using several CAD tools.

The course will include 2 projects:

- (i) complete design and simulation of an industrial controller, following commercial specifications (such as for NXP/Philips' I2C serial bus), modelling with VHDL and using Altera Quartus simulation package;
- (ii) complete RTL design of an entire custom digital system, from top-level specification to detailed implementation, exploring performance optimization techniques. Recent examples include: (a) a trigonometric hardware accelerator, (b) floating-point add/multiply unit, (c) on-chip network router with error handling.

Detailed topics include:

*Introduction to modern system-level design:* register-transfer level (RTL), algorithmic state machine models (ASMs), datapath/control allocation and interconnection. System-level performance optimization: resource sharing, scheduling, inner loop optimization, and area/delay tradeoffs.

*Introduction to VHDL* (an industry-standard hardware modelling language), practical VHDL modelling strategies.

*Large-scale digital system case studies:* designing a custom floating-point unit; counting and pattern detection units; the Philips I2C commercial serial bus interface; Huffman encoding/decoding.

*Synthesis of digital controllers* (Mealy and Moore state machines); controller optimization (state encoding, state minimization); iterative circuits.

*Advanced high-speed adder/multiplier design:* conditional sum, carry-skip, carry-select, carry-lookahead, carry-save. High-speed array multipliers. Design approaches using parallelism and speculation. Power, area and performance tradeoffs.

*Low-power optimization techniques:* precomputation architectures for pipelined systems; bus encoding strategies.

*Fault-tolerance and reliability:* error detection and correction (parity, Hamming and CRC codes; two-dimensional codes); recent strategies to make circuits resilient to "soft errors" (transient faults due to strikes by alpha particles and neutrons). Crosstalk reduction through bus encoding.

*Introduction to asynchronous (i.e. clockless) digital circuits:* designing clockless controllers and high-speed pipelines; hazard-free logic synthesis.

*Miscellaneous topics:* Commercial structured logic blocks – FPGA internals and micro-architectures. Metastability, synchronizers and synchronization failure. Introduction to floating-point arithmetic: number representation, floating-point unit design. Approximate computing for low power.

*Note:* While the course includes two challenging moderate-sized projects, and the use of CAD tools, it is not primarily a project/lab course. It also has a solid focus on written homeworks and technical concepts and ideas. Also, you do not need to be an experienced digital designer to take this course: you should simply have basic background in digital logic.

**Prerequisites:** Introductory basic course on digital logic and design (i.e. a *half-semester to one-semester introductory course*), such as CSEE 3827 Fundamentals of Computer Systems, or the equivalent.

*Desired pre-requisite background:* It is assumed that you are already familiar with: laws of Boolean algebra; truth tables; binary number representation (e.g. 2's complement); combinational logic design (Karnaugh maps, basic gates, negative logic, two-level [sum-of-products/AND-OR] and multi-level digital design); combinational building blocks (multiplexers, demultiplexers, decoders); basic adder design; latches, flipflops and registers. *Note: No VLSI or EE circuits background is required!*

A quick refresher on these topics will be included in the course. However, students with serious deficiencies should take an earlier course. If you have any questions about pre-requisites, contact the instructor (nowick@cs.columbia.edu).

**Required Text:**

Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with VHDL Design*, **3rd EDITION, including Altera's Quartus II CAD System (on CD-ROM)**, McGraw-Hill, New York, NY (2005).

*NOTE:* The 2nd edition has a number of differences from the 2nd edition, including in homework problems. We will ONLY be using the 3rd edition.

Copies of the book will be placed on reserve in the Engineering School Library. The book will only be used for part of the course material. A number of additional handouts will be provided by the instructor, as well as recent technical papers and articles.

**Other Background Texts (optional):**

*digital design:*

Daniel D. Gajski, *Principles of Digital Design*, Prentice Hall (1997).

Randy H. Katz, *Contemporary Logic Design*, Benjamin/Cummings Publishing Company, Inc., Redwood City, CA (1994).

Charles R. Kime and M. Morris Mano, *Logic and Computer Design Fundamentals*, 4th edition, Prentice-Hall, Upper Saddle River, NJ (2007).

Edward J. McCluskey, *Logic Design Principles: with emphasis on testable semicustom circuits*, Prentice-Hall, Englewood Cliffs, NJ (1986).

Charles H. Roth, Jr., *Fundamentals of Logic Design*, 5th edition, West Publishing Co., St. Paul, MI (1992).

John F. Wakerly, *Digital Design: Principles and Practices*, 4th edition, Prentice-Hall, Upper Saddle River, NJ (2006).

*VHDL background:*

J. Bhasker, *A VHDL Primer (3rd Edition)*, Prentice Hall (1999).

Stanley Mazor and Patricia Langstraat, *A Guide to VHDL*, 2nd edition, Kluwer Academic Publishers, Boston, MA (1993).

Stefan Sjöholm and Lennart Lindh, *VHDL for Designers*, Prentice-Hall, Englewood Cliffs, NJ (1997).

John F. Wakerly, *Digital Design: Principles and Practices*, 4th edition, Prentice-Hall, Upper Saddle River, NJ (2006).

*All books will be on reserve in the Engineering Library.*

**Homework.** There will be several homework assignments throughout the course. These assignments will include both written problems and small exercises with CAD software (see below).

**CAD Tools.** There will be two different computer-aided design (CAD) tools used in the course: (i) *Altera's Quartus II CAD System*, for VHDL modelling and simulation; and (ii) the *MINIMALIST Tool Package*, a public-domain tool for the synthesis and optimization of asynchronous controllers (developed by Prof. Nowick and his students at Columbia).

The Altera Quartus tool is included on CD-ROM with the required Brown/Vranesic text, and can also be downloaded from a web site; it can be installed on a variety of PC configurations. Details will be announced, and we expect to have alternative ways to access the tools for those who do not have appropriate PC's.

Likewise, arrangements will be made to access the MINIMALIST tool.

**Projects:** There will be two medium-sized projects, in addition to the above homework. Each will involve about three weeks of work. Details will be provided later in the course. The first project will involve the design of a substantial controller from industry specifications, which you will also model in VHDL, simulate and validate. The second project will involve the design and optimization of an entire RTL subsystem (such as a floating-point multiplier, a network router node, etc.).

**Exams.** Any material covered in assigned book readings, handouts, homework, lectures or discussion sections may appear in exam questions.

**Grading:** Course grades will be based on homework (about 15%), the first project (about 15%), the second project (about 20%), the midterm (about 15%), and the final exam (about 35%).

**Recitation and Review Sections:** Occasional recitation sections may be scheduled to introduce the CAD tools and the VHDL hardware description language, and there may be a review session before the final exam. The sessions will be led by the instructor and/or teaching assistant. Stay tuned for further announcements.

**Class Attendance:** You are responsible for the material regardless of your attendance in class. Regular class attendance is the best way to insure that you learn the material. *Lectures may often diverge from the book.*

**Late Policy:** If you hand in something after the due date without the explicit approval of the instructor or the TA, you might receive zero credit. Homeworks are due at the beginning of class on the assigned due date. Under real emergencies, extensions might be given by the instructor, if you contact me in advance.

**Cooperation on Homework and Exams:** Collaboration on deriving homework solutions, or sharing or copying of solutions, is *not* allowed. Of course, no cooperation is allowed on exams. *The department academic honesty policy is listed in:* <http://www.cs.columbia.edu/academics/honesty>. It is your responsibility to be aware of this policy, and to conform to it.

**Handouts:** Additional copies of handouts will be available on the class web page. Hardcopy handouts are available from the TA.

**Class Web Page:** The URL of the class web page is: <http://www.cs.columbia.edu/~cs4823>. This page will contain copies of handouts, homework assignments and solutions, and other important information. You should read it regularly. (It is also linked to the Courseworks web site for the class.)