

Cheng-Hong Li

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EDUCATION	Columbia University <i>PhD candidate in Computer Science</i> , GPA 4.0/4.0 PhD Thesis: Methods for Performance Optimization and Validation of Latency-Insensitive Systems Adviser: Prof. Luca Carloni	Expected Spring 2009 New York, NY
	National Taiwan University <i>M.S. in Computer Science</i> , GPA 4.0/4.0 MS Thesis: Analysis of Some Verification Problems for Controlled Petri Nets Adviser: Prof. Hsu-Chun Yen	Sept. 1998 – June 2001 Taipei, Taiwan
	<i>B.S. in Electrical Engineering</i> . GPA 3.85/4.0 (overall); 3.96/4.0 (major).	Sept. 1994 – June 1998
INTERESTS	CAD/EDA tools for system level design, formal verification, and computer architecture.	
WORK EXPERIENCE	IBM, Austin Research Lab. <i>Summer Intern</i> · Programmed and analyzed multicore architectures (Cell and GPU) and development tools.	May 2007 – Aug. 2007 Austin, TX
	VIA Technologies <i>Software Engineer</i> · Developed a video driver on Windows CE for an embedded system in team of 3 engineers.	Feb. 2002 – June 2002 Taipei, Taiwan
	Trend Micro Inc. <i>Software Engineer</i> · Worked in team of 6 people to develop self-update module for product deployment and management.	Feb. 2001 – July 2001 Taipei, Taiwan
	Siemens <i>Full-time Intern</i> · Developed an UML-based performance simulator for distributed software systems in Java.	June 2000 – Nov. 2000 Munich, Germany
RESEARCH EXPERIENCE	Optimization of Latency-Insensitive Systems · Implemented logic optimization and latch-based clustering algorithms (30000 lines of C++ code). · Developed synthesizable and efficient latency-insensitive wrappers and relay stations in Verilog and VHDL. · Formally verified the RTL design using NuSMV.	2005 – present Columbia University
	Code Compression for Embedded Systems · Achieved the best program compressions on ARM processors without any modification to compiler tools and processors. · Developed and managed code compression tool for ARM and Thumb (20000 lines of C++ code). · Invented <i>curve-fitting Huffman code</i> , and various efficient state- and context-based higher-order models.	Sept. 2002 – 2006 Columbia University
PUBLICATIONS	[1] C.-H. Li and L. P. Carloni, “Leveraging local intra-core information to increase global performance in block-based design of systems-on-chip,” <i>IEEE T-CAD</i> (to appear). [2] C.-H. Li and L. P. Carloni, “Using functional independence conditions to optimize the performance of latency-insensitive systems,” in <i>ICCAD’07</i> , pp. 32–39. [3] C.-H. Li, R. L. Collins, S. Sonalkar, and L. P. Carloni, “Design, implementation, and validation of a new class of interface circuits for latency-insensitive design,” in <i>MEMOCODE’07</i> , pp. 13–22. [4] C.-H. Li and S. M. Nowick, “An architecture-oriented approach to code compression for embedded processors,” in <i>WASP’05</i> , pp. 83–90. [5] Y.-K. Lin, C.-H. Li, and H.-C. Yen, “Synthesis of control policies for lossy controlled Petri nets,” in <i>IEICE Transactions: Systems and Control</i> , 86(7):1790–1798, July 2003.	
COURSE PROJECTS	Computer Hardware Design (Prof. Ken Shepard) · Built fully-functional PDP-8 with UART I/O on FPGA.	Spring, 2003 Columbia University
	VLSI Design (Prof. Ken Shepard) · Designed ALU and mini instruction decoder (full-custom).	Fall, 2002, Columbia University
TEACHING EXPERIENCE	Computer Architecture <i>Teaching Assistant</i> · Designed course project using SimpleScalar and SimWattch to conduct design space exploration.	Fall, 2003/04/05 Columbia University
SKILLS	Programming Languages: C++, C, Java, shell scripts, AWK, Perl HDLs: VHDL and Verilog Tools: Synopsys DesignCompiler, Cadence, SIS, SimpleScalar	
HONORS AND AWARDS	Class A scholarship , 2 times, National Taiwan University, top 5% of class Presidential Award , 3 times, National Taiwan University, top 5% of class	