An Overview of the Electronic Design Automation (EDA) Field

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Electronic Design Automation

EDA: Software engineers use to design integrated circuits

Most tools focus on large digital ICs:

- Microprocessors (Intel, Sun, Motorola)
- Graphics chips (nVidia, S3)
- Digital signal processors (TI, Motorola)

Design complexity the biggest challenge (millions of transistors).

Typical Design Flow

Overall flow: Translate high levels of abstraction to low levels

1. Register-transfer level Verilog or VHDL
2. Gate-level netlist
3. Transistor-level netlist
4. Polygons describing “masks” for transistors and wires

Register-transfer level Verilog

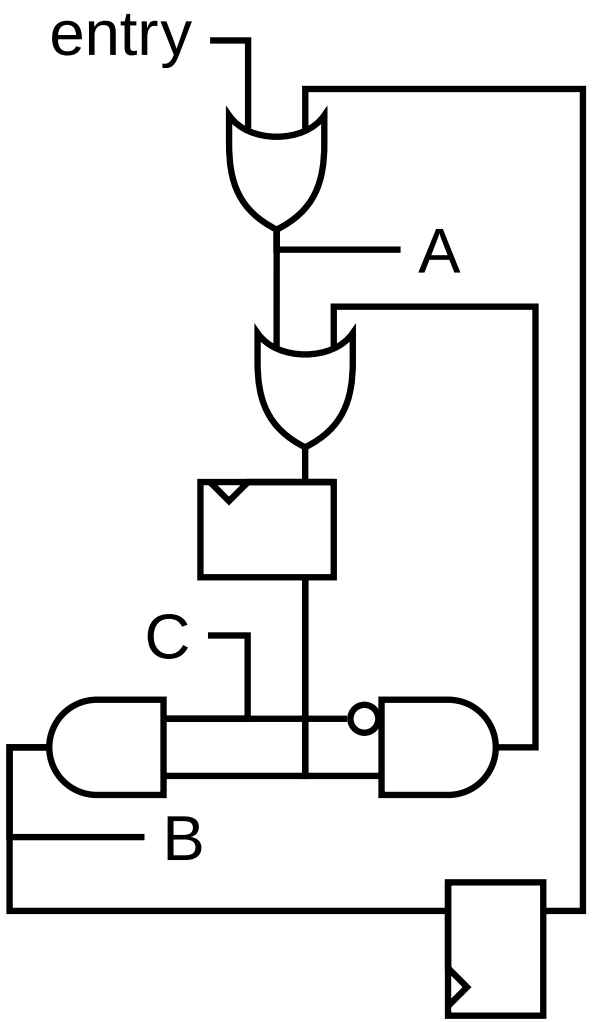
Like a C or Java program:

```
module gcd(r, ready, clk, reset, a, b);
  output r[7:0], ready; reg r[7:0];
  input clk, reset, a[7:0], b[7:0];

  always @(posedge clk) begin
    ready = 0;
    if (a == b) begin
      r = a; ready = 1;
    end else if (a <= b) b = b - a;
    else a = a - b;
  end
end module
```

Gate-level netlists

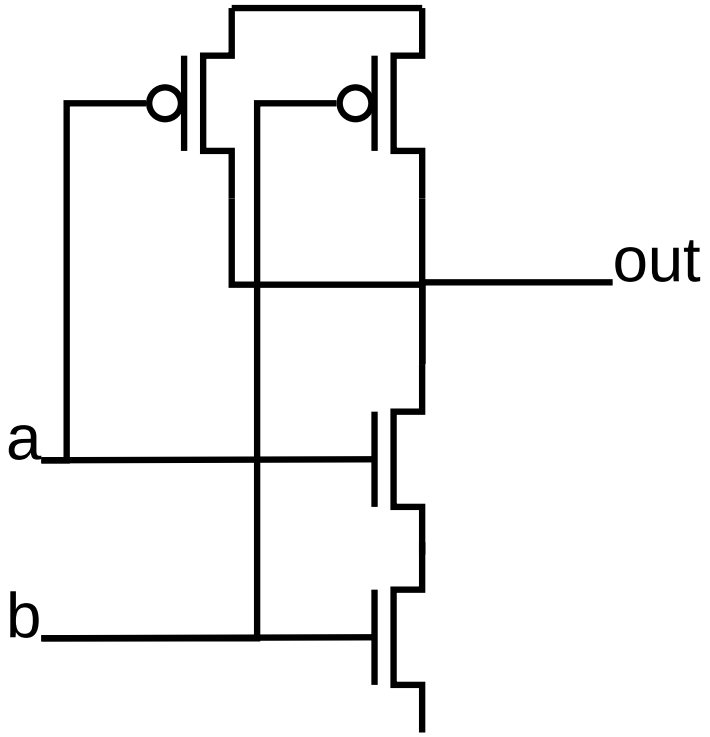
Collection of logic gates and flip-flops connected by wires.



Transistor-level netlists

Collection of MOS transistors (two types) connected by wires.

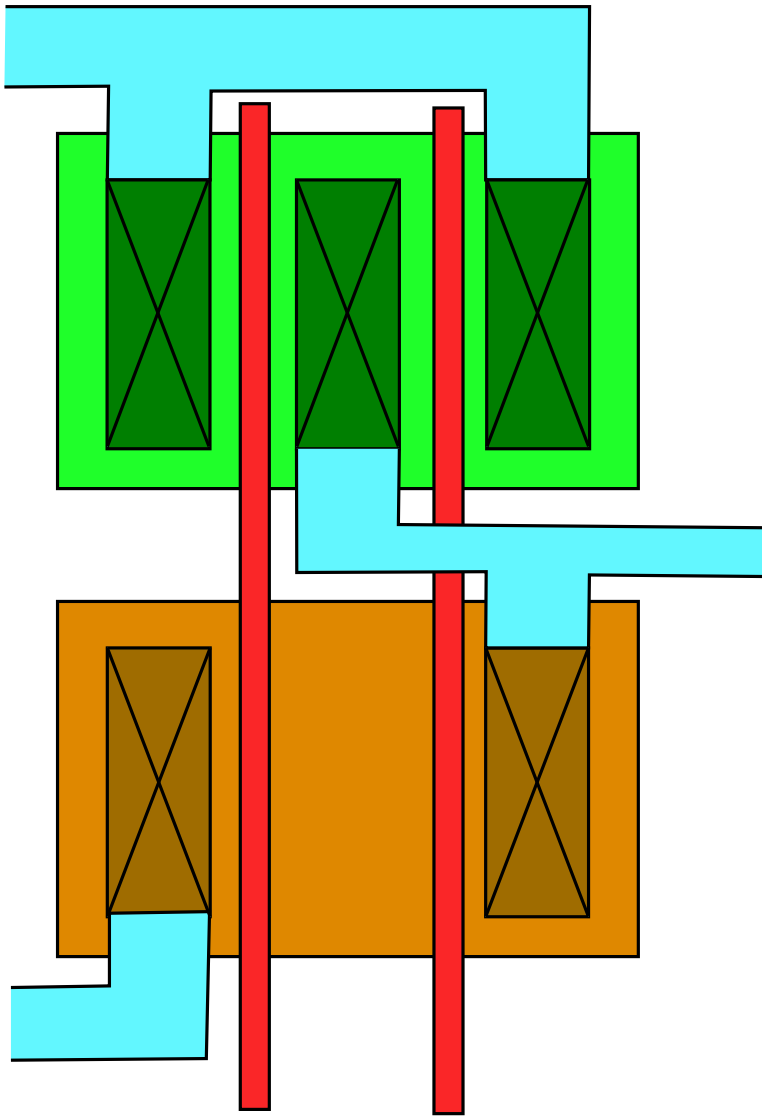
Transistor netlist for a single NAND gate:



Polygon Layout

Collection of polygons (lists of 2D points) on different masks (metal, gate, etc.).

Layout for a single NAND gate:



Types of EDA/IC companies

Chip designers

- Intel, Motorola, TI, nVidia, S3, IBM

Chip fabricators

- TSMC, LSI Logic, NEC

Fab equipment suppliers

- Applied materials

EDA tool vendors

- Cadence, Synopsys, Magma, (Avanti)

EDA Tools

Logic synthesis

- Translates high-level languages into netlists
- Synopsys main supplier

Place-and-route tools

- Takes netlists and decides where to put each wire and transistor
- Cadence main supplier

EDA Tools

Simulation tools

- Takes a description of a circuit (netlist) and simulates its behavior
- Critical to get a chip right the first time
- Synopsys and Cadence both

Verification tools

- Design rule/electrical rule checkers. Are the netlist and polygons right?
- Equivalence checkers: do the polygons match the netlist? Does the netlist match the original?

Large EDA Conferences

Design Automation Conference (DAC)

- Yearly, in early June, different US locations
- Large technical program plus enormous tradeshow

International Conference on Computer-Aided Design (ICCAD)

- Yearly, early November, San Jose, California
- Large technical program

Design Automation and Test in Europe (DATE)

- Yearly, March, alternates between Munchen and Paris
- Smaller, European version of DAC

Other Academic Resources

Journals:

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TransCAD)

ACM Transactions on Design Automation for Electronic Systems (TODAES)

Workshops:

Many small workshops and conferences (logic synthesis, low-power design, FPGAs, low-power, verification, etc.)

Professional Organization:

IEEE SIGDA (Special Interest Group on Design Automation). Sponsors DAC, ICCAD, etc.