# Qsys (Platform Designer) and IP Core Integration

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IP Cores

Altera's IP Core Integration Tools

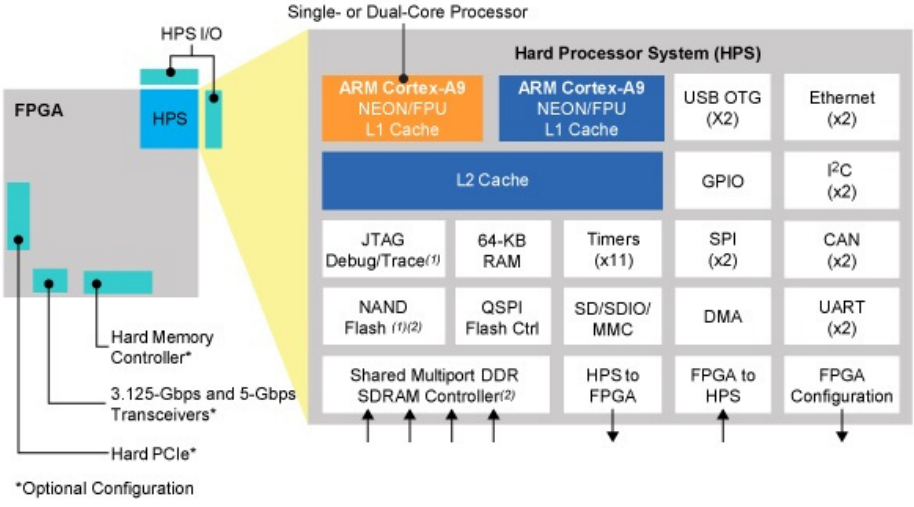
Connecting IP Cores

# IP Cores

# Cyclone V SoC: A Mix of Hard and Soft IP Cores

IP = Intellectual Property
Hard = wires & transistors

Core = block, design, circuit, etc.
Soft = implemented w/ FPGA




Source: Altera

# Example IP Cores

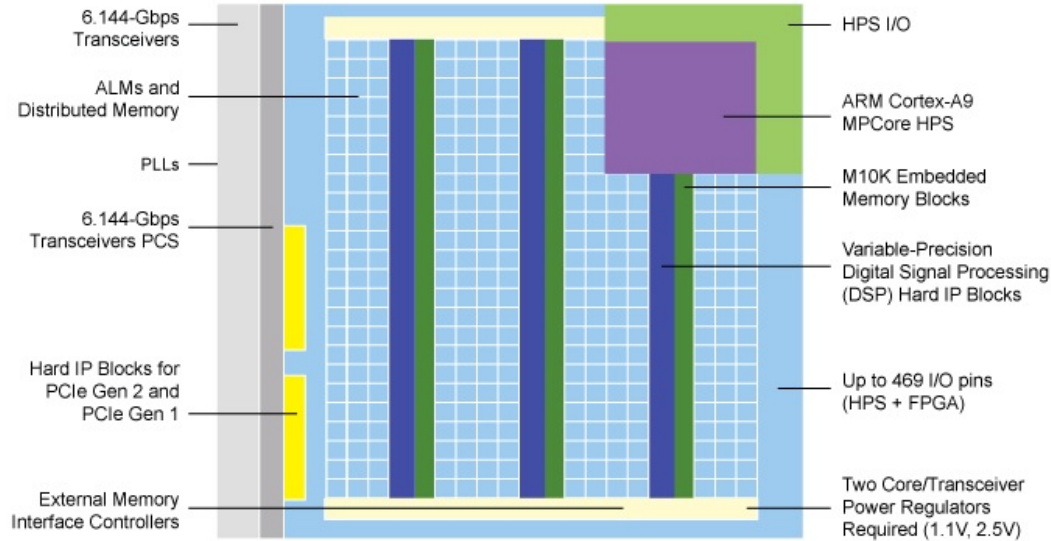
**CPUs**: ARM (hard), NIOS-II (soft)

**Highspeed I/O**: Hard IP Blocks for High Speed Transceivers (PCI Express, 10Gb Ethernet)

**Memory Controllers**: DDR3

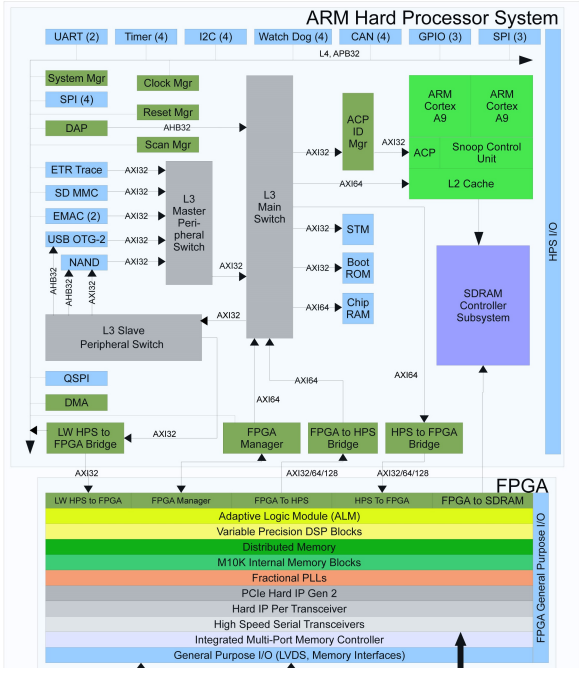
**Clock and Reset signal generation**: PLLs

# Cyclone V SoC: FPGA layout



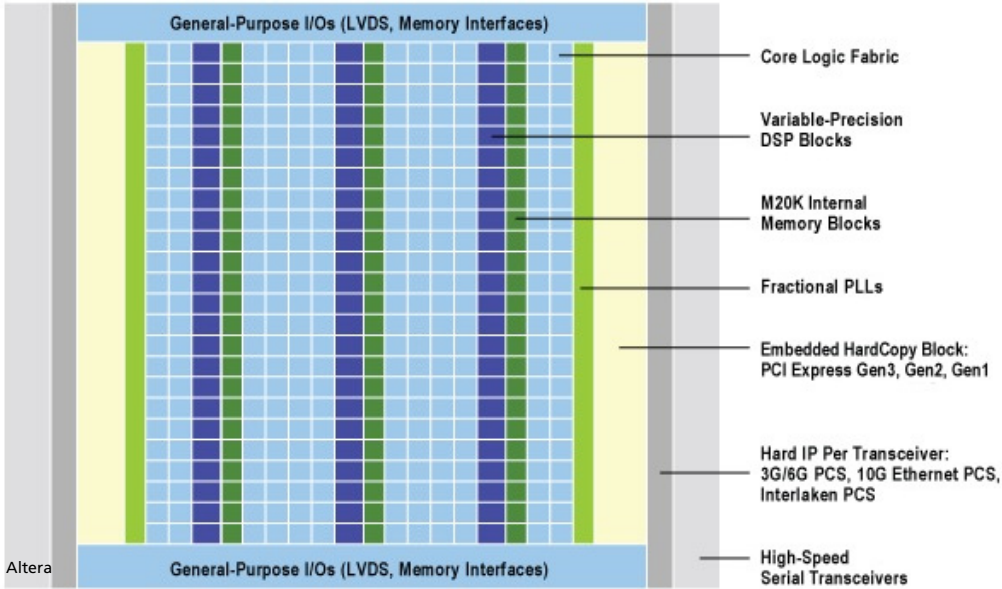

Source: Altera

# Cyclone V SoC: HPS Layout




Source: NARD, LLC.

# Stratix V: FPGA Layout




Source: Altera

# Bus Bridges

A bus bridge connects two, often different, buses.

Enables multiple clock domains, different protocols (e.g., AXI $\leftrightarrow$ Avalon), bus widths, etc.

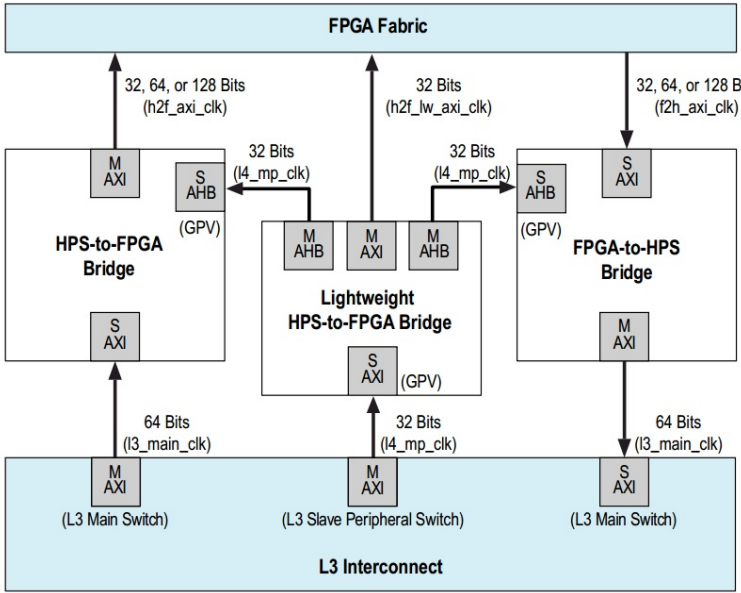
**Example Bridge Types**:

SOC HPS $\leftrightarrow$ FPGA Bridge

Avalon MM Clock Crossing Bridge

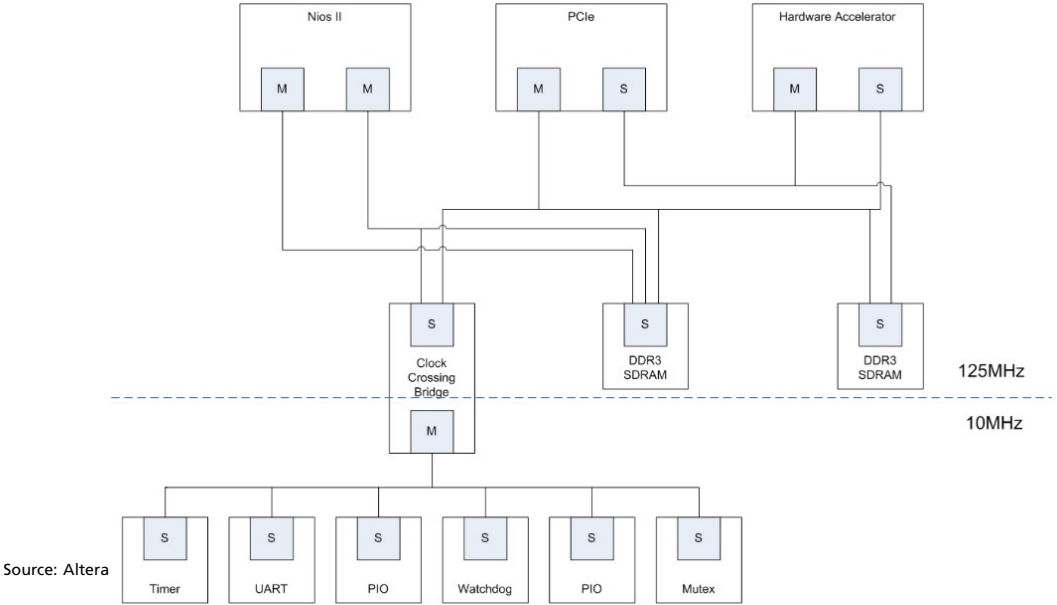
Avalon MM Pipeline Bridge

# Cyclone V SoC: FPGA ↔ HPS Bridge




Source: Altera

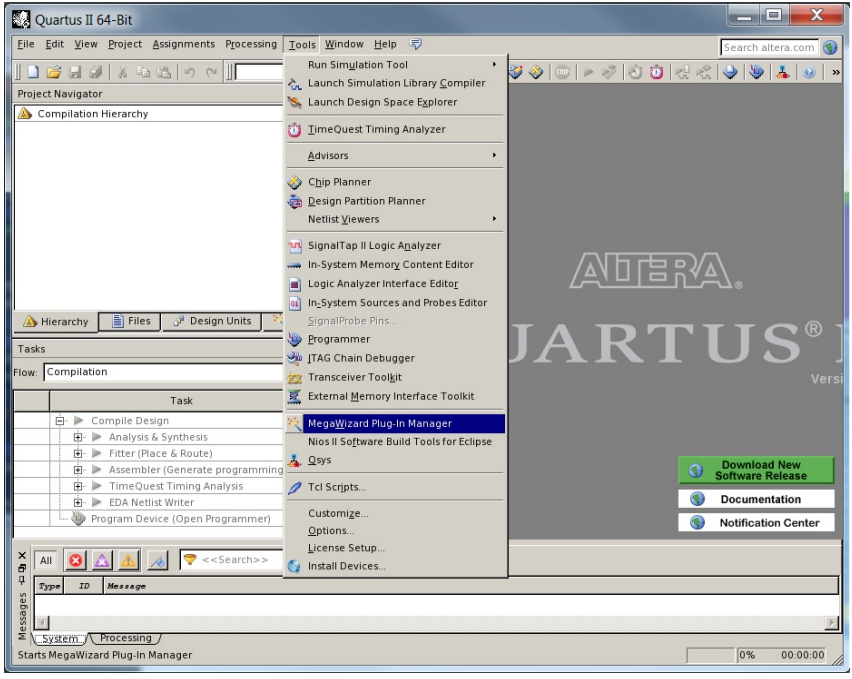
# Clock Crossing Bridge Example




Source: Altera

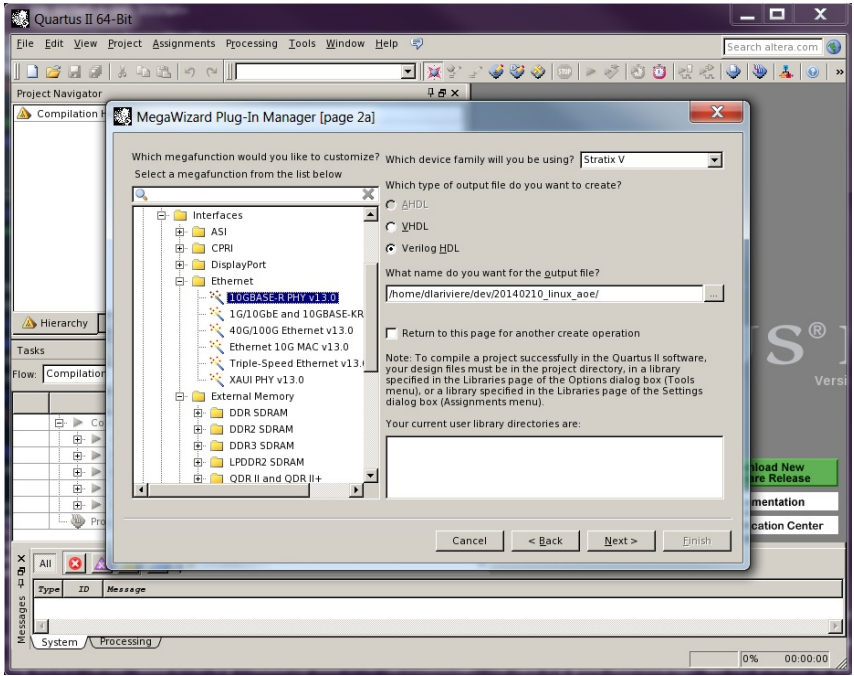
# Altera’s IP Core Integration Tools

# The Quartus Megawizard




Source: Altera

# Megawizard Example: 10Gb Ethernet PHY




Source: Altera

# Megawizard IP Cores

*Core-specific interfaces on each*

**Arithmetic**: $+$, $-$, $\times$, $\div$, Multiply-Accumulate, ECC

**Floating Point**: $+$, $-$, $\times$, $\div$

**Gate Functions**: Shift Registers, Decoders, Multiplexers

**I/O Functions**: PLL, temp sensor, remote update, high speed transceivers

**Memory**: Single/Dual-port RAMs, Single/Dual-clock FIFOs, Shift registers

**DSP**: FFT, ECC, FIR, etc.

**Video**: large suite

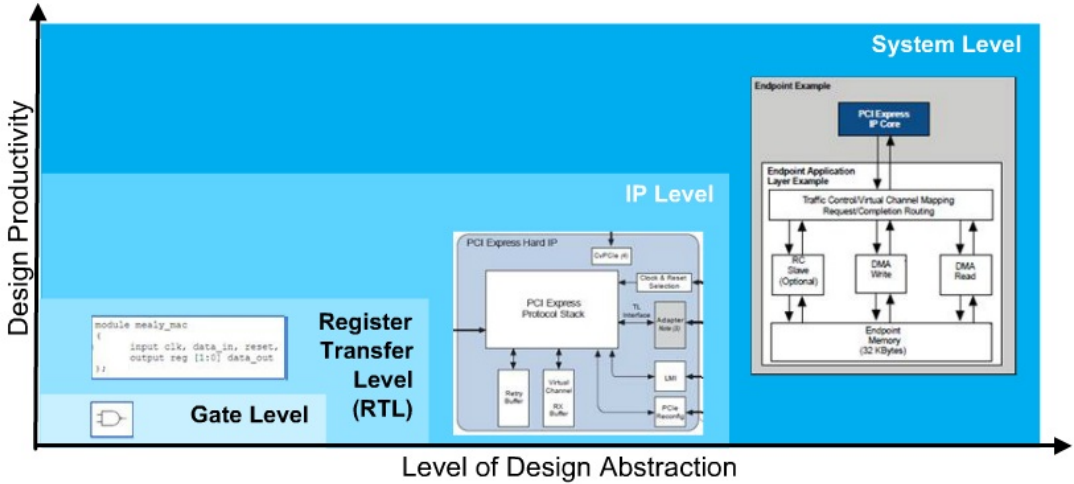
*Some megafunctions are only available on certain FPGAs*

# Qsys/Platform Designer

Platform Designer (formerly Qsys) is Altera's system integration tool for building Network-on-Chip (NoC) designs connecting multiple IP cores.

| You | Qsys |
|---|---|
| List the IP components and how you want them connected | Generates the interconnect (arbiters, etc.), adds adapters as necessary, warns of errors |

# Qsys: Raising Level of Abstraction

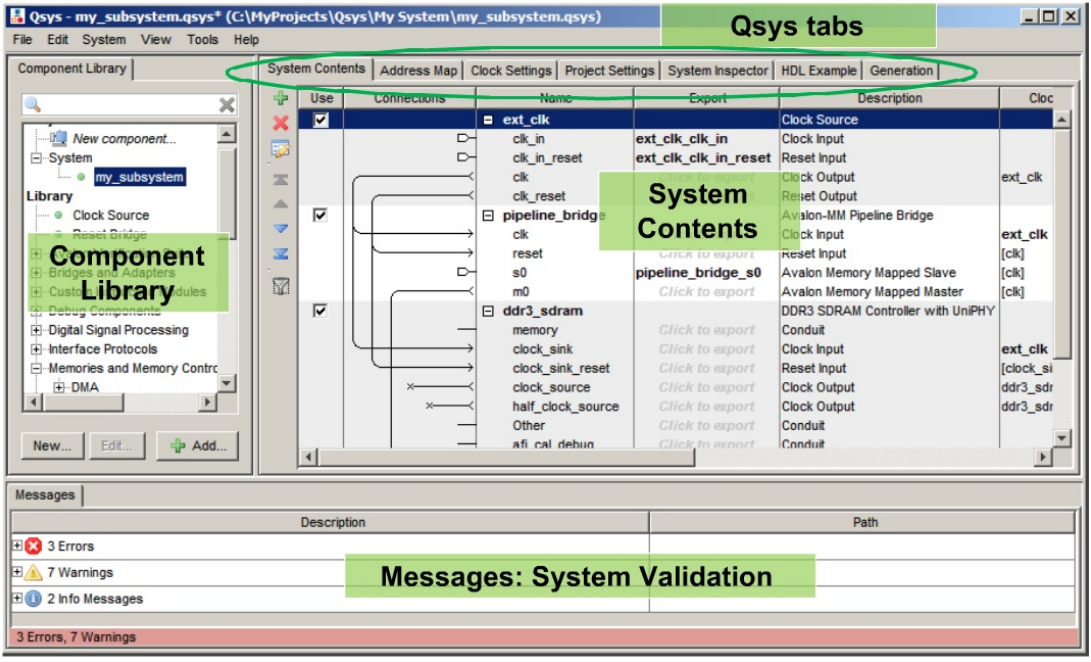



Source: Altera

ALTERA

Schematic Entry | Quartus II Synthesis | SOPC Builder

Qsys


Qsys - my_subsystem.qsys* (C:\MyProjects\Qsys\My System\my_subsystem.qsys)
File Edit System View Tools Help
Qsys tabs
Component Library
System Contents
Address Map
Clock Settings
Project Settings
System Inspector
HDL Example
Generation
Use
Connections
Name
Export
Description
Cloc
ext_clk
Clock Source
clk_in
ext_clk_clk_in
Clock Input
clk_in_reset
ext_clk_clk_in_reset
Reset Input
clk
Clock Output
ext_clk
clk_reset
Reset Output
pipeline_bridg
Avalon-MM Pipeline Bridge
clk
Clock Input
ext_clk
reset
Reset Input
[clk]
s0
pipeline_bridge_s0
Avalon Memory Mapped Slave
[clk]
m0
Click to export
Avalon Memory Mapped Master
[clk]
ddr3_sdram
DDR3 SDRAM Controller with UniPHY
memory
Click to export
Conduit
clock_sink
Click to export
Clock Input
ext_clk
clock_sink_reset
Click to export
Reset Input
[clock_si
clock_source
Click to export
Clock Output
ddr3_sdr
half_clock_source
Click to export
Clock Output
ddr3_sdr
Other
Click to export
Conduit
afi_cal_debug
Click to export
Conduit
New component...
System
my_subsystem
Library
Clock Source
Reset Bridge
Component Library
Bridges and Adapters
Custo
dules
Debug Components
Digital Signal Processing
Interface Protocols
Memories and Memory Contro
DMA
New...
Edit...
Add...
Messages
Description
Path
3 Errors
7 Warnings
2 Info Messages
Messages: System Validation
3 Errors, 7 Warnings

# System Level Design: Why Use Qsys

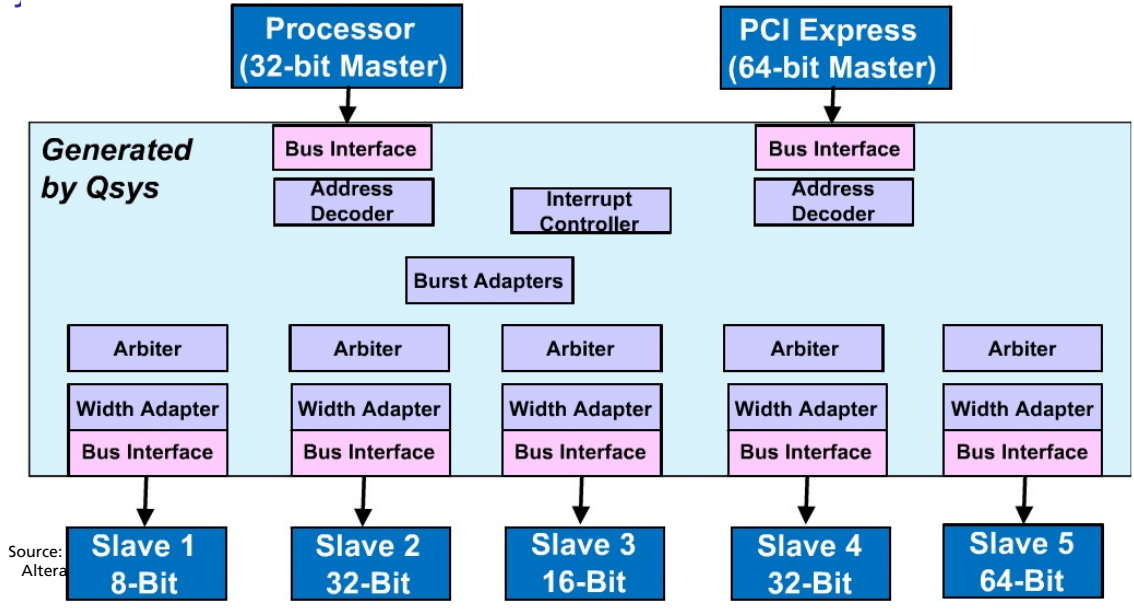
Avoids manually developing custom interconnect fabrics and signaling.

Instead of cycle-to-cycle coordination between every individual IP core, focus on transaction-level designs.

Design IP without knowing exactly when data will transfer and instead only focus on how (once it does).

(Only valid if you design your individual components to one of the standardized interfaces)

# Qsys-based Method of Design




Source: Altera

# Connecting IP Cores

# Interface Types

**Memory-mapped** Interfaces:

Avalon MM (Altera)

AXI (ARM, supported by Qsys now for SoC)

**Streaming** Interfaces: Avalon ST:

Avalon ST source port: outputs streaming data

Avalon ST sink port: receives incoming streaming data

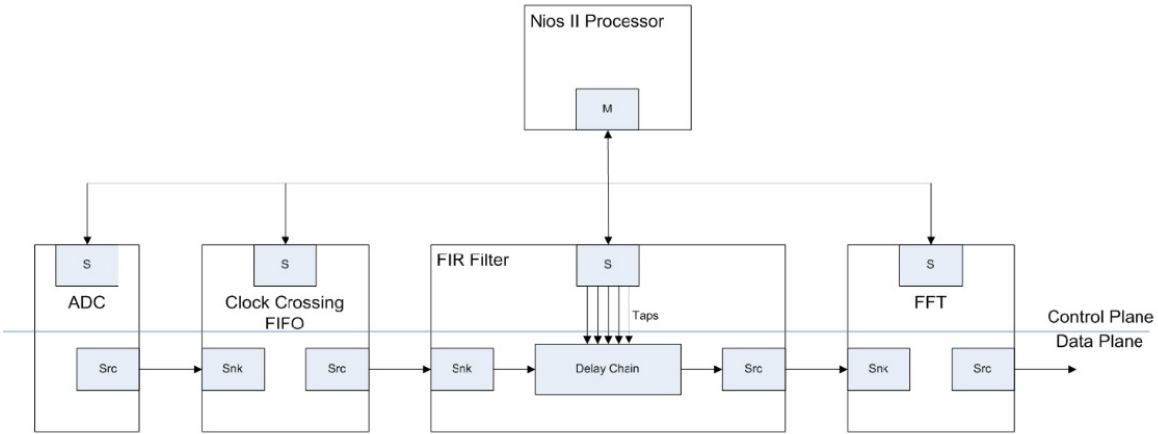
# Control vs. Data Planes

**Control Plane**: Memory mapped registers typically used for configuring devices, querying status, initiating transactions, etc (low bandwidth)

**Data Plane**: Streaming directed graphs for actually moving and processing large amounts of data (audio/video, network packets, etc); high bandwidth

A single IP core can have both MM and ST interfaces (including multiple of each).

# Control and Data Planes Example




Source: Altera

# Additional References

Altera online training lectures: (HIGHLY recommended; many of these slides are taken directly from them)

`http://www.altera.com/education/training/curriculum/trn-curriculum.html`

Introduction to Qsys

Advanced System Design Using Qsys

Custom IP Development Using Avalon and AXI Interfaces

(Everything has moved to Intel; above link still works)