

Qsys (Platform Designer) and IP Core Integration

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IP Cores

Altera's IP Core Integration Tools

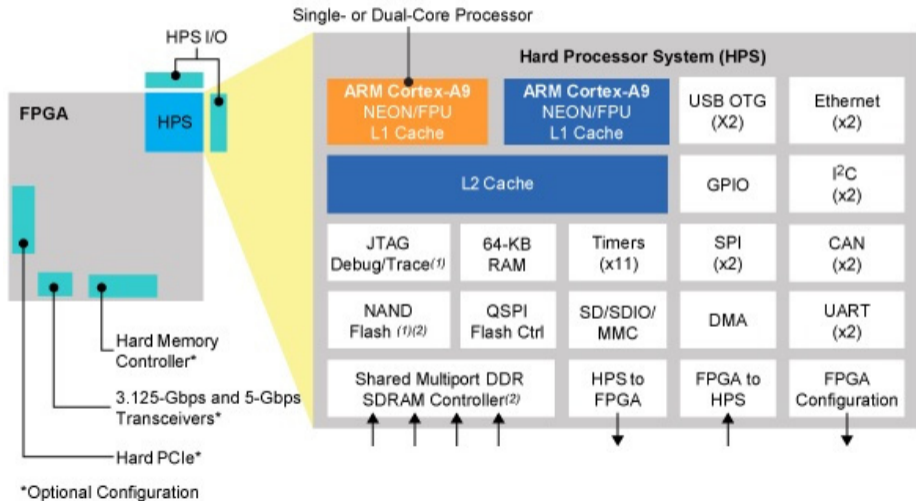
Connecting IP Cores

IP Cores

Cyclone V SoC: A Mix of Hard and Soft IP Cores

IP = Intellectual Property
Hard = wires & transistors

Core = block, design, circuit, etc.
Soft = implemented w/ FPGA



Example IP Cores

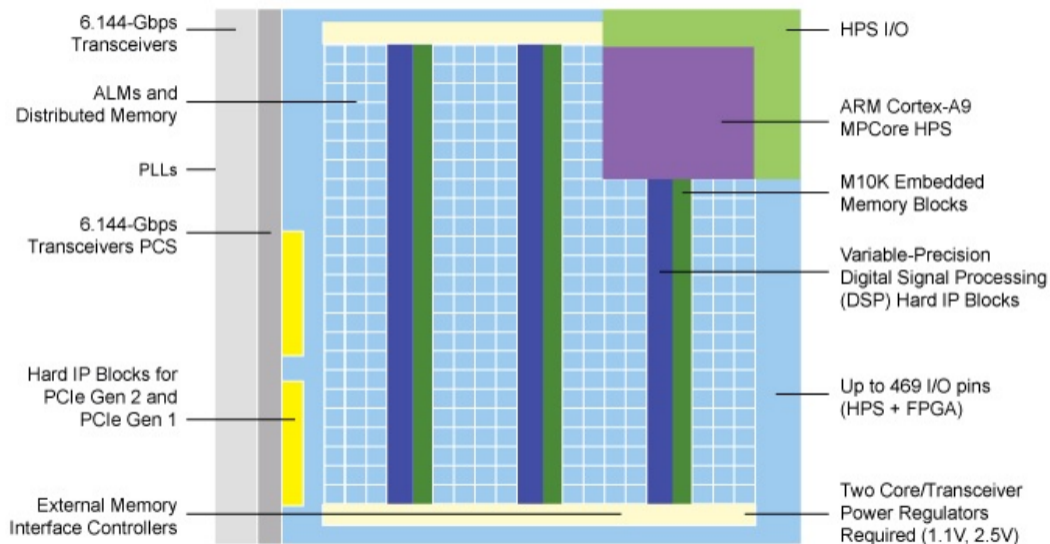
CPUs: ARM (hard), NIOS-II (soft)

Highspeed I/O: Hard IP Blocks for High Speed Transceivers (PCI Express, 10Gb Ethernet)

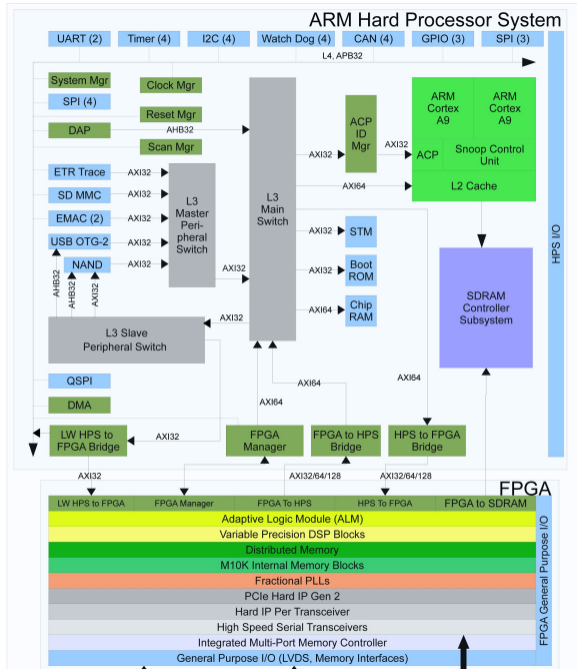
Memory Controllers: DDR3

Clock and Reset signal generation: PLLs

Cyclone V SoC: FPGA layout

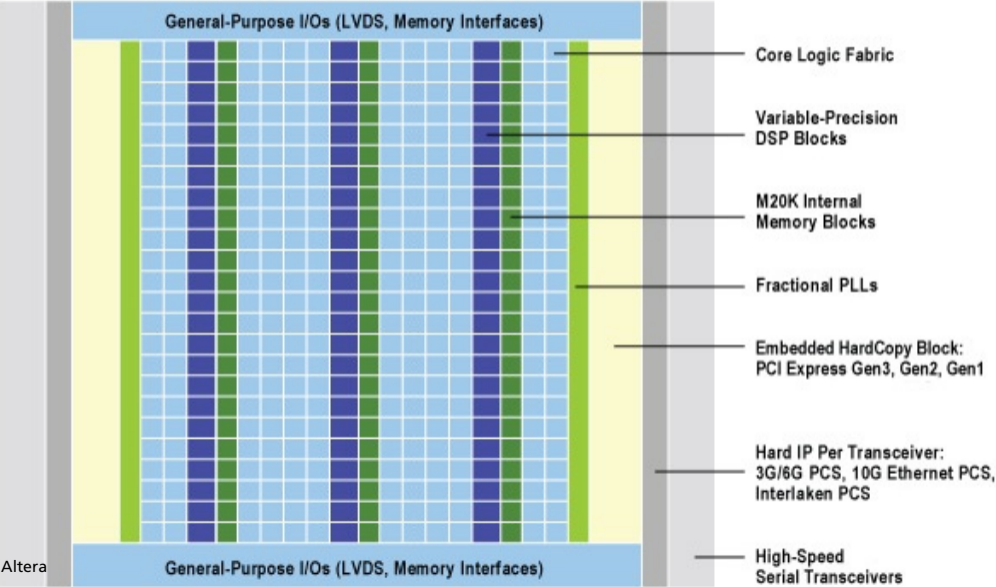


Cyclone V SoC: HPS Layout



Source: NARD, LLC.

Stratix V: FPGA Layout



Source: Altera

Bus Bridges

A bus bridge connects two, often different, buses.

Enables multiple clock domains, different protocols (e.g., AXI ↔ Avalon), bus widths, etc.

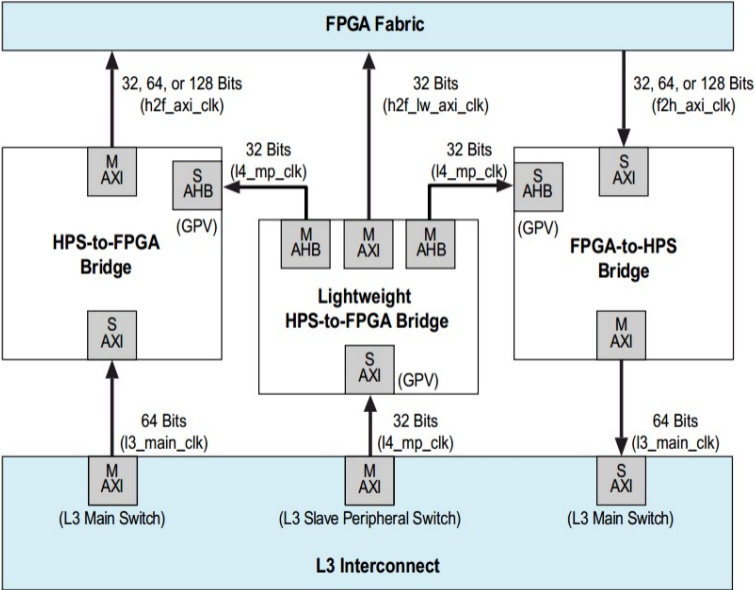
Example Bridge Types:

SOC HPS ↔ FPGA Bridge

Avalon MM Clock Crossing Bridge

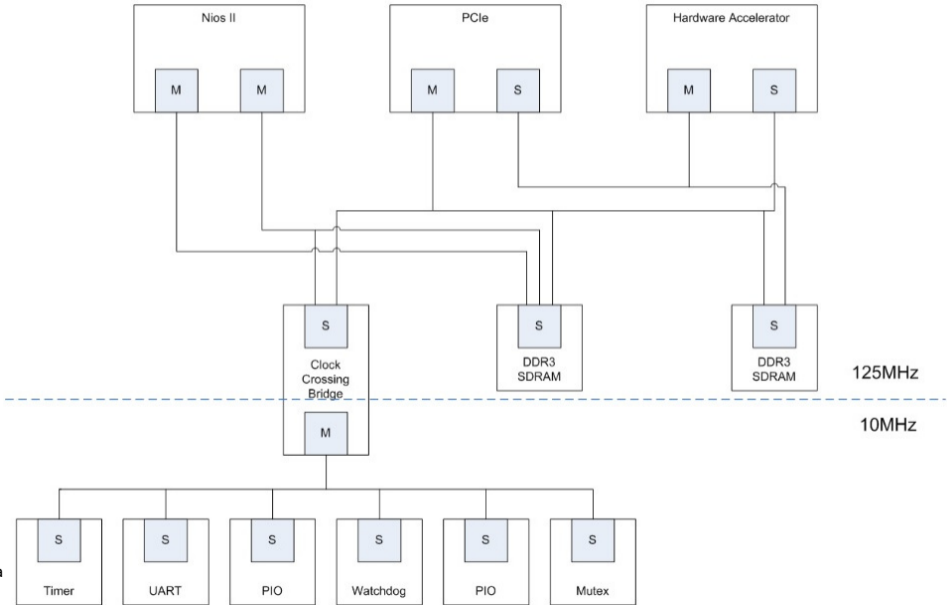
Avalon MM Pipeline Bridge

Cyclone V SoC: FPGA ↔ HPS Bridge



Source: Altera

Clock Crossing Bridge Example



Source: Altera

Altera's IP Core Integration Tools

The Quartus Megawizard

The screenshot displays the Quartus II 64-bit software interface. The main window shows the 'MegaWizard Plug-In Manager' menu, which is open and lists various tools and options. The 'MegaWizard Plug-In Manager' option is highlighted in blue. The background of the main window features the 'ALTERA' and 'QUARTUS' logos.

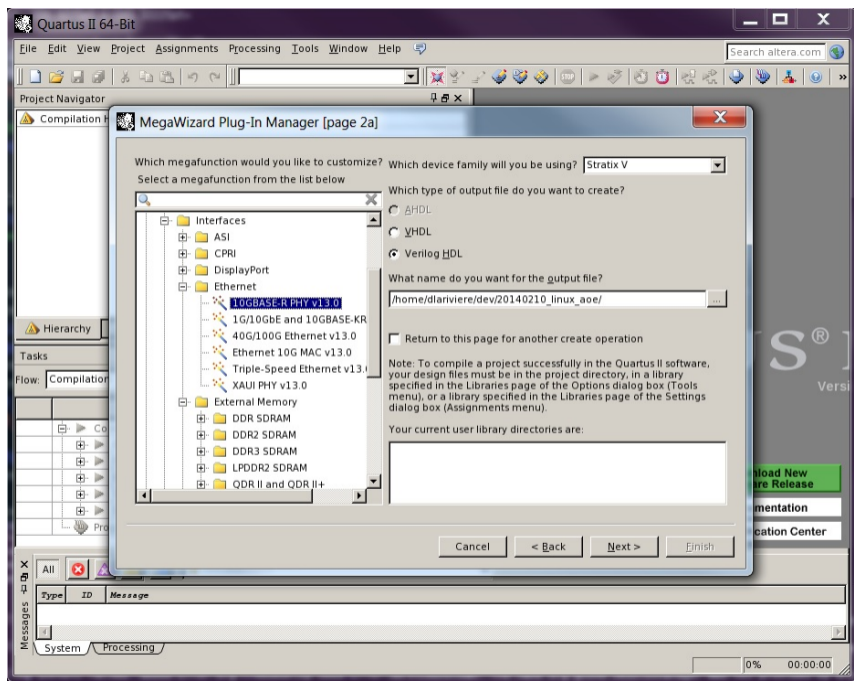
The interface includes a menu bar with 'File', 'Edit', 'View', 'Project', 'Assignments', 'Processing', 'Tools', 'Window', and 'Help'. Below the menu bar is a toolbar with various icons. The 'Project Navigator' pane on the left shows a 'Compilation Hierarchy' tree. The 'Tasks' pane below it shows a 'Flow: Compilation' task list with sub-tasks like 'Compile Design', 'Analysis & Synthesis', 'Filter (Place & Route)', 'Assembler (Generate programming)', 'TimeQuest Timing Analysis', 'EDA Netlist Writer', and 'Program Device (Open Programmer)'. The 'Messages' pane at the bottom shows a message: 'Starts MegaWizard Plug-In Manager'.

The 'MegaWizard Plug-In Manager' menu items are:

- Run Simulation Tool
- Launch Simulation Library Compiler
- Launch Design Space Explorer
- TimeQuest Timing Analyzer
- Advisors
- Chip Planner
- Design Partition Planner
- Netlist Viewers
- SignalTap II Logic Analyzer
- In-System Memory Content Editor
- Logic Analyzer Interface Editor
- In-System Sources and Probes Editor
- SignalProbe Pins...
- Programmer
- JTAG Chain Debugger
- Transceiver Toolkit
- External Memory Interface Toolkit
- MegaWizard Plug-In Manager**
- Nios II Software Build Tools for Eclipse
- Qsys
- Tcl Scripts...
- Customize...
- Options...
- License Setup...
- Install Devices...

The 'Messages' pane at the bottom shows a message: 'Starts MegaWizard Plug-In Manager'.

Megawizard Example: 10Gb Ethernet PHY



Megawizard IP Cores

Core-specific interfaces on each

Arithmetic: +, -, ×, ÷, Multiply-Accumulate, ECC

Floating Point: +, -, ×, ÷

Gate Functions: Shift Registers, Decoders, Multiplexers

I/O Functions: PLL, temp sensor, remote update, high speed transceivers

Memory: Single/Dual-port RAMs, Single/Dual-clock FIFOs, Shift registers

DSP: FFT, ECC, FIR, etc.

Video: large suite

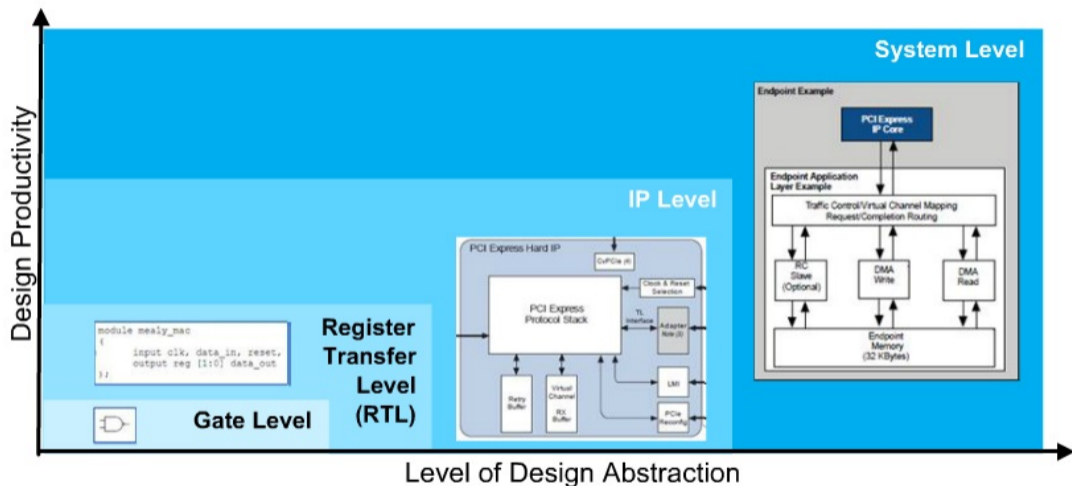
Some megafunctions are only available on certain FPGAs

Qsys/Platform Designer

Platform Designer (formerly Qsys) is Altera's system integration tool for building Network-on-Chip (NoC) designs connecting multiple IP cores.

You	Qsys
List the IP components and how you want them connected	Generates the interconnect (arbiters, etc.), adds adapters as necessary, warns of errors

Qsys: Raising Level of Abstraction



ALTERA

Source: Altera

Schematic
Entry

Quartus II
Synthesis

SOPC
Builder



Component Library | System Contents | Address Map | Clock Settings | Project Settings | System Inspector | HDL Example | Generation

Component Library

System Contents

Use	Connections	Name	Export	Description	Clock
<input checked="" type="checkbox"/>		ext_clk		Clock Source	
		clk_in	ext_clk_clk_in	Clock Input	
		clk_in_reset	ext_clk_clk_in_reset	Reset Input	
		clk		Clock Output	ext_clk
		clk_reset		Reset Output	
<input checked="" type="checkbox"/>		pipeline_bridge		Avalon-MM Pipeline Bridge	
		clk		Clock Input	ext_clk
		reset		Reset Input	[clk]
		s0	pipeline_bridge_s0	Avalon Memory Mapped Slave	[clk]
		m0		Avalon Memory Mapped Master	[clk]
<input checked="" type="checkbox"/>		ddr3_sdr		DDR3 SDRAM Controller with UniPHY	
		memory		Conduit	
		clock_sink		Clock Input	ext_clk
		clock_sink_reset		Reset Input	[clock_si
		clock_source		Clock Output	ddr3_sdr
		half_clock_source		Clock Output	ddr3_sdr
		Other		Conduit	
		afi_cal_debug		Conduit	

Component Library

Library

- Clock Source
- Reset Bridge
- Bridges and Adapters
- Custom Modules
- Debug Components
- Digital Signal Processing
- Interface Protocols
- Memories and Memory Control
- DMA

New... Edit... Add...

Messages

Description	Path
3 Errors	
7 Warnings	
2 Info Messages	

3 Errors, 7 Warnings

System Contents

Messages: System Validation

System Level Design: Why Use Qsys

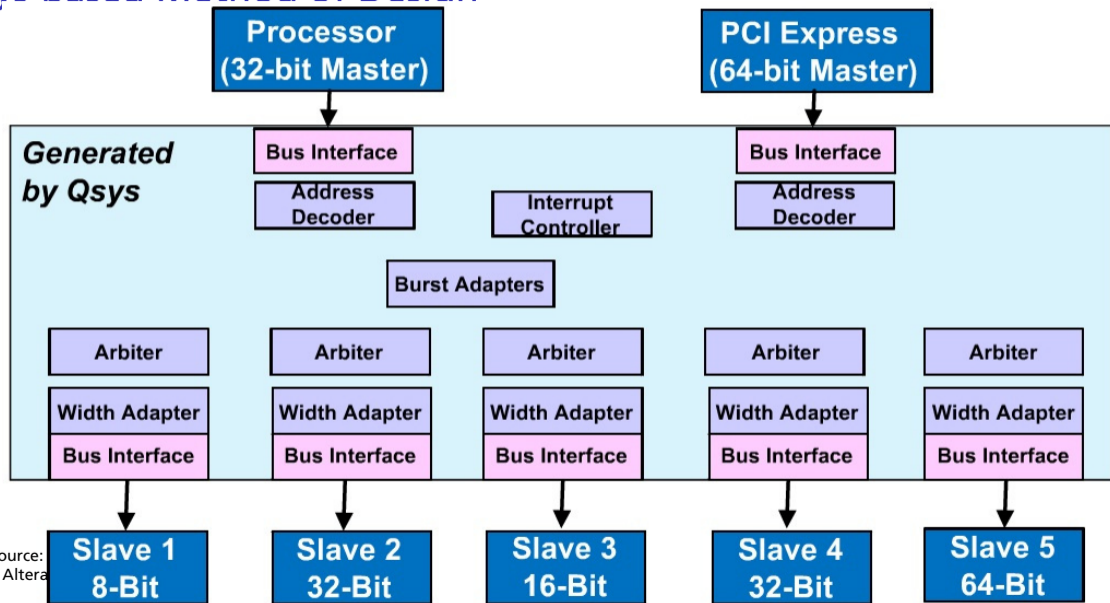
Avoids manually developing custom interconnect fabrics and signaling.

Instead of cycle-to-cycle coordination between every individual IP core, focus on transaction-level designs.

Design IP without knowing exactly when data will transfer and instead only focus on how (once it does).

(Only valid if you design your individual components to one of the standardized interfaces)

Qsys-based Method of Design



Source:
Altera

Connecting IP Cores

Interface Types

Memory-mapped Interfaces:

Avalon MM (Altera)

AXI (ARM, supported by Qsys now for SoC)

Streaming Interfaces: Avalon ST:

Avalon ST source port: outputs streaming data

Avalon ST sink port: receives incoming streaming data

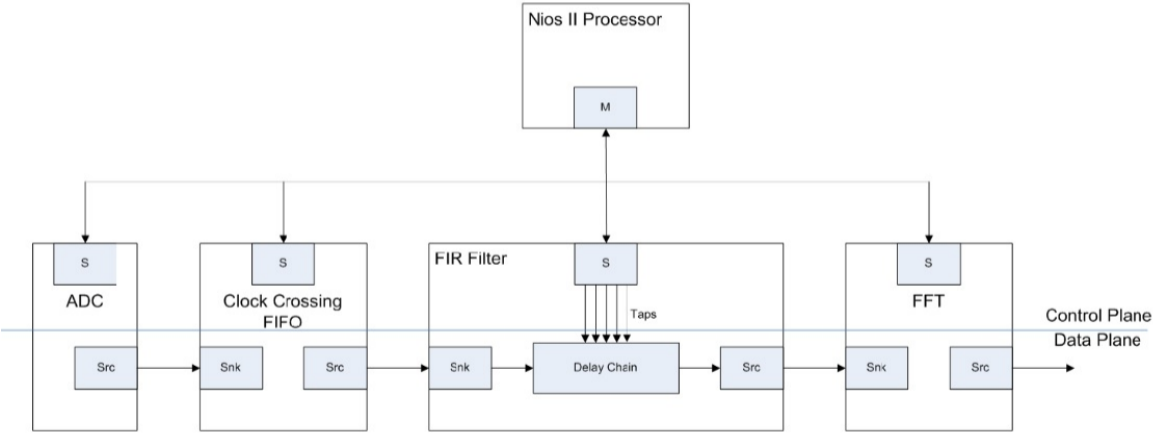
Control vs. Data Planes

Control Plane: Memory mapped registers typically used for configuring devices, querying status, initiating transactions, etc (low bandwidth)

Data Plane: Streaming directed graphs for actually moving and processing large amounts of data (audio/video, network packets, etc); high bandwidth

A single IP core can have both MM and ST interfaces (including multiple of each).

Control and Data Planes Example



Source: Altera

Additional References

Altera online training lectures: (HIGHLY recommended; many of these slides are taken directly from them)

<http://www.altera.com/education/training/curriculum/trn-curriculum.html>

Introduction to Qsys

Advanced System Design Using Qsys

Custom IP Development Using Avalon and AXI Interfaces

(Everything has moved to Intel; above link still works)