

High Frequency Trade Book Builder using FPGA

1st Choka Thenappan
MS Computer Engineering
Columbia University
ct3185@columbia.edu

2nd Shivam Shekhar
MS Computer Engineering
Columbia University
ss6960@columbia.edu

3rd Ameya Mallya
BS Computer Engineering
Columbia University
am6024@columbia.edu

Abstract—High-frequency trading (HFT) is a form of algorithmic trading that involves the rapid execution of a large number of orders at extremely high speeds. Key characteristics include: Speed, Low Latency, High Order-to-Trade Ratios, Market Making and Accuracy. The HFT engine is responsible for receiving this data, parsing it with the protocol provided by the exchange, updating its internal state about the market, submitting orders back to the exchange in reaction to market updates, and storing the buy and trade in a sorted order book that keeps records per share. In this project, we to build a Low-Latency FPGA based Order book for High Frequency Trading.

I. INTRODUCTION

High-frequency trading (HFT) refers to the practice of using powerful computers and algorithms to execute trades at extremely high speeds in financial markets. These trades are typically executed in fractions of a second, taking advantage of small price discrepancies or market inefficiencies. Key Components of High-Frequency Trading

- **Low-Latency Infrastructure:** HFT firms invest significant resources in building ultra-fast trading infrastructure to minimize latency—the time it takes for data to travel from one point to another.
- **Market Data Feeds:** HFT firms subscribe to direct market data feeds from exchanges, which provide real-time information about prices, trade volumes, order book changes, and other relevant market data. These data feeds are crucial for making split-second trading decisions.
- **Execution Platforms:** HFT firms use advanced trading platforms and execution systems capable of processing large volumes of orders rapidly. These platforms often feature co-location services, which allow firms to place their trading servers in close proximity to exchange servers for further latency reduction.

While it's possible to implement high-frequency trading (HFT) strategies using software running on traditional CPUs, there are several limitations that make FPGAs a preferred choice for many HFT applications:

- **Latency:** FPGAs offer significantly lower latency compared to software running on CPUs as they allow for the implementation of trading algorithms directly in hardware, bypassing the overhead associated with executing instructions in software.
- **Parallelism:** FPGAs excel at parallel processing, allowing multiple tasks to be executed simultaneously that can be harnessed to process large volumes of market data and

make numerous trade decisions concurrently, improving overall throughput and responsiveness.

- **Low-Level Access to Hardware:** FPGAs provide direct access to hardware resources, allowing for fine-grained control and optimization of the underlying hardware architecture, whereas software running on CPUs operates at a higher level of abstraction and may be subject to limitations imposed by the operating system or underlying hardware platform.

II. ALGORITHM EXPLANATION

In high-frequency trading (HFT), an order book is a real-time, continuously updated list of buy and sell orders for a particular stocks. The order book displays the current market depth, showing the quantity of shares or contracts that traders are willing to buy or sell at different price levels. It plays a crucial role in the price discovery process and provides important information for traders looking to execute trades. In short, order book is keeps track of the market state and the Trading logic uses these information to make trading decisions.

The Order Book we are implementing is an adaptation from [1]. The order book is structured as a binary search tree based on prices, with each price having an internally sorted linked list according to the time of arrival. In order to uniquely identify orders placed we will use a serial number which normally is assigned by the exchange. The size of the book also called the depth depends on the number of stocks we wish to keep track of.

III. IMPLEMENTATION

For the Implementation we will simulate an real-world situation based oh how these accelerators will be deployed. For this we will use the following components:

- FPGA
- VGA Monitor

We will connect the FPGA to our micro PC and have a program that sends market information to the FPGA, this setup will help us simulate the exchange. This data inside the FPGA will go to the parser module which will then process this information and send update requests to the order book to keep track of the current state of the market.

Implementing the trading logic is not feasible within the given timeline. The complexity arises from the sequential

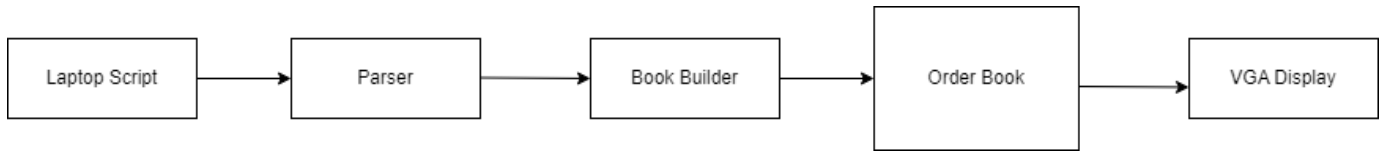


Fig. 1. Block Diagram for Book Keeping

nature of the order book, making it challenging to efficiently implement on an FPGA, which is a parallel processing unit.

IV. MILESTONES

- **First Milestone :**

- Integrating the FPGA with the test script running locally.
- VGA setup to display the order book.
- Setting up the pipeline for the process.

- **Second Milestone :**

- Creating the Parser Module
- Creating order book
- Integrating the order book to the pipeline (*test script* → *parser* → *bookbuilder* → *orderbook*)

- **Third Milestone :**

- Completing the pipeline for the project
- Performance Optimization

REFERENCES

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- [2] <https://web.mit.edu/6.111/volume2/www/f2019/projects/endriasprojectproposalRevision.pdf> "HFT Accelerator"