

CSEE 4840: Embedded Systems Project Proposal: Broadcasting Real-Time Video Capture to VGA Monitor

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Abstract – [Since its inception, video has gone on to become a vital source of entertainment for millions around the globe. Despite its wide use, the process of converting data captured from a camera to the video that one ultimately views is a challenging and difficult task that isn't often mentioned. In this proposal, our team outlines the motivation behind this project proposal while also discussing some possible challenges. A brief discussion regarding the software and hardware that will be required is also included along with milestones that our team has set for our project.]

1. Project Overview

Prior to the 19th century the only method to experience somebody else's memories or witness an event was to go out and experience it for oneself. Everything changed however with the introduction of video, a method that allowed people to capture events using a recording device and then convert it into a form that was viewable on a display. Today millions enjoy the many forms of media that video has to offer from providing a method to record their most cherished moments such as a wedding, to enjoying the latest blockbuster movie or just laughing to a short clip from social media. However despite its widespread popularity and extensive use by everyday people, the actual process of converting a camera feed into a viewable video format is quite complex and difficult especially for the standards that one expects from video today such as 4K resolutions. It is with these details in mind that our group is motivated to center the project around video in an effort to gain a deeper appreciation and understanding of what goes into creating the video that is central to many of our lives.

The goal of this project is to utilize a DE1-SoC FPGA to facilitate the conversion from the live-feed of an external camera to produce a video of the data being captured by the camera to two separate external VGA monitors. One will be outputted directly from the FPGA whereas the other will be sent over the network onto a server. One of the biggest challenges we foresee is processing the data. Mainly regarding whether it will be possible to achieve a video display with RGB or if this will prove to be too difficult within our timeline in which case our group will prioritize achieving a black and white video.

I. Design: Hardware and Software



Figure 1: OV7670 VGA CMOS Camera Module

The input for the project will come from a OV7670 VGA CMOS Camera Module that is capable of outputting data to I2C. This will require us to find a method to input this data so that it is available to the software located on the FPGA similar to how the keyboard was utilized as an input device in LAB 2. This will also involve making sure that the FPGA is configured correctly to ensure it follows the bus protocol of I2C. Once the FPGA is set up to take in the data correctly the focus will shift to being able to establish two separate displays. One will be a direct output onto a monitor whereas the second one will be a bit more in depth as the idea is to transmit it over the network to a separate display. This will involve utilizing a frame buffer to specify the color (or intensity of black in the case color is too difficult) of each pixel as well as map them correctly onto the screen utilizing VGA as an output. While the exact details are still unknown we suspect that careful attention will have to be placed in regards to raster scanning utilized to produce the video output as well as setting up the networking correctly. The final optimization that we anticipate will be required is to ensure the screen does not produce any weird glitches or shearing and that the final product will mimic the incoming feed from the camera.

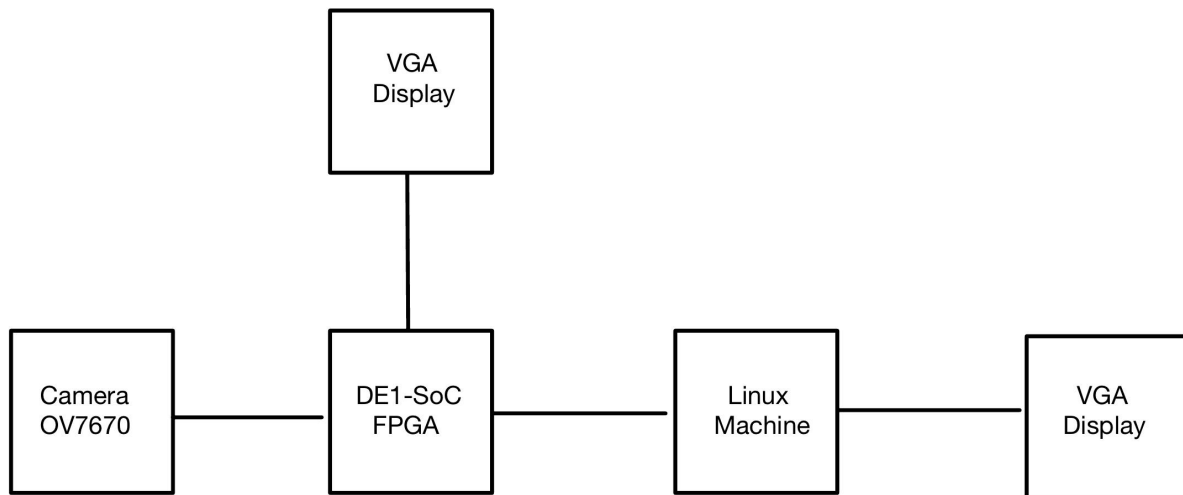


Figure 2: Block Diagram for proposed project.

II. Milestones

Milestone 1 (25%): Interface Camera with the FPGA using I2C protocol. The goal for this milestone is get the FPGA communicating with the camera by following the I2C protocol so we can begin processing the raw data coming from the camera.

Milestone 2 (50%): Networking. For this milestone the main goal is to sort out the networking portion of the project. At this point the fpga should be able to communicate with a computer in the network and be able to start to send the pixels that have been processed.

Milestone 3 (75%): Achieve raw live-feed video on VGA display. For this milestone, our project should be capable of displaying a very raw version of the live-feed. The display should be recognizable but will probably contain glitches and issues that make it behave weirdly.